IPC Tutorial Topic 3:

Evaluation of No-clean Pb-free Halogen-free Solder Pastes That Can Effectively Mitigate Head-in-Pillow Defects and Have Good In-Circuit Testability

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Pb-free

CISCO

Outline

- Background and Objective
- Head-in-Pillow (HiP) Defect
- In Circuit Test (ICT) Testability
- Evaluation Steps
  - ❖ Solder Paste Selection
  - ❖ Head-in-Pillow Test
  - ❖ Printability & Solderability Tests
  - ❖ Surface Insulation Resistance (SIR), Electrochemical Migration (ECM) & Ion Chromatography (IC) Tests
  - ❖ Verification Build

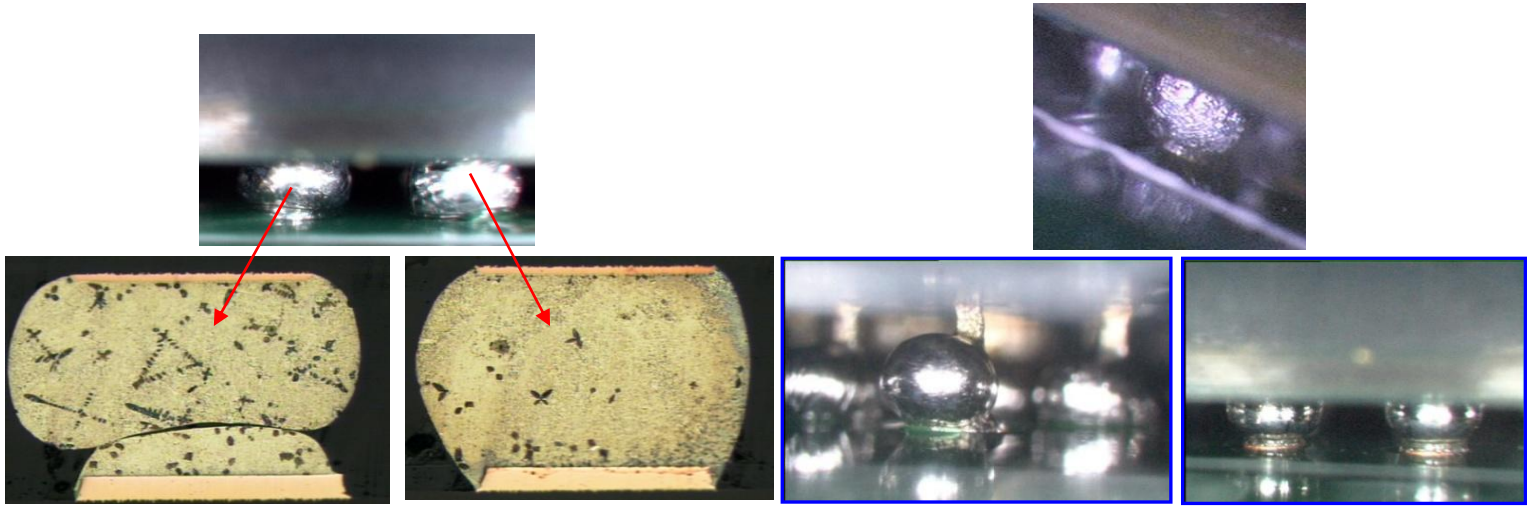
Background and Objective

- **Background**
  - There are several possible root causes for HiP, the root cause at Cisco seems to be component warpage
  - Pb-free process will increase HiP defect due to higher reflow temperature, which causes more component warpage
  - Optimization of PCB assembly process can not completely prevent HiP from forming
  - There are some ICT contact issues with our manufacturing partners' Pb-free solder pastes
  - If solder paste flux can remain active throughout reflow period and removes the oxide layer on BGA solder balls, good solder joint formation is still possible
  - Proper solder paste chemistry can provide wider process window to mitigate HiP defect and improve ICT testability

- **Objective**
  - Standardize Cisco qualified no-clean Pb-free solder pastes (SnAgCu with 3.0-4.0% Ag and 0.5±0.2% Cu & flux type ROL0)
  - Deploy the qualified pastes on Cisco products
  - Evaluate no-clean Pb-free Halogen-free solder pastes, which can effectively mitigate HiP defect and also have good ICT testability
  - Identify the best pastes by performing HiP test, printability & solderability tests, SIR, ECM & IC tests and verification build

Head-in-Pillow Defect

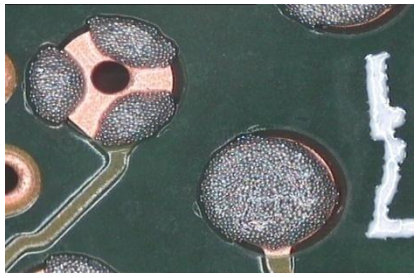
- HiP is a solder joint defect in which solder paste wets pad, but does not coalesce with BGA ball together
- HiP defects often pass electrical tests due to partial connection between BGA ball and solder
- Due to lack of solder joint strength, components with HiP defect may fail under minimal mechanical or thermal stress in the field

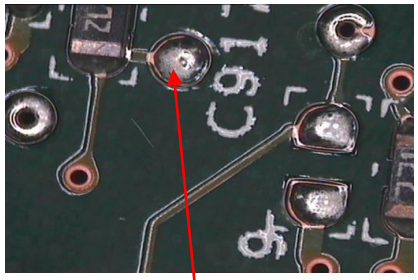


HiP Good joint

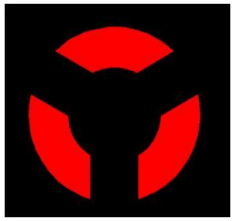
ICT Testability

- No-clean process has been implemented to all Cisco products in both SnPb and Pb-free processes, flux residue is left on PCBA
- Solder paste should have ICT probe-testable flux residue on both test pads and test via pads



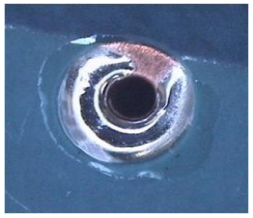


Reflowed test pad

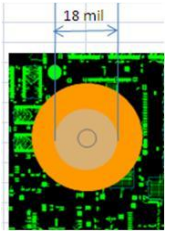


Three stoke stencil open

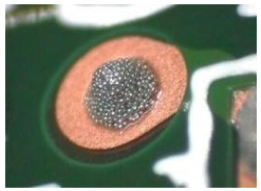
After paste printing



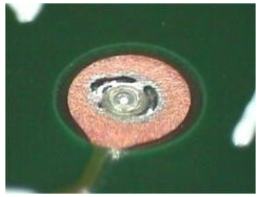
After reflow



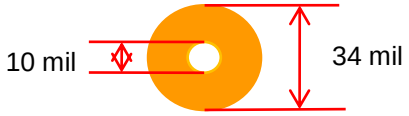
18 mil round centered on via hole stencil open



After paste printing



After reflow



ICT test via pad dimension

Evaluation Steps

- Phase 1, Solder paste selection
- Phase 2, Head-in-pillow test
- Phase 3, Printability & solderability tests
- Phase 4, SIR, ECM & IC tests
- Phase 5, Verification build

Phase 1, Solder Paste Selection

Solder Paste Selection

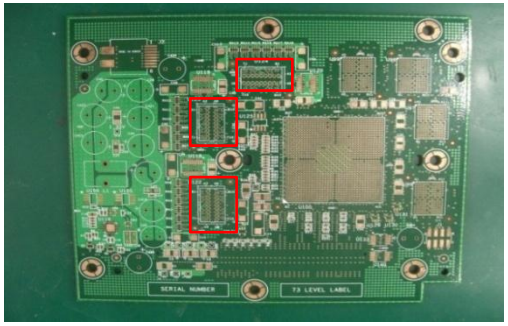
- **Six major solder paste suppliers and our manufacturing partners (MPa) are requested to provide their recommendations based on the following questions**
  - What is your recommendation for a no-clean Pb-free Halogen-free paste that can mitigate HiP defects ?
  - Does this paste satisfy all Cisco requirements ? please provide data to support
  - What are the special properties of this paste that mitigates HiP defect?
  - What are the activation and deactivation temperatures of the flux system ?
  - Does the flux in this paste stay on the top or it flows out after melting?
  - Is the flux active throughout time above liquidous ?
  - What is the flux type ?
  - Is the paste halogen-free ?
  - Is this paste used by any major MPa in production?
  - What is the history of usage for this paste?
  - Is this paste manufactured in China ?
  - How is ICT testability ?
  - What are SIR, Electrochemical migration and Ion chromatography test results ?

- **Seven solder pastes (A, B, C, D, E, F & G) are selected into this evaluation**
  - SAC305 solder alloy
  - Halogen free
  - ROL0 flux type classification

Phase 2, Head-in-Pillow Test

HiP Test Methodology

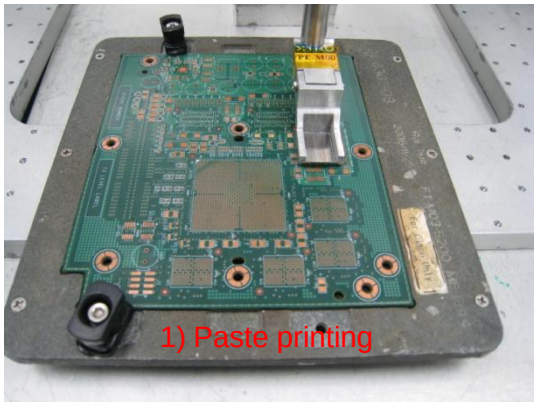
- **Test board and Pb-free BGA**
  - Test board: 152 x 131 x 2.4 mm, OSP finish
  - BGA: 0.8 mm pitch, 92 I/Os
  - BGA ball height & diameter: 0.3 mm and 0.4 mm
  - BGA package size: 9.2 x 15 x 0.9 mm

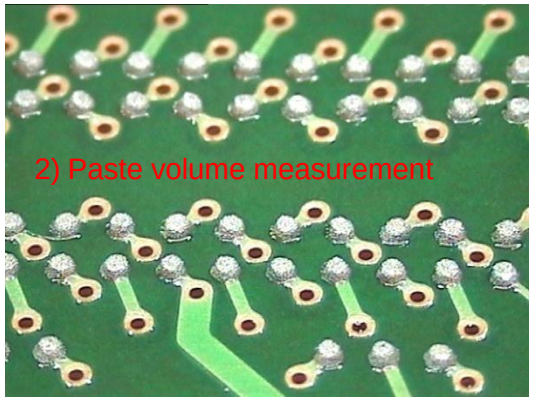


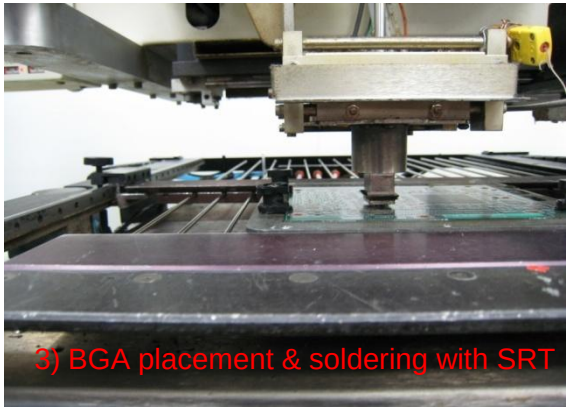
- **HiP test methodology**
  - SRT-1800 rework station is used to hold one BGA above molten solder then place the BGA later at the defined temperatures to simulate component warpage condition in reflow
  - Paste is first tested at 225 degree C
  - If there are more HiP at 225 degree C then next the paste is tested at 220 degree C, otherwise, tested at 230 degree C
  - Each paste is tested at two temperatures

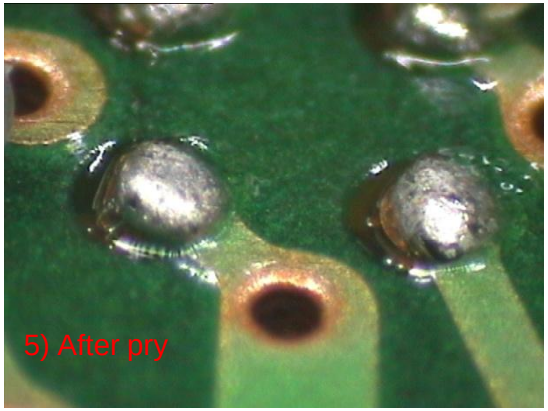
- **HiP test steps**
  - Print solder paste with mini stencil
  - Measure solder paste volume
  - Place one BGA on top of molten solder when the solder temperature reaches 220, 225 and 230 degree C and solder it with BGA rework station SRT-1800
  - Check the BGA with 5DX (5 slices), 2D X-ray and pry test to find out how many pillow joints occurred

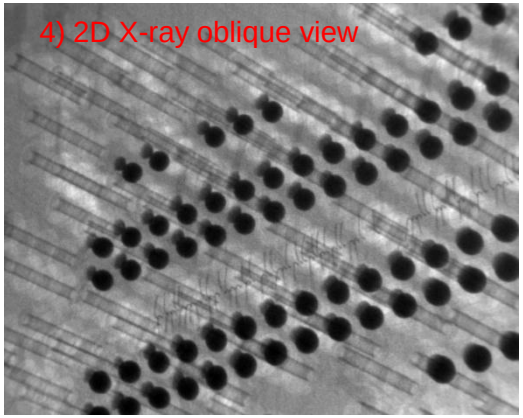
HiP Test Steps

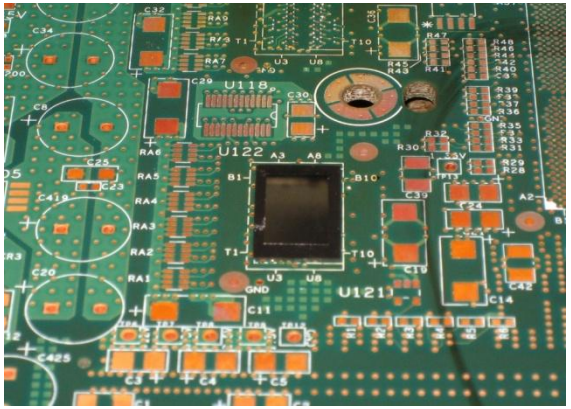








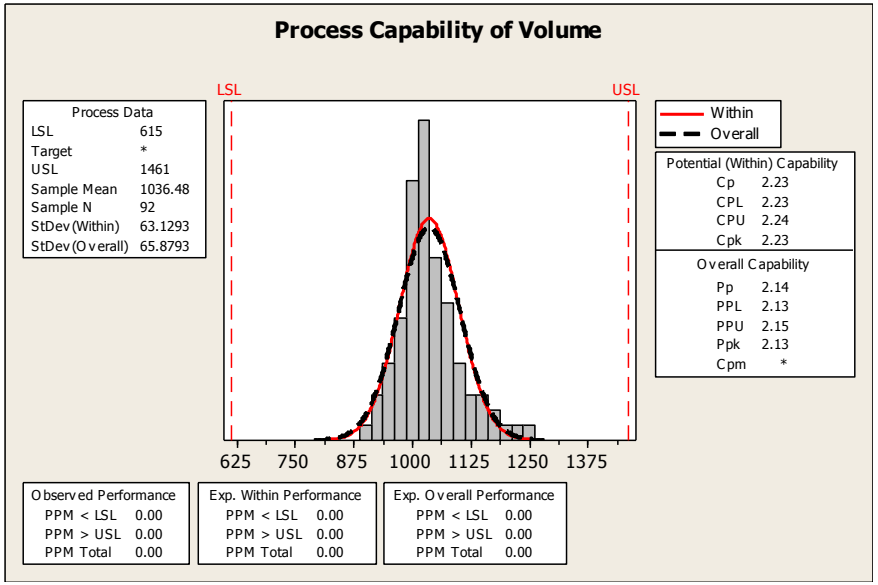


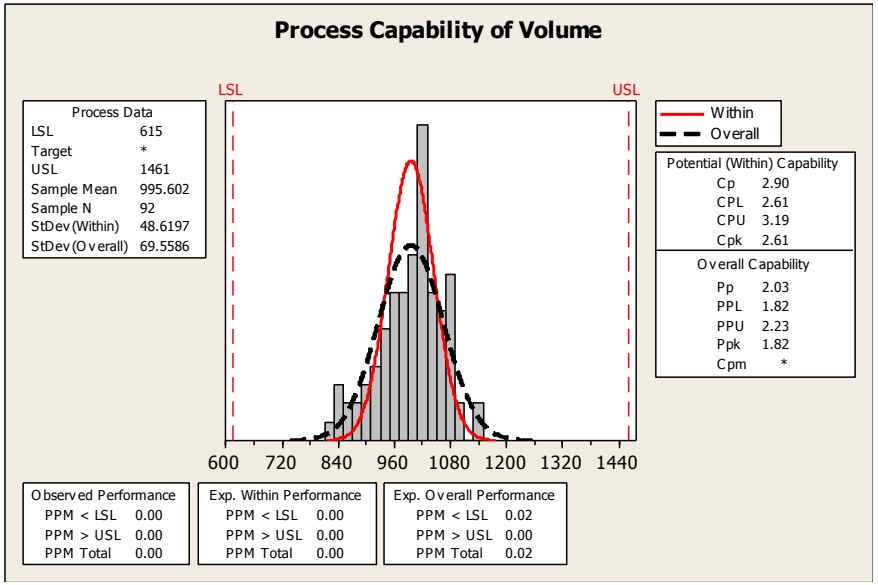


HiP Test Video, 2 min

Solder Paste Volume Measurement

- **Solder paste volume measurement with SPI CyberOptics SE 300**
- **Paste printing process capability C_{pk} calculation**
  - Nominal volume: 769 mil^3 (round stencil open: 14 mil in diameter & 5 mil thick)
  - LSL: 80% of nominal volume, 615 mil^3
  - USL: 190% of nominal volume, 1461 mil^3





Initial HiP Test Results

- Following table shows the number of HiP defects occurred at each temperature
- One BGA (92 I/Os) is placed and soldered at defined temperatures for each paste
- The ranking is based on the number of HiP defects when HiP first occurred
- Top five pastes are chosen to replicate of HiP test

Solder paste	HiP @ 220C	HiP @ 225C	HiP @ 230C	Ranking
G	N/A	0	0	1
D	N/A	0	53	2
C	N/A	4	26	3
A	1	28	N/A	4
B	5	79	N/A	5
F	11	20	N/A	6
E	19	80	N/A	7

Results for Replicate of HiP Test

- Following table shows the number of HiP defects occurred at each temperature
- Three BGAs (S1, S2 & S3) are placed and soldered at defined temperatures for each paste
- The ranking is based on the number of HiP defects when HiP first occurred

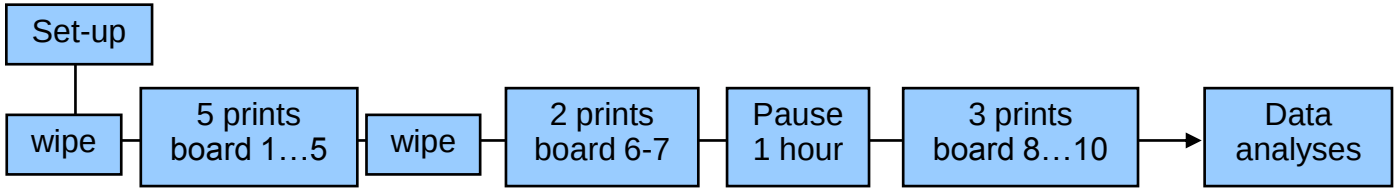
Solder pastes	Temperature	S1, HiP	S2, HiP	S3, HiP	Average HiP	Ranking	Initial HiP test result	Initial HiP test ranking
	225C	0	0	0	0		0	
G	230C	0	0	7	2	1	0	1
	225C	0	1	0	0		0	
D	230C	17	6	29	17	2	53	2
	225C	0	0	9	3		4	
C	230C	4	1	22	9	3	26	3
	220C	0	0	1	0		1	
A	225C	7	48	25	27	4	28	4
	220C	8	0	1	3		5	
B	225C	70	49	38	52	5	79	5

Phase 3, Printability & Solderability Tests

Printability Test

- **Paste printing test**
  - ❖ Five solder pastes (A, B, C, D & G)
  - ❖ Printing process capability analyses
  - ❖ Cold slump test (after 2 hours)
  - ❖ Downtime test (after 1 hour pause, no paste kneading before printing)

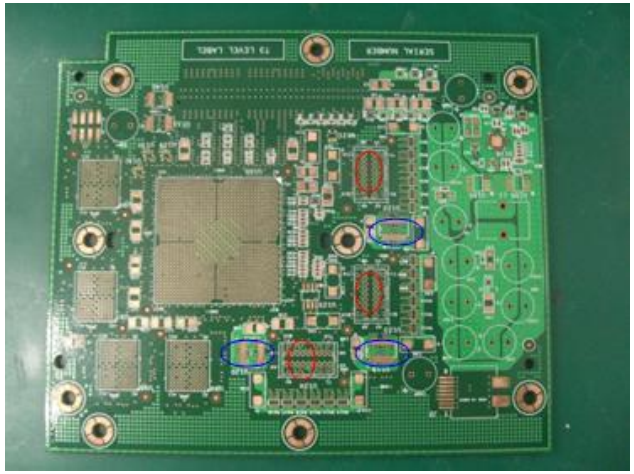
- **Printability test procedure is designed to simulate the worst conditions in mass production**



Printability test procedure

Printability Test Setup

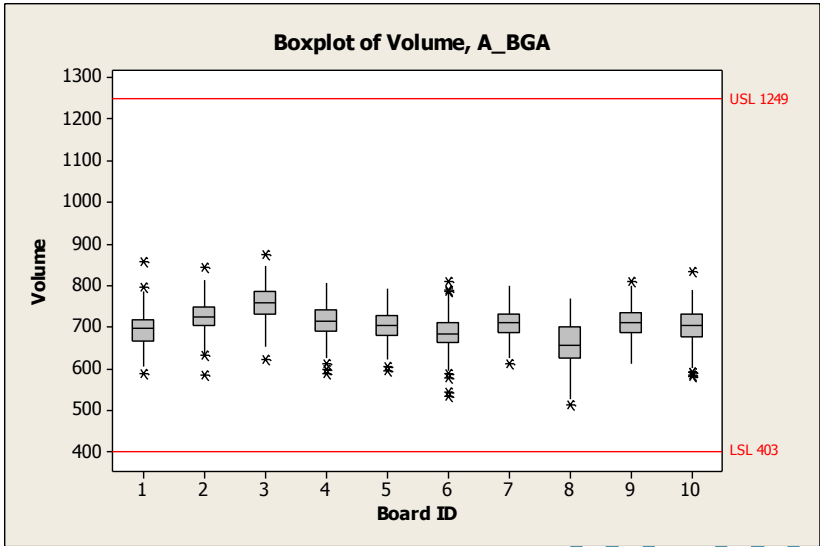
- **Paste printer: DEK FP Platform i Plus**
  - Front/rear print speed: 35 mm/s
  - Front/rear pressure: 10 kg
  - Separation speed: 0.3 mm/s
  - Stencil wipe cleaning: wet-vacuum-vacuum-dry
- **5 mil thick laser-cut stainless steel stencil**
- **All five pastes are tested with the same parameters**
- **Test vehicle**
  - Test board: 152 x 131 x 2.4 mm
  - Three BGA: 0.8 mm pitch, 92 I/Os
  - Three SSOP: 0.65 mm pitch, 24 pins



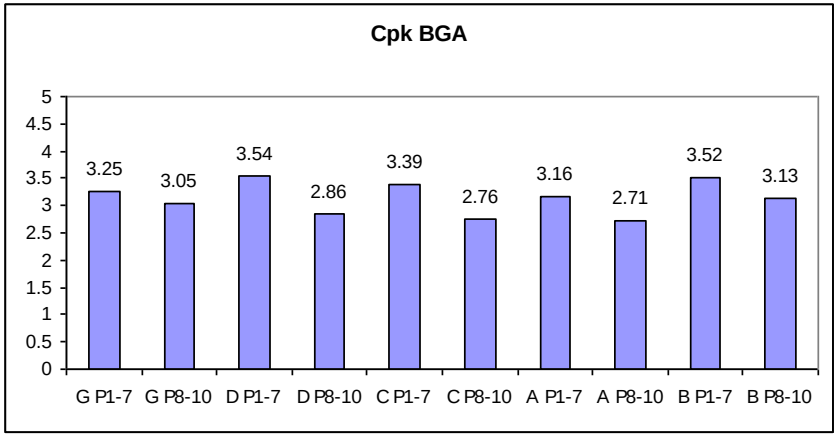
Printability Test Analyses

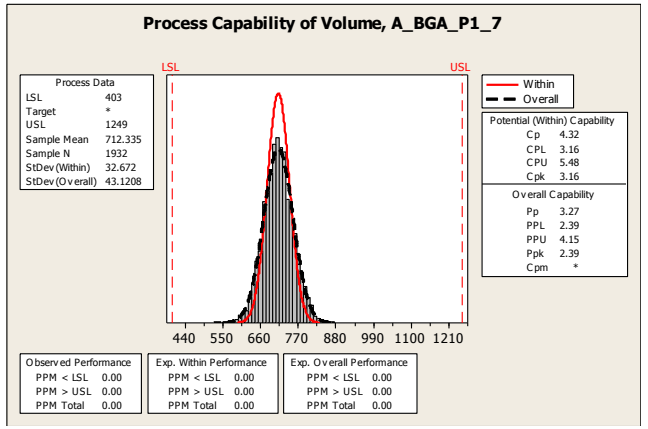
- **Paste deposit volume measurement with SPI CyberOptics SE 300**
- **Process capability analyses for paste deposit volume**
- **Paste deposit height analyses for cold slump test**

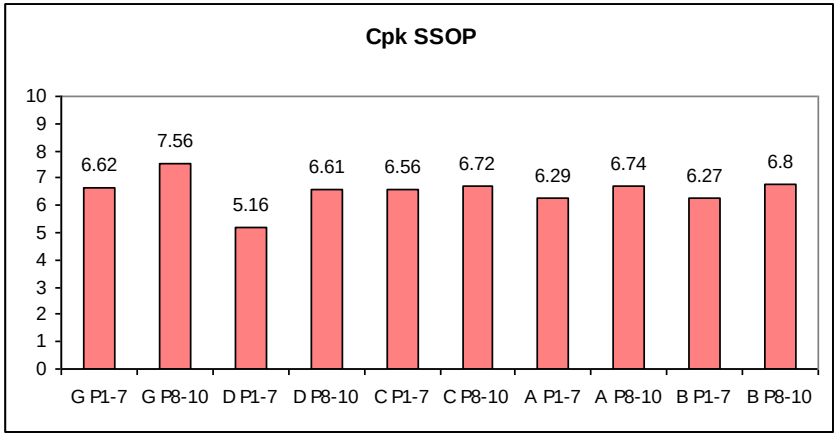
- **Specifications used in process capability analyses**
  - 0.8 mm pitch BGA
    - V_{nom} = 769 mil^3
    - LSL = 0.525 V_{nom} = 403 mil^3
    - USL = 1.625 V_{nom} = 1249 mil^3
  - 0.65 mm pitch SSOP
    - V_{nom} = 5880 mil^3
    - LSL= 0.525 V_{nom} = 3087 mil^3
    - USL = 1.625 V_{nom} = 9555 mil^3

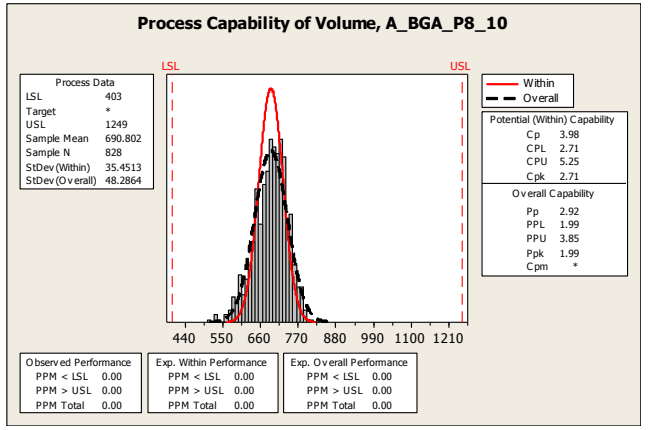


Paste Printing Process C_{pk} Summary





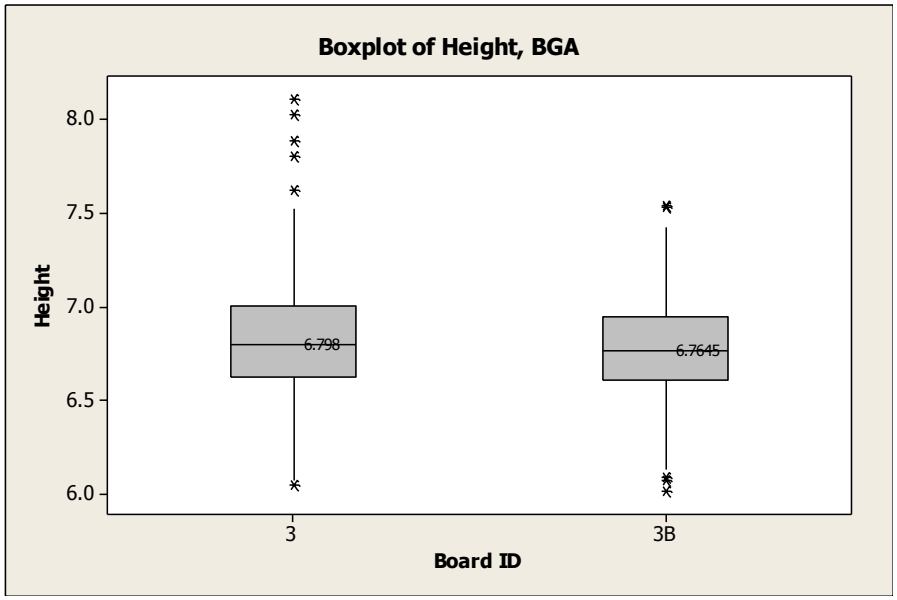


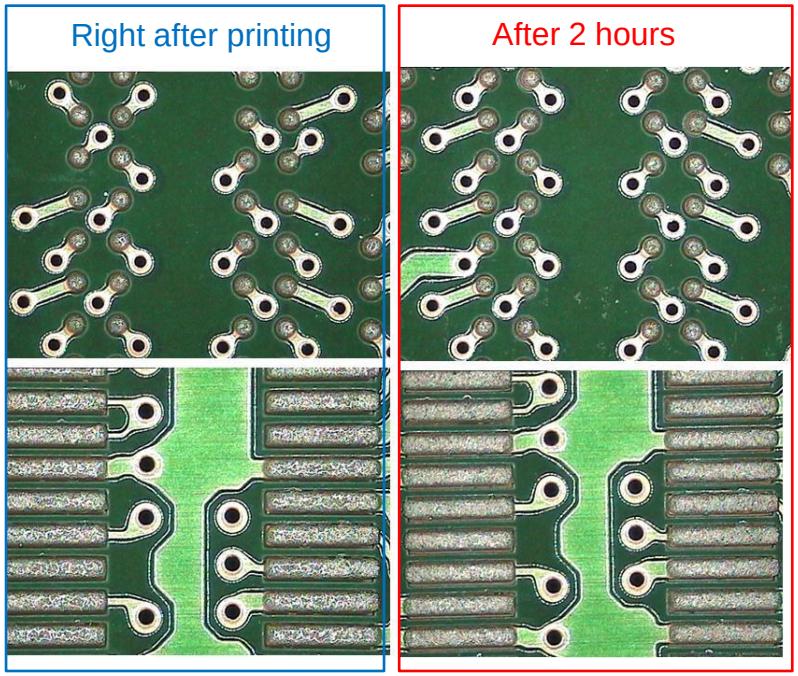


P1-7: print 1-7, P8-10: print 8-10

Cold Slump Test

- Board # 3 is chosen for cold slump test
- Board # 3 is measured once right after paste printing, data is shown as Board ID 3
- Board # 3 is measured the second time after 2 hours, data is shown as Board ID 3B



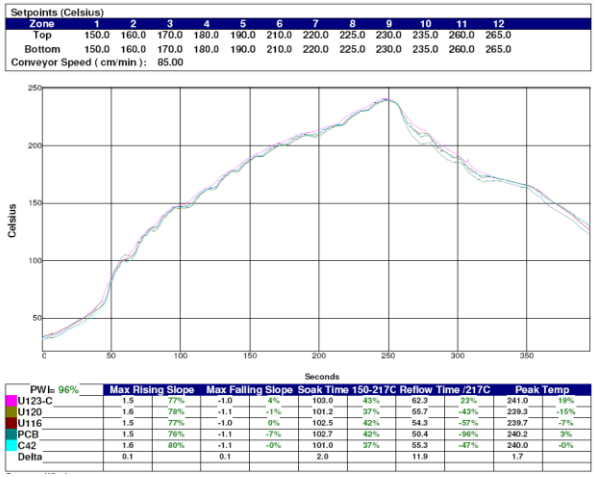


Solderability Test

- **Solderability test**
  - Five solder pastes (A, B, C, D & G)
  - Both air and N_2 (<300 PPM O_2 level) reflow
  - Cross-section analyses for the BGA U123
  - BGA and QFN voiding
  - Solder joint appearance
  - Wettability
  - Flux residue
  - Solder balling

- **All five pastes are tested under the same conditions**

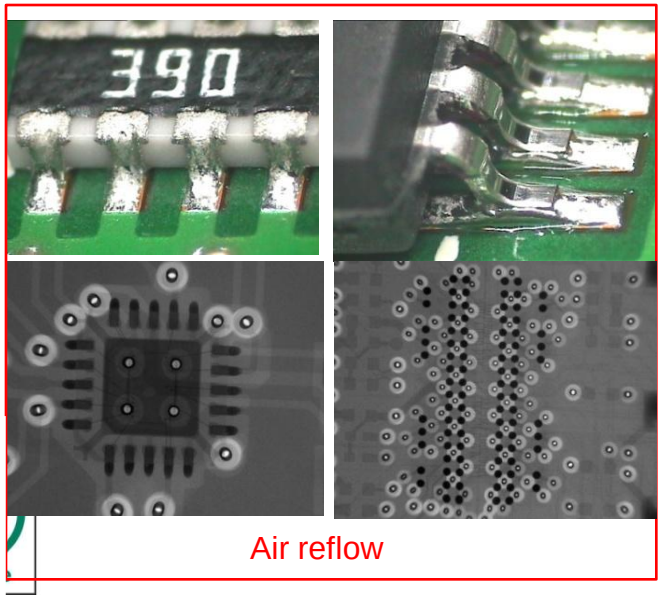
Reflowed board



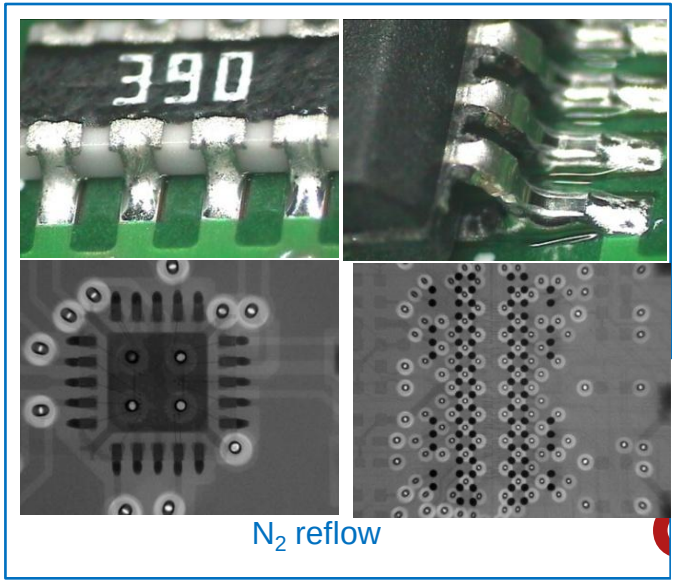
Reflow profile

Components in Solderability Test

Component Description	Component Location	QTY
CAP,TA, 100uF, 10V,10%,SM,2816,D CASE	C14	1
CAP, CE, 22uF,6.3V,20%,SM,1210,X5R	C42	1
RES,TF,22,.063W,5%,SM,0402,Pb-FREE	R18, R22, R23, R24	4
RNW,ISO, 39,5%, 4R,63mW,CRA8	RA1, RA12	2
IC,74LVC07A ,BUFR,HEX ,TSSOP14	U133	1
IC,W134S,RAMBUS CLK GEN,SSOP24,CAUTIO	U120	1
IC,DRAM-RAMBUS,512Kx18x32,1066MHz,uBGA92,Pbfree	U123	1
IC,IRU3039,PWM,DUALSYN,VTT-TRACK,QFN	U116	1
PCBFAB, 16L,OSP, CONGO NP DTRB		1

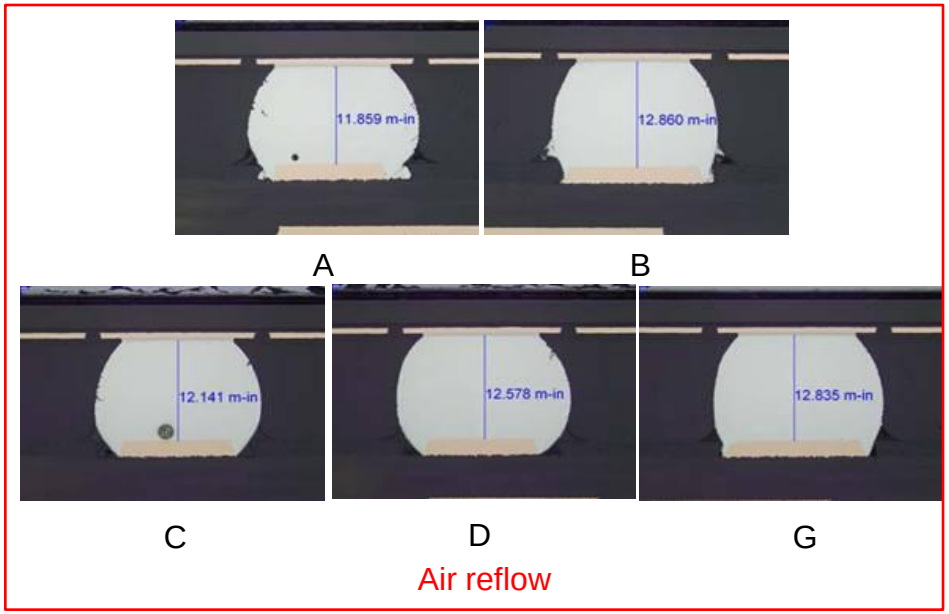


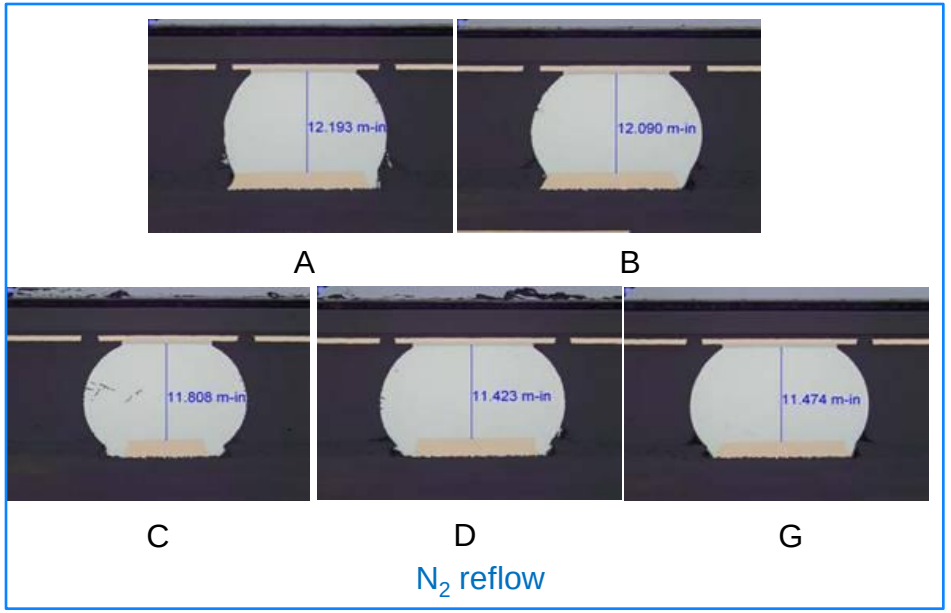
Air reflow



N_2 reflow

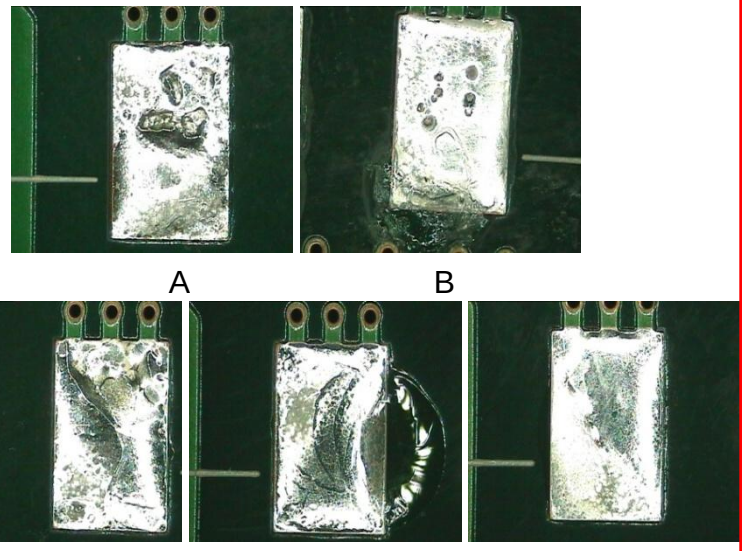
Cross-sections & Summary of 2D X-ray Inspection

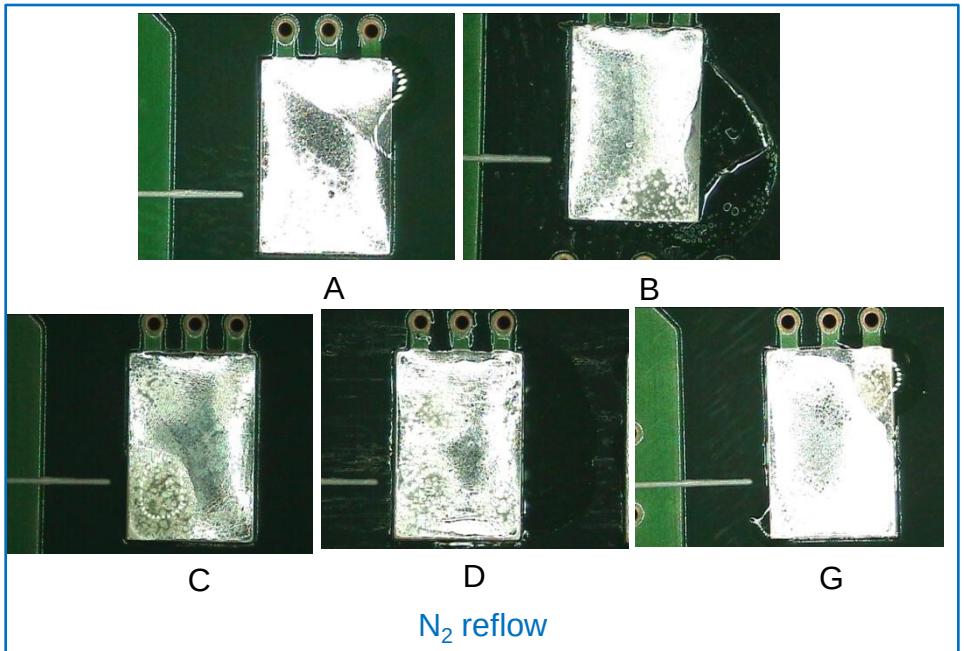




Sample #	Solder paste	Condition	Location	2D X-ray inspection	
				Max. % voids	Observation
1	A	Air reflow	U123	6.60%	No anomaly
2	B		U123	4.90%	No anomaly
3	C		U123	2.70%	No anomaly
4	D		U123	4.70%	No anomaly
5	G		U123	2.70%	No anomaly
6	A	N_2 reflow	U123	5.90%	No anomaly
7	B		U123	6.80%	No anomaly
8	C		U123	4.20%	No anomaly
9	D		U123	6.00%	No anomaly
10	G		U123	4.80%	No anomaly

Flux Residue with Air & N_2 Reflow





Summary of Printability & Solderability Tests

- **Printability Test**
  - ❖ All five pastes have very good printability even after 1 hour downtime
  - ❖ All five pastes have good cold slump performance

- **Solderability Tests**
  - ❖ All five pastes have good wetability and small BGA & QFN voids
  - ❖ No solder balling is found for all five pastes
  - ❖ N_2 reflow gives better wetting, bright solder joints and less flux residue
  - ❖ Paste A has soft and sticky flux residue with both air and N_2 reflow
  - ❖ Paste C has more brown flux residue
  - ❖ Pastes B, D and G have transparent and hard flux residue

Phase 4, SIR, ECM & IC Tests

SIR, ECM & IC Tests

- **Surface insulation resistance (SIR) test**
  - Per IPC-J-STD-004A, IPC-TM-650, Method 2.6.3.3
  - Per IPC-J-STD-004B, IPC-TM-650, Method 2.6.3.7

- **Electrochemical migration (ECM) test**
  - Per GR-78-Core, IPC-TM-650, Method 2.6.14.1

- **Ion chromatography (IC) test**
  - Per IPC-TM-650, Method 2.3.28

- **SIR, ECM & IC test results**

Solder paste	SIR 2.6.3.3	SIR 2.6.3.7	ECM 2.6.14.1	IC 2.3.28
A	Pass	Pass	Pass	Pass
B	Pass	Pass	Pass	Pass
C	Pass	Pass	Pass	Pass
D	Pass	Pass	Pass	Pass
G	Pass	Pass	Pass	Pass

3rd party test results for SIR and ECM

Phase 5, Verification Build

Test Board Information

- Board size: 366 x 254 x 1.6 mm
- Minimum pitch for BGA: 0.8 mm
- Maximum BGA I/O: 516
- Minimum pitch for QFP: 0.5 mm

Top side

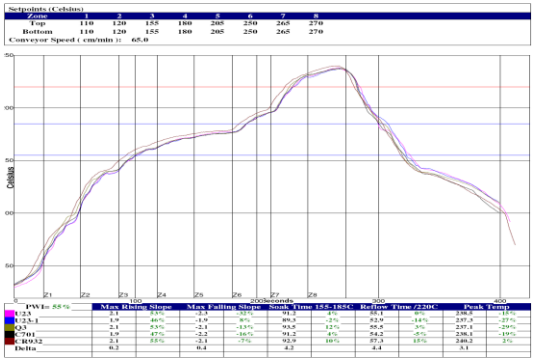
Bottom side

Verification Build Information

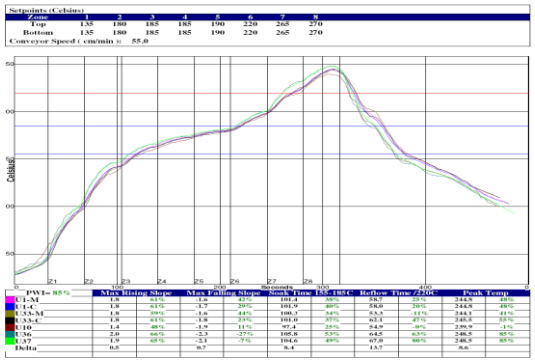
- 20 boards are built for each solder paste (A, B, C, D & G)
- All boards are reflowed with N_2, < 300 PPM O_2 level
- All boards are built, inspected and tested under the same conditions as current mass production
- SMT and ICT first pass yields (FPY) are used for performance comparison

- Paste printer setup
  - ❖ Front/rear print speed: 30 mm/s
  - ❖ Front/rear pressure: 8 kg
  - ❖ Separation speed: 0.3 mm/s
  - ❖ Stencil wipe cleaning: wet-vacuum-vacuum-dry

- Bottom & top side reflow profiles



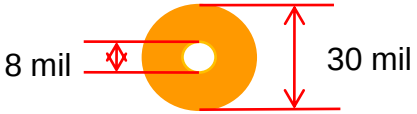
Bottom side



Top side

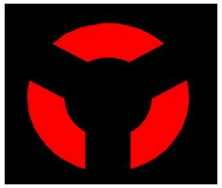
Bottom Side Stencil for Test Board

- **Solder paste is printed onto test via pads to check ICT testability**
- **Test via dimensions**
  - Outer diameter: 30 mil
  - Inner diameter: 8 mil



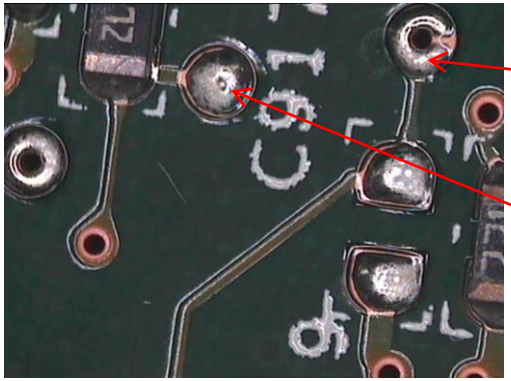
ICT test via pad dimension

- **Test via stencil open dimensions**
  - Stencil thickness: 4 mil
  - Outer diameter: 40 mil
  - Inner diameter: 15 mil
  - Open width: 10 mil

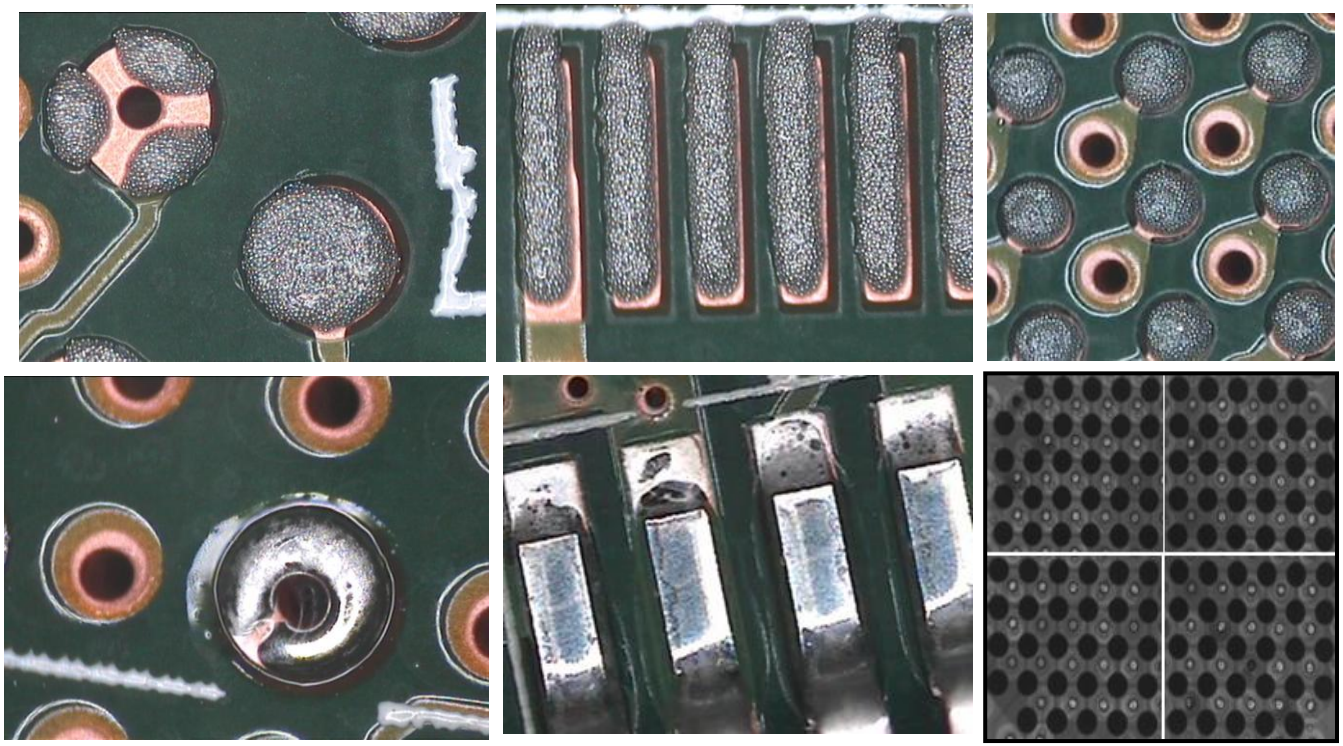


Stencil open

- **Reflowed test pad and test via pad**



Verification Build Results



Summary of Verification Build

Solder paste	SMT		ICT	
	Passed/Total	FPY	Passed/Total	FPY
G	20/20	100%	6/20	30%
C	20/20	100%	13/20	65%
B	20/20	100%	19/20	95%
D	20/20	100%	19/20	95%
A	20/20	100%	20/20	100%

Solder paste	Printing process C_{pk}	Cold slump after 1 hour	Solderability	BGA void
G	2.65	Good	Good	Good
C	1.96	Good	Good	Good
B	2.64	Good	Good	Good
D	2.25	Good	Good	Good
A	2.03	Good	Good	Good

Summary

- The HiP test method has showed repeatable results
- The printability test procedure has been proved to be a good way to check solder paste printability
- The qualified solder pastes show good printability & solderability, SMT and ICT FPY in the verification build
- The qualified solder pastes have been identified and deployed in mass production

Question ?

Thank You