3D Interconnection Technologies for Electronic Products: A Perspective View of Electronic Interconnection Technologies from Chip to System

Joseph Fjelstad
Verdant Electronics
Cupertino, CA

Abstract:
3D is the shorthand term for the three dimensions of Cartesian coordinate space X, Y and Z. With that definition in mind, one will find with little or no stretching of the imagination, that the first electrical interconnections, performed using discrete wires were unquestionably 3D. If one doubts it they can look at almost any electrical product from the time of the 19th century telegraph onward. 3D interconnections are found virtually everywhere. It is really 2D that is more illusive if one thinks about it. Even so, 3D interconnection solutions and options have dominated the electronics manufacturing industry's attention over the last few years and interest in the topic has been accelerating. The reasons for this interest are manifold but the root cause is that the third dimension provides the ability to extend the pursuit of ever greater density when the acknowledged physics based limits that will ultimately spell the end of Moore's Law kick in. In order to keep delivering the promise of better cost/performance metrics for each new generation of electronics, interconnection technologies which take advantage of the third dimension will play an increasing important role in the future. In fact electronic interconnection technologies will undoubtedly pace price and performance improvements for most if not all future electronic products and 3D interconnections will play a pivotal role. This paper discusses 3D solutions which have been used from past to present from chip to system and will included a glimpse of what might be ahead.

Introduction
The invention of the integrated circuit was a technological development of historic proportions. The IC has enabled countless products which have collectively accelerated the advance of global wealth and knowledge to extent that has likely far exceeded the dreams and expectations of the individuals credited with its conception, Jack Kilby of Texas Instruments and Robert Noyce of Fairchild and Intel and those who worked with them to make it possible. However before the IC there were discrete transistors in small packages and a compliment of discrete devices mounted on printed circuits which served the purpose. These assemblies where many times larger and engineers of the time did their best to conserve space and improve overall performance by using creative methods of interconnections which often took advantage of the third dimension to accomplish their objectives. Figure 1 shows an example of a transistor cordwood module from the late1950s which is unquestionably a 3D assembly.

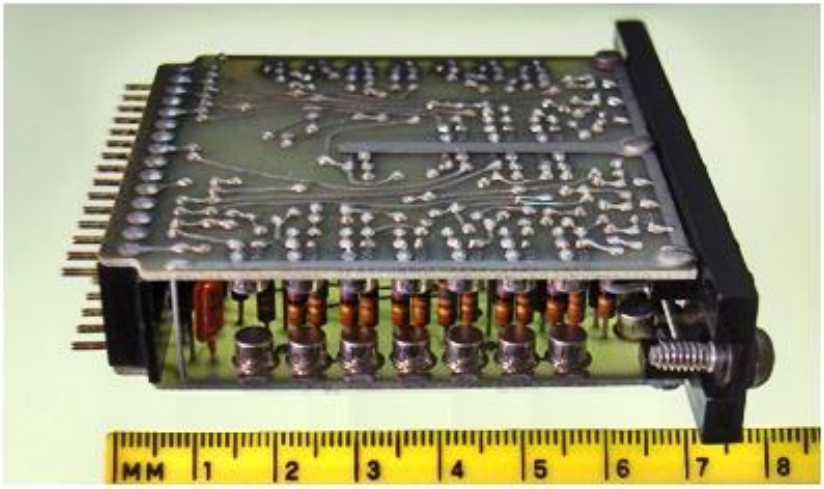


Figure 1 A "cordwood" module built by Control Data Corporation was developed to minimize connecting wire lengths and used a 3D stacked printed circuit arrangement to make electrical interconnections. (Source: Computer History Museum)

The first planar IC was fabricated by Fairchild in May 1960 and as the IC began to be commercialized by co-innovators and developers, Fairchild and Texas Instruments, each company went in search of markets. Fairchild's first IC products were called "Micrologic Elements," and were packaged in the then commonly available 8-lead TO-5 cans (which were interestingly reminiscent in shape and format to the vacuum tubes they were replacing) These were later replaced by the dual inline (DIP) package. Texas Instruments, on the other hand, introduced its IC and a new low profile packaging format at the same time.[i] The new package was called a "flat-pack" and was designed to be surface mounted.

It was a very good solution, however used of surface mount technology for components did not gain wide acceptance in the electronics industry until almost two decades later.

3D and IC Package – Stacking Chips and Packages

While there is a natural tendency to be enamored of the latest and greatest technological advances as harbingers of things to come, with a little bit of digging, one can often find that many of those things that seem to continually pop up have sprouted from seeds planted long ago. Perhaps the first (and maybe only) real 2D interconnection was the single metal layer printed circuit for as soon as the second side was added, it arguably became a 3D interconnection substrate. When two metal layers proved insufficient, inner layers were added and 3D was then unquestionably in play. The same arguments hold true for integrated circuit mentioned earlier.

Accepting these arguments one can begin to look back at the electronic "fossil record" and this was done by reviewing patents from the past for evidence of TSV (through silicon via), IC chip stacking and IC package stacking. While the search performed in preparation for this paper was neither extensive nor exhaustive, it did reveal that the back side of the IC was "discovered" as early as 1971 by two engineers at Honeywell in Italy. This is shown in the Figure 2.

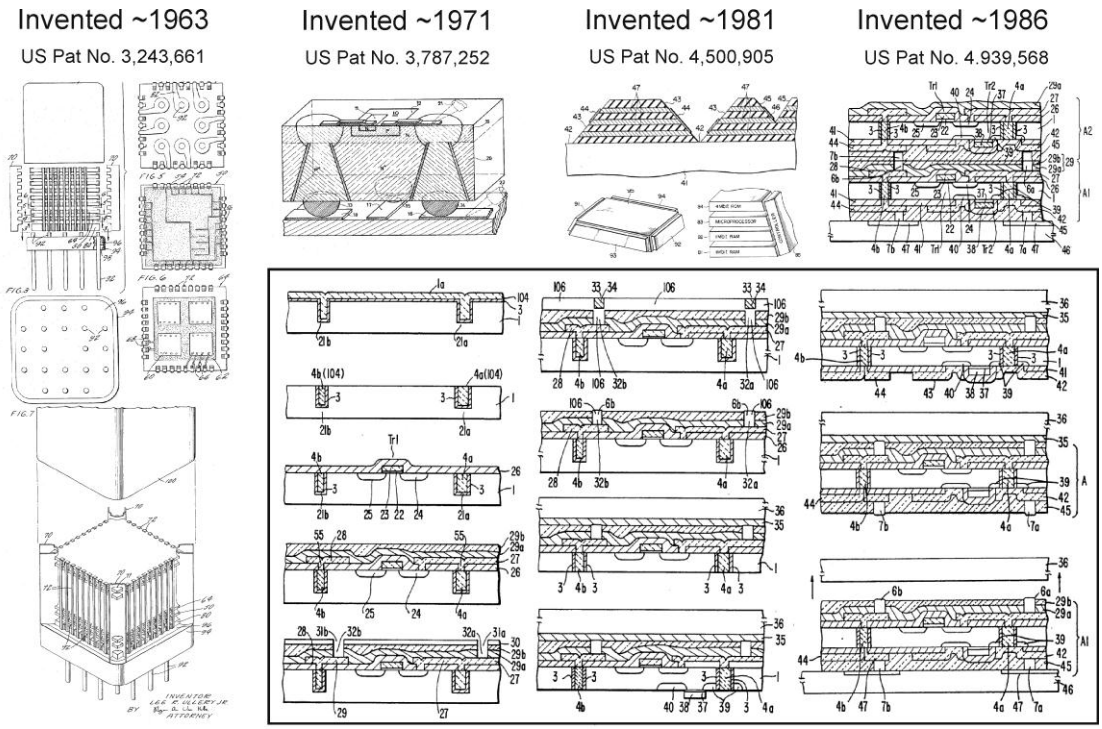


Figure 2 Above is a collage of patent drawings for early 3D concepts for packaging and interconnecting ICs. On the top from the left the titles and inventors for the patent drawings shown are: *"Enhanced micro-modules"* by Ullery, *"Connection means for semiconductor components and integrated circuits"* by Filippazzi, et al., **"***Stacked semiconductor device with sloping sides"* by Shibata and "*Three-dimensional integrated circuit and manufacturing method thereof"* by Kato, et al.
(Source: US Patent and Trademark Office)

While the possibilities of the back side of the chip were possibly noted and suggested earlier by others, because of the limited time spent in the search, this finding serves only to provide clear evidence that TSVs are actually are not all that new conceptually. Still, it is unquestionably true that the technology for TSVs has improved greatly over the years in an effort to refine processes for making them and those responsible for those improvements are equally deserving of credit for their efforts.

Looking further into the records, one will find processes detailing how to build 3D ICs which were being devised and disclosed in the early to mid 1980s at the latest. An example of such effort is present in a patent issued in to Fujitsu in 1990 based on work performed in the 1980s. Returning to the figure, one can see a product and process which show strong resemblance to processes and structures that are being described today some 20 years later.

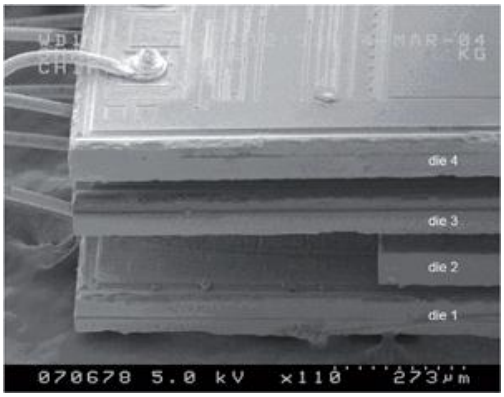


Figure 3 Stacked chip packages can help significantly conserve PCB real estate and with the use of thinned die, very little penalty in the Z axis, however, die yields must be near perfect. Such structures are commonly employed to create system in package (SiP) alternative solutions to the time and expense of designing a complex chip. (Source: unknown)

The stacking of chips in pyramidal fashion, ala, is often shown in cross section in technical presentations and papers on IC packaging technology advances, most often with the chips being interconnected by wire bonds. (see Figure 3) However a look backward in time reveals a structure that looks strikingly similar to an ancient ziggurats of Zoroaster from the 5th century BCE ziggurat, (refer back to Figure2)

The particular invention shown relies on edge connections, similar to a number or present day 3D solutions, is made more interesting by the inventor's cleverly thinking to use the sloped edges of the assembly for interconnecting and controlling the individual chips, thus creating a multichip electronic system. While there was no evidence found that this was ever reduced to practice, the inventor definitely understood the benefit of 3D in the 1980s.

The final item for discussion is one related to stacking of chip packages to create a chip package in the form of a device similar to a pin grid array (PGA). Once again, the potential benefit of the third dimension for creating a dense electronic assembly was clearly understood by at least one individual and the evidence can be found in Figure 2 and the time frame was the early 1960s, almost a half century ago. There have been significant improvements in density however as can be seen in Figure 4

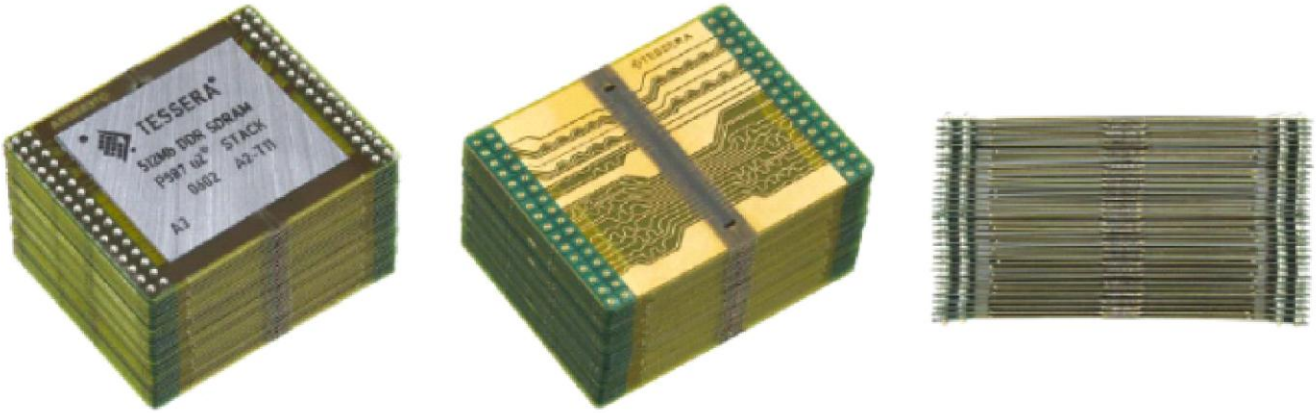


Figure 4 Top, bottom and side views of an extreme example of package stacking (Source: Tessera)

Thus the current world wide effort to take advantaged of the third dimension for making electronic interconnections from the chip to chip, wafer to wafer and package to package has deep roots. It seems fitting that those who passed the torch of innovation to the current generation should be given at least a small "tip of the hat" from time to time, for helping the industry get to where it is today, just as those who are creating the future today might hope from those who will be "pushing the ball" forward in the years to come.

3D for Printed Circuits and Backplanes

Printed circuit motherboards and backplanes have been using three dimensional concepts for many years, especially in the construction of computers.

Daughter cards have long been interconnected to computer mother boards in a perpendicular manner (see Figure 4) and the same for backplanes.

Both are most definitely a 3D interconnection assemblies, however, no one ever has made an overt point of it, it was simply a fact. (That said, the technique was applied to chips in some development projects in the 1980s and 1990s.)

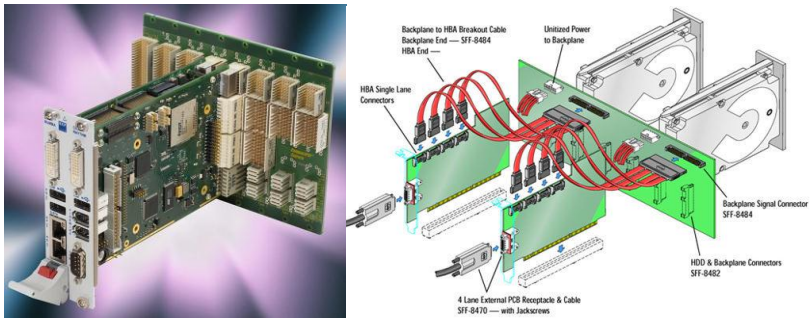


Figure 4 Examples of how the 3rd dimension has been employed for mother boards and backplanes
(Source: Industrial Computers and Information Technology)

The "two-dimensional" nature of printed circuit board backplanes is the root cause of many of the signal integrity problems in current high-speed electronic systems system noise and attenuation top the list. In response a novel three-dimensional backplane technology has been developed. (See Figure 5) The 3D design both addresses the signal via stub problem and opens the door to the use of wider high speed routing channels which have challenged designers by allowing them to be routed separately in a plane perpendicular to the main structure of the backplane on the side opposite the daughter cards. The proprietary design approach enables optimization of conductor width and spacing, minimizing conductive losses, by using a microstrip coplanar transmission line configuration to reduce dielectric losses even with standard materials. Low loss materials will further improve the performance.

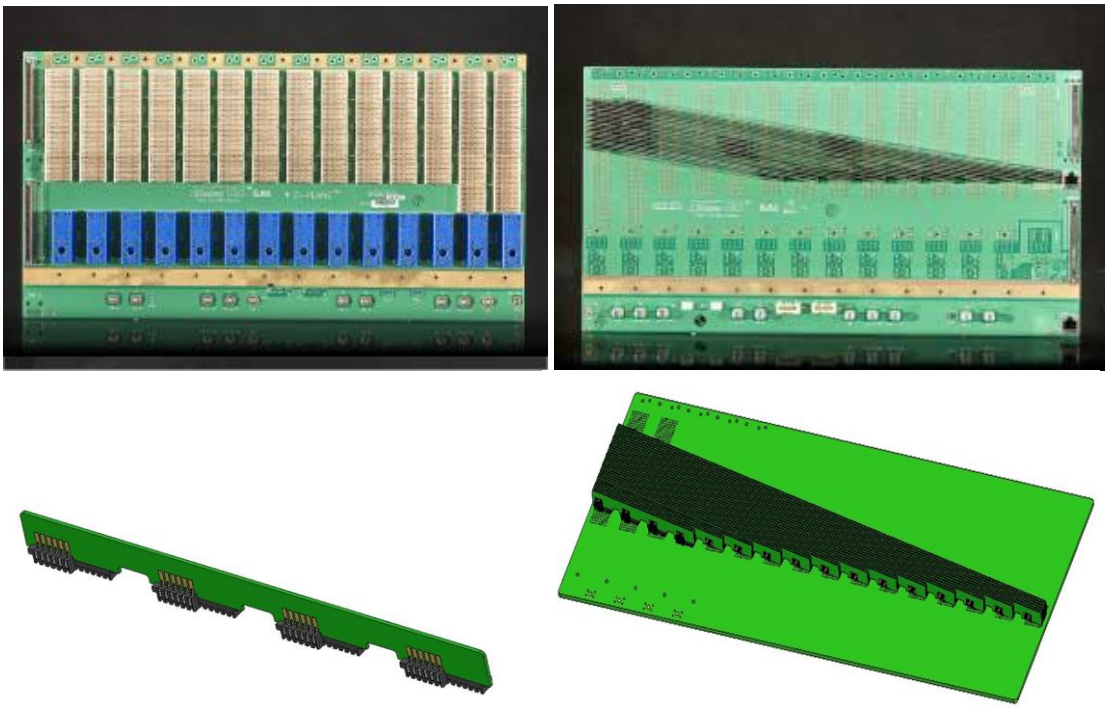


Figure 5 A newly developed approach to backplane design improves performance by routing high speed channels separately from the rest of the circuits of the board. Top row left and right images are front and back side views respectively and on the bottom left and right show an example of one of the vertical circuits and a perspective view of the back side of an assembly. The overall height is low enough profile for use in many current systems.
(Source: Z-Plane Inc.)

Looking to the potential of 3D with daughter cards and considering all that has transpired since the development of 3D packaging it is clear that interconnections are a rich area for exploration and new concepts.

New technologies continue to come to the forefront offering themselves as potential solutions to the ever expanding world of electronic products. One realm that offers significant promise is in chip-to-chip interconnection[ii].

In spite of the excellent performance of copper as an interconnection medium, this material is often assumed to be too slow for next generation electronics applications requiring GHz speeds In truth, copper can successfully transmit signals at near the speed of light if properly configured.

Echoing back to the discussion of backplanes and mother boards, the challenge is not so much achieving signal speed as avoiding signal degradation. Signal integrity experts have frequently pointed out over the years all of the issues and hurdles associated with present printed circuit materials, manufacturing practices and design approaches. With the understanding that the fundamental objective is to get the signal to its objective as cleanly, clearly and as fast as possible, a family of novel IC packages interconnection technology was introduced in 2003 and demonstrated 20Gbps performance[iii]. In practice, all high speed signals are launched from the surface of the chip package with I/O drivers connected directly to those signal lines though a controlled impedance cable to the surface of another chip package of similar construction (See Figure 7).

This allows signals to be transmitted directly between chips with virtually no performance sapping interruptions. Simplicity is one of the important overarching results of this approach. The method allows for a reduction in layer count in both the IC package and the substrate to which they are mounted. These proprietary copper-based interconnection solutions for high-speed electronic applications are capturing increased interest as a potential solution for high performance applications in both Asia and the west.

Current literature indicates that a number of companies are looking at such prospective solutions for solving problems on the horizon, not the least of which is energy conservation as the technology has been shown to significantly reduce power requirements for data transmission from point to point. For companies with large numbers of routers and servers, this could translate into savings of hundreds of millions of dollars annual, most of ir resulting from relatively simple changes to the IC package and its interconnection a benefit of 3D that is not always given its proper due.

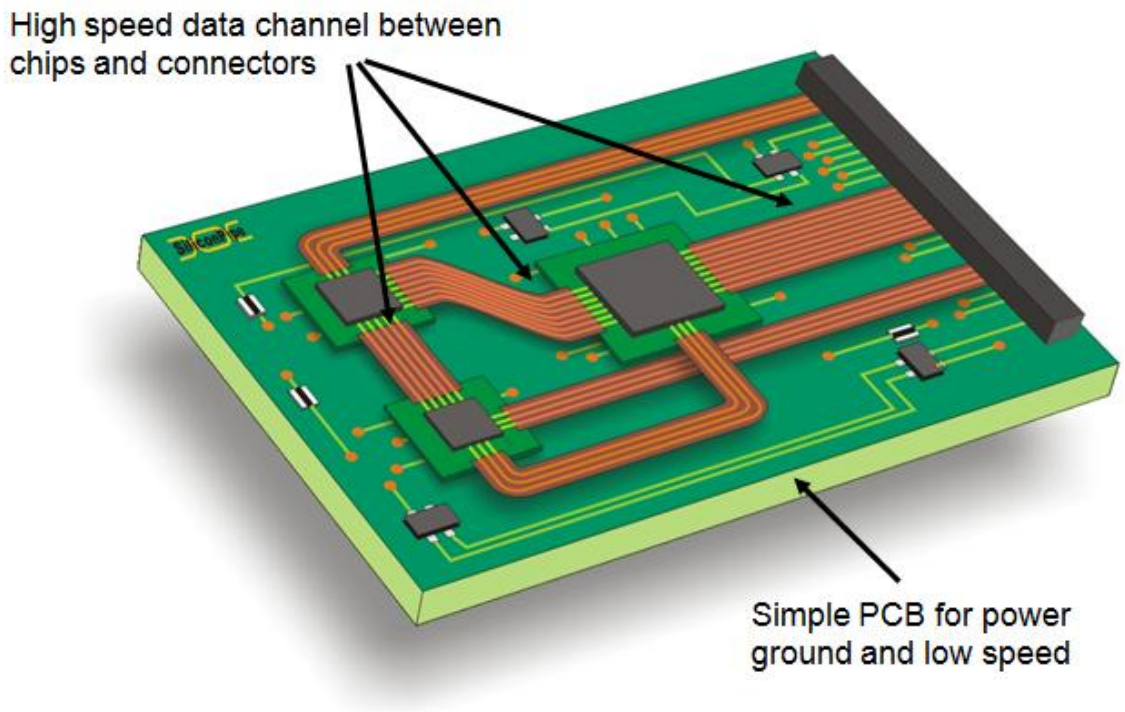


Figure 7 Making interconnections directly between IC packages has been shown to greatly improve circuit performance while simultaneously reducing system power requirements
(Source: SiliconPipe, Inc)

3D in Reverse

Constant change is a hallmark of the electronics industry, unfortunately some change is forced by legislation such as the RoHS requirements out of Europe which forces the electronics industry to use higher temperature lead-free solder and there are many problems now coming into focus. In the wake of the present challenges, there are a few movements underway to eliminate solder from the assembly process. It has been observed by reliability experts in studies from around the globe, that most of the yield loss and reliability problems facing the industry are related to solder so it removal from the process is deemed logical. In fact completely solder free assembly with circuits plated direct to component leads will reduce total manufacturing steps and thus cost but there are a host of other benefits[iv].

For example low material use and near zero waste is possible as nearly all materials used can stay with product. Elimination of solders, which now increasingly use expensive semi-precious metals such as silver, will reduce component height as the solder ball often represents up to one half of component height Moreover, lower cost materials can be used in some assemblies and copper peel strength requirements can be potentially reduced. The elimination of solder lands in design allows for improved routing and reduction in circuit layer count with associated cost and improved design security is possible with component BOM hidden from public view.

Such inverted 3D structures will allow for integral heat spreader possibilities for improved thermal management and there will be no board damage due to high temperature exposures and no high temperature damage to electronic devices or PCB (e.g. "popcorning"). In addition, no expensive or suspect finishes required or will be greatly reduced and PCB shelf life issues are avoided and no spares required because the circuits are produced in situ. The structures can be all copper requiring no RoHS restricted material and solderability testing requirements are eliminated from specifications. Overall manufacturing energy requirements are reduced with no pre-bakes or high temperature reflow required and by passing solder related defects including excessive copper dissolution which has become a recent concern. There is also no post assembly cleaning concern which is a significant challenge for fine pitch devices and less testing is needed.

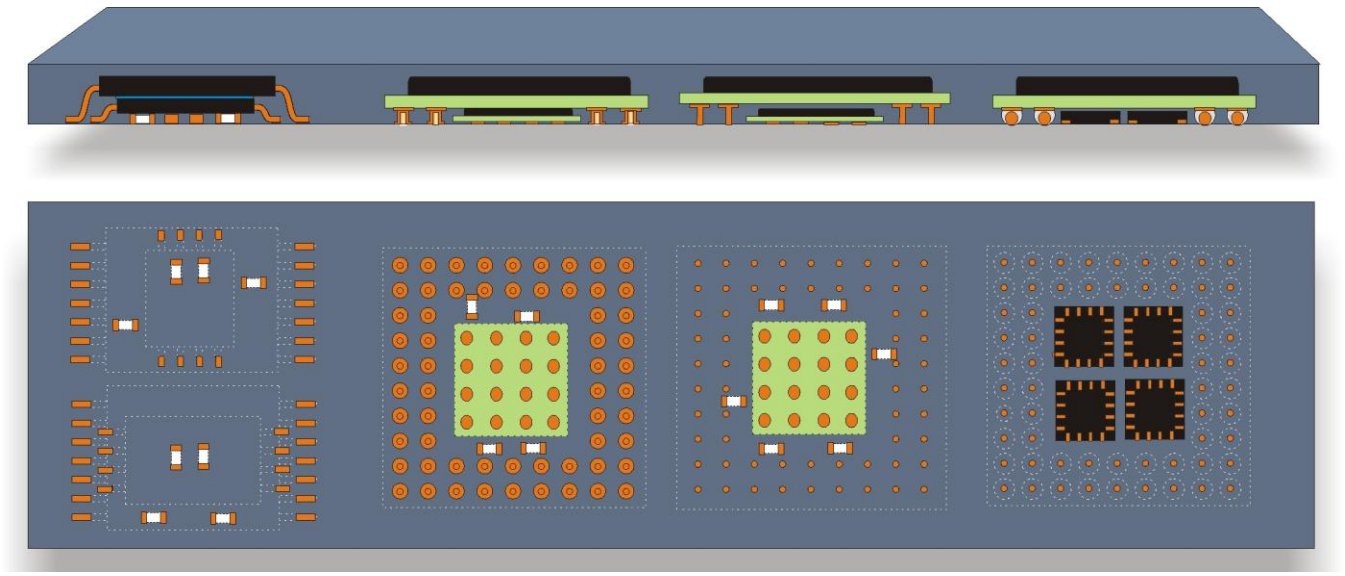


Figure 8 Overlapping of packages and discretes is another prospective 3D solution which could be employed. Such devices could be either surface mounted as a component or embedded in an inverted or reverse 3D structure. (Source: Verdant Electronics, Inc)

The method also allows for components can be overlapped (e.g., package over package as opposed to package on package) as shown above in Figure 8. Moreover, because the packages are embedded, the components are virtually immune to shock and vibration, which according to a relatively recent report by Davide de Maio of National Physical Laboratory in England, indications are that 80% of failures in lead-free soldering are related to shock and vibration[v]. In addition, when using a reverse 3D method, the completed assembly can be jacketed with metal to create a near hermetic assembly and that same metal jacket can provide complete EMI immunity for assembly. In anticipation of optical interconnections of the future, assemblies are amenable to adaptation to optoelectronic component integration and inclusion of optical channels on surfaces. Finally assemblies can be joined in 3D fashion creating true "Manhattan" routing of signals, up, down and laterally. (Figure 9 shows an example) Investigation and development of the technology is underway in several locations around the globe and published results are expected in the coming year.

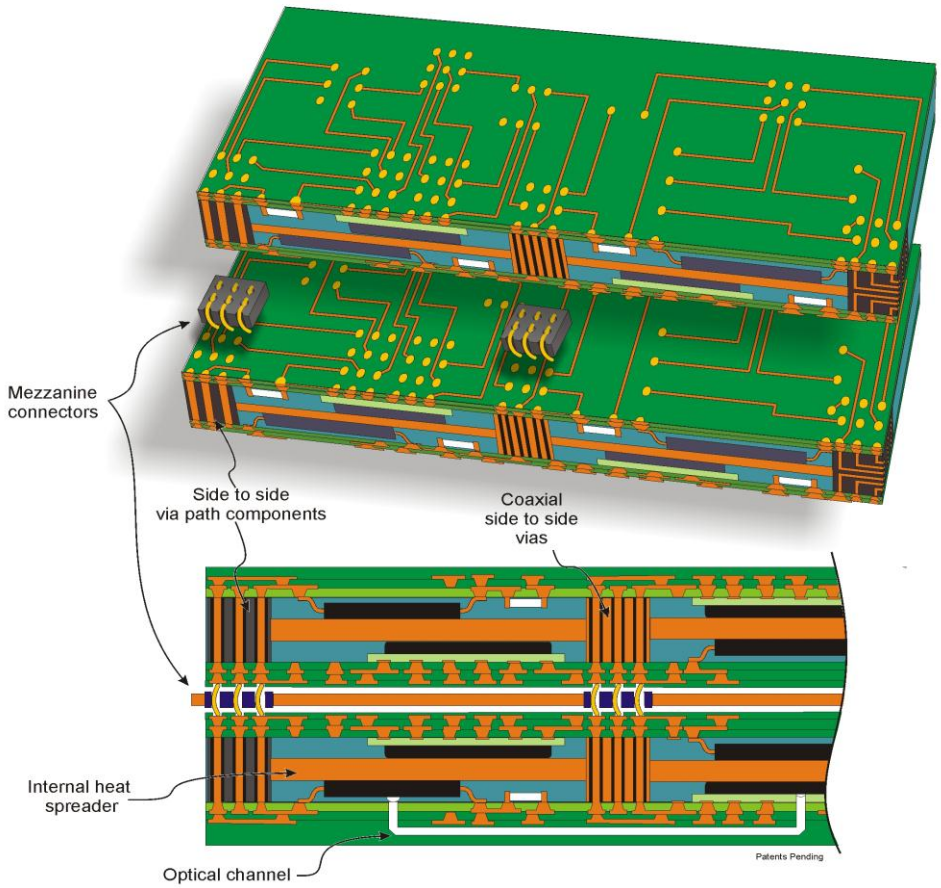


Figure 9 Solderless assembly of electronics, an "inverted" 3D process is an area of growing interest due to the many advantages that it prospectively presents including optical channels built into the assembly. The assemblies can be joined together in a 3D stacked manner to provide true Manhattan, shortest path routing and the potential to address thermal issues on the front rather than the back end of the design process.
(Source: Verdant Electronics)

Summary

In spite of the apparent novelty of 3D packaging and interconnection solutions, it should be evident that 3D solutions have deep roots in the electronics industry and this paper has hopefully provided sufficient examples to make the case. There are of course many other 3D solutions such as flex circuits and cables which further and extend the cause. It is anticipated given the examples provided that the future will see an increasing number of designers and system developers taking advantage of all the benefits that the Z axis of Cartesian space has to offer for cost, performance and convenience.

References

[i] National Museum of American History's Chip Collection Website—The Texas Instruments Collection http://smithsonianchips.si.edu/index2.htm

[ii] Fjelstad, J, Yasumura, G and Grundy, K., "3-D Partitioning of Printed Circuit Design – '*Elevated Highway Bypass*' Packaging Design, *Advanced Packaging* February 2005 pp: 12-19

[iii] Grundy, K. et al., "Designing Scalable 10G Backplane Interconnect Systems Utilizing Advanced Verification Methodologies" Proceedings *DesignCon*, February 2006

[iv] http://www.verdantelectronics.com/process.php

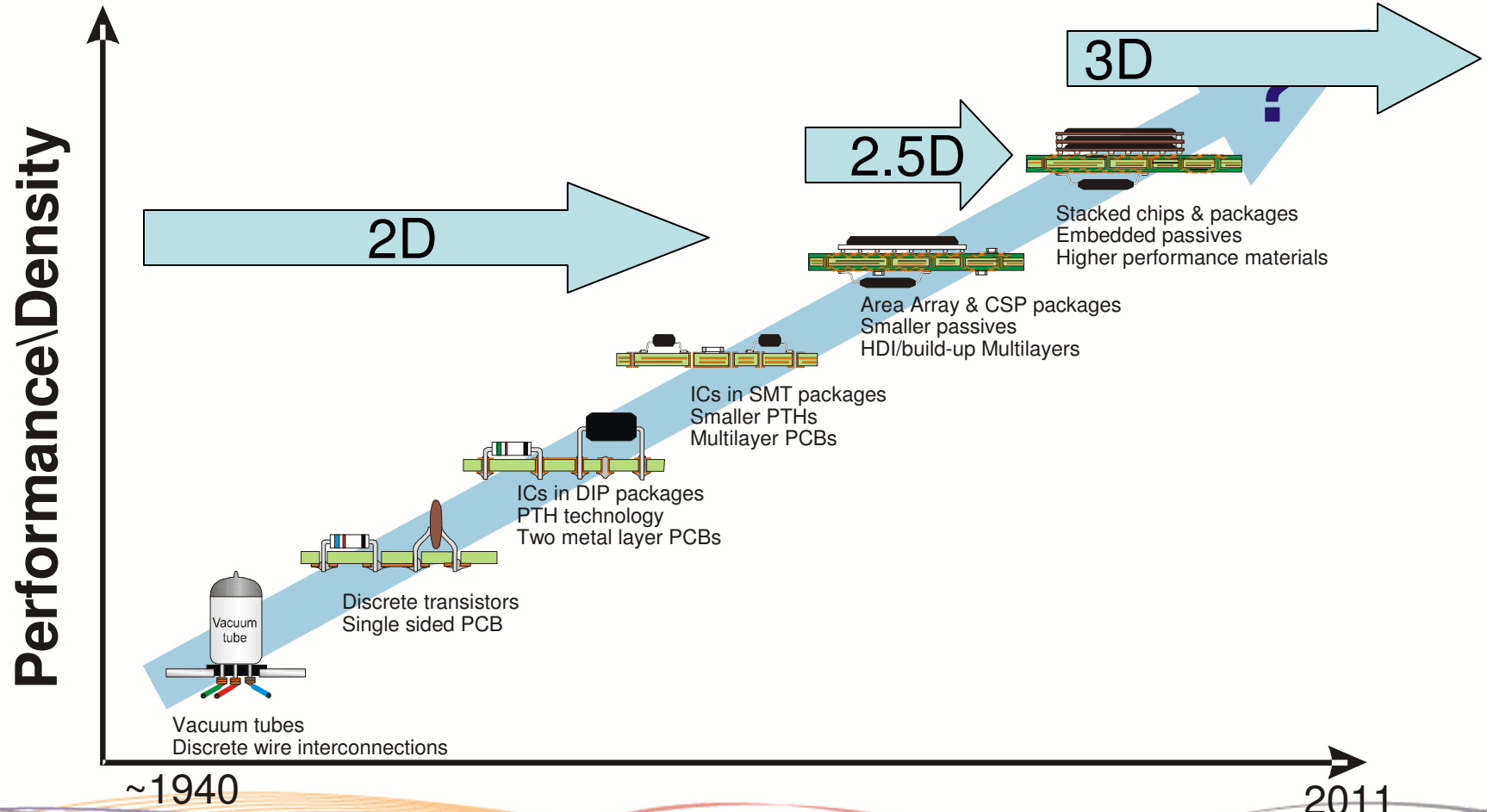
[v] de Maio, D. **"**High-frequency vibration tests of Sn-Pb & lead-free solder joints" Proceedings *IEMRC/TWI Technical Seminar: Developments in Interconnection, Assembly and Packaging*, December 2008

3D Interconnection Technologies for Electronic Products:

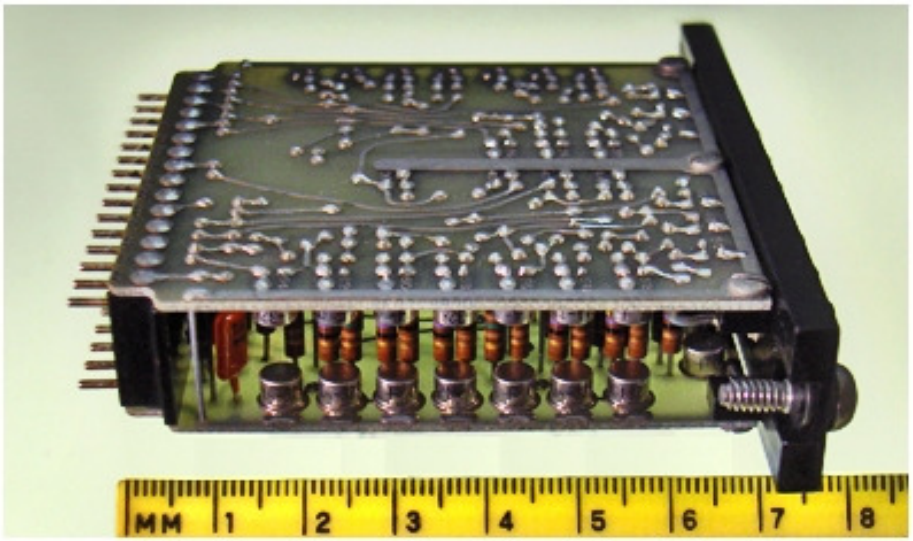
A Perspective View of Electronic Interconnection Technologies from Chip to System

Joseph Fjelstad
Verdant Electronics
Cupertino, CA

The Evolution of Electronic Assembly



Is 3D Interconnection New?



A “cordwood” module built by Control Data Corporation was developed to minimize connecting wire lengths and used a 3D stacked printed circuit arrangement to make electrical interconnections.

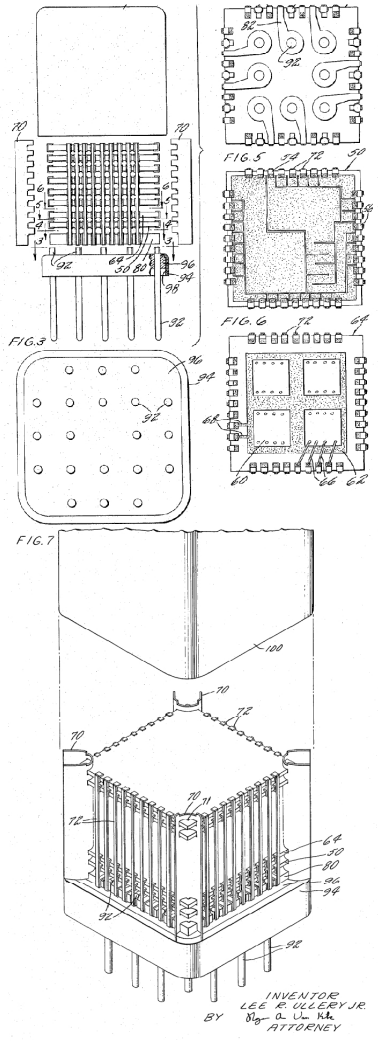
(Source: Computer History Museum)

(Source: Wikipedia)

3D through the years…

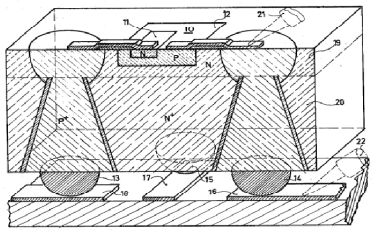
Invented ~1963

US Pat No. 3,243,661



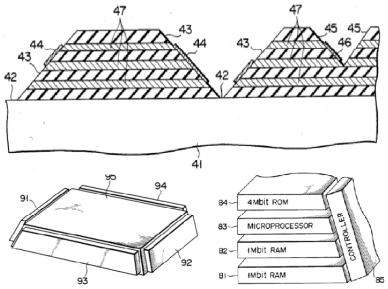
Invented ~1971

US Pat No. 3,787,252



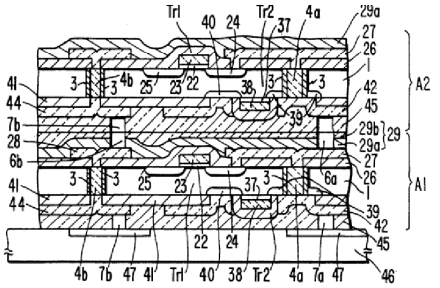
Invented ~1981

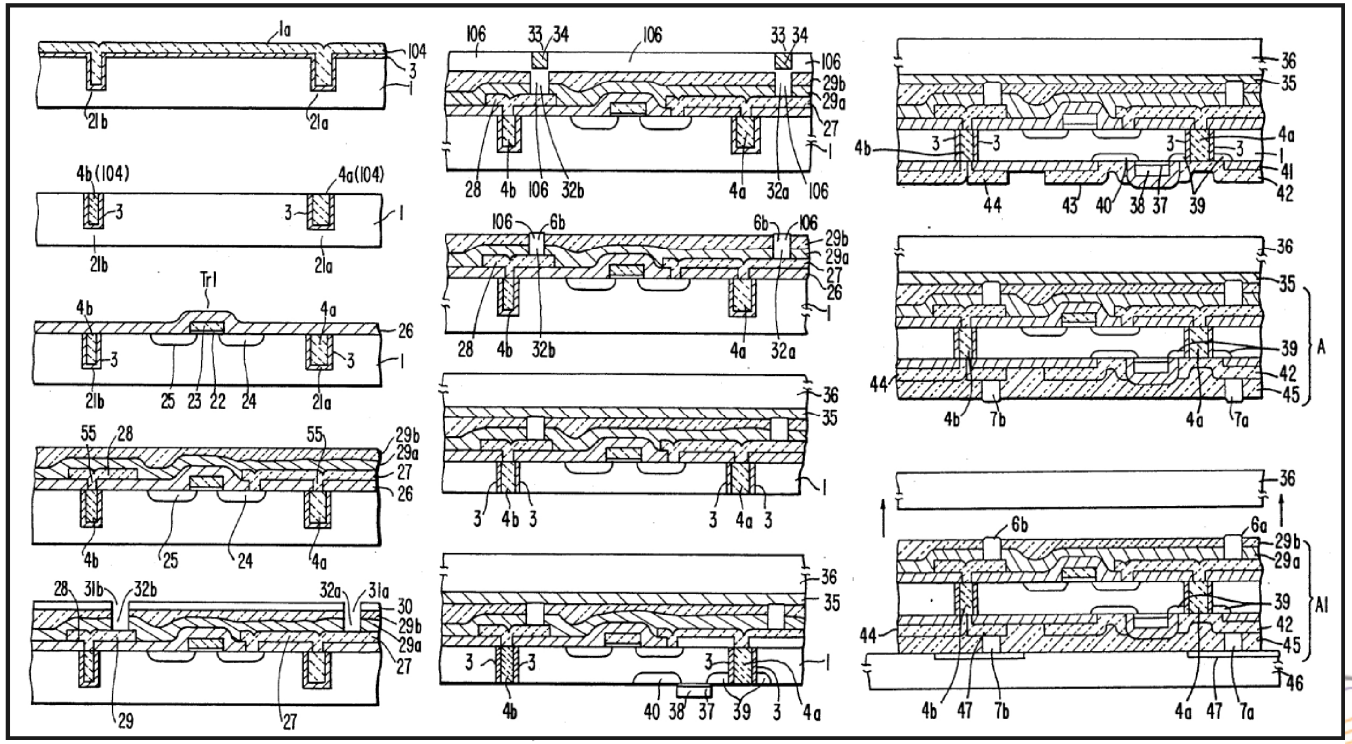
US Pat No. 4,500,905



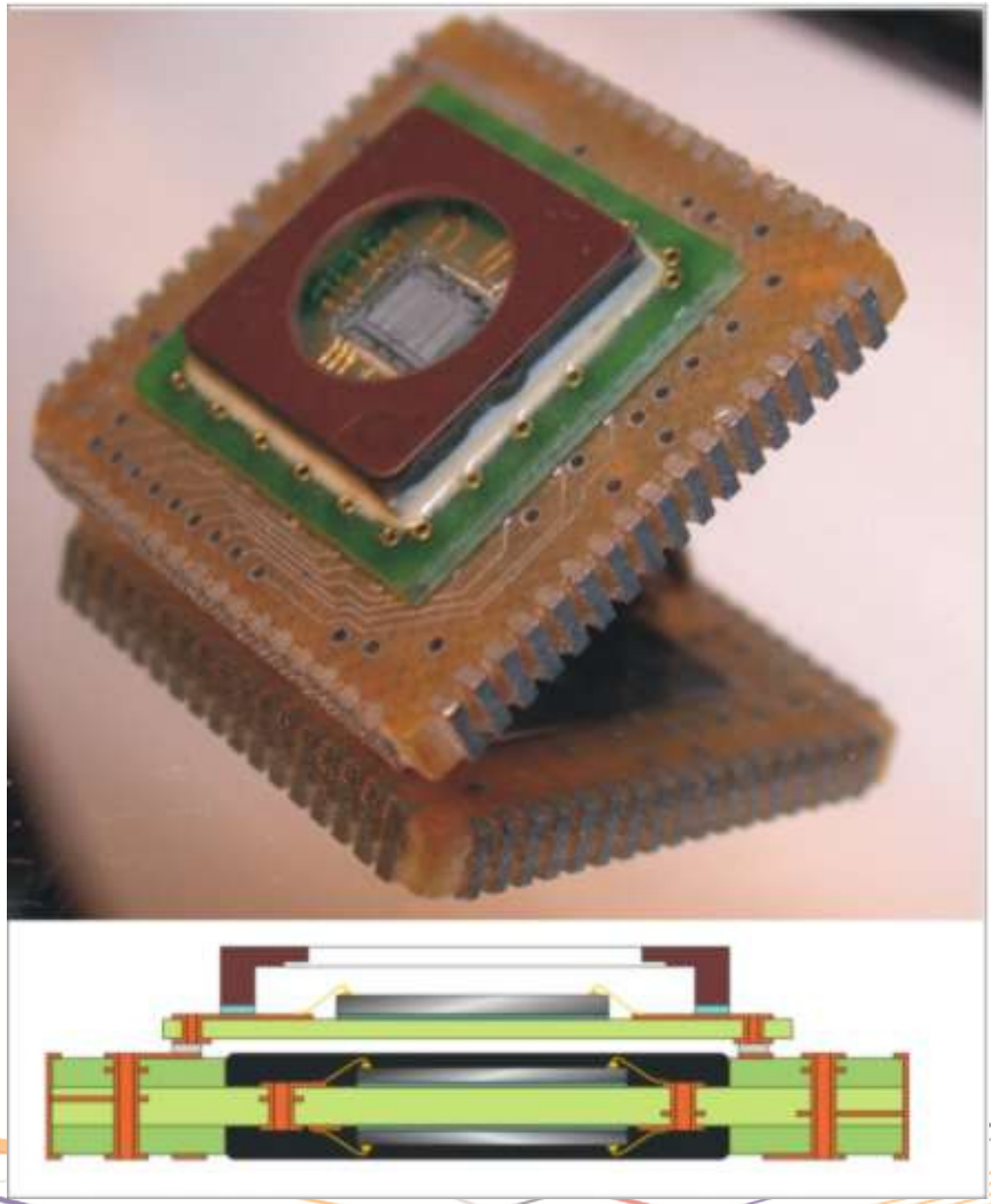
Invented ~1986

US Pat No. 4.939,568





Example of stacked chip packaging assembly from the mid 1980s



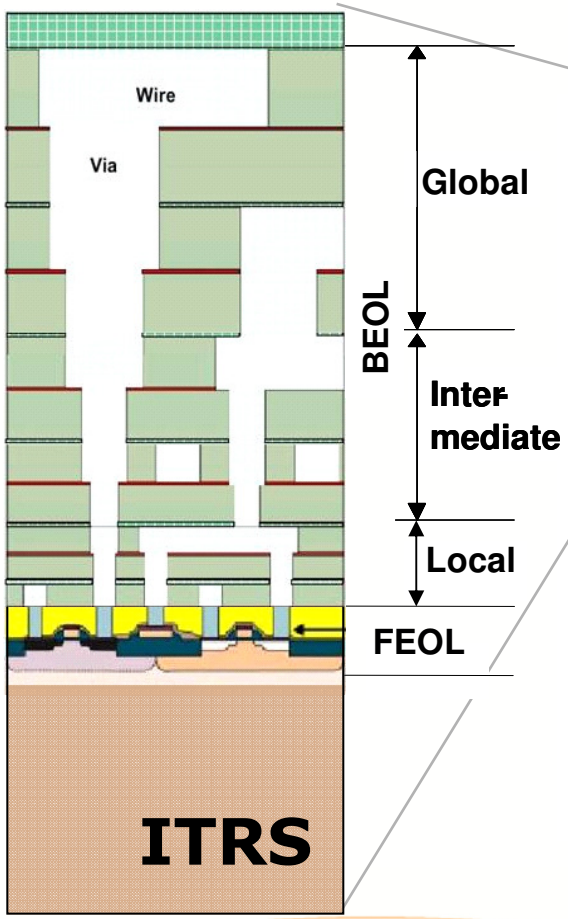
Traditional Interconnection Hierarchy

- **Electronic systems are organized in a hierarchical way :**
  - Electronic components, sub-circuits, circuits,…
  - At the lowest interconnect levels there is the largest number of interconnects and the smallest dimensions and the shortest lengths.
  - At higher interconnect levels there are less interconnects with larger dimensions and longer lengths
- **Interconnects within a level are essentially routed in a 2D-fashion:**
  - This is because of manufacturing and design efficiencies related to lithography and general circuit “printing” methods
  - Yet even ‘folded’ or flexible circuits are electrically 2D interconnects

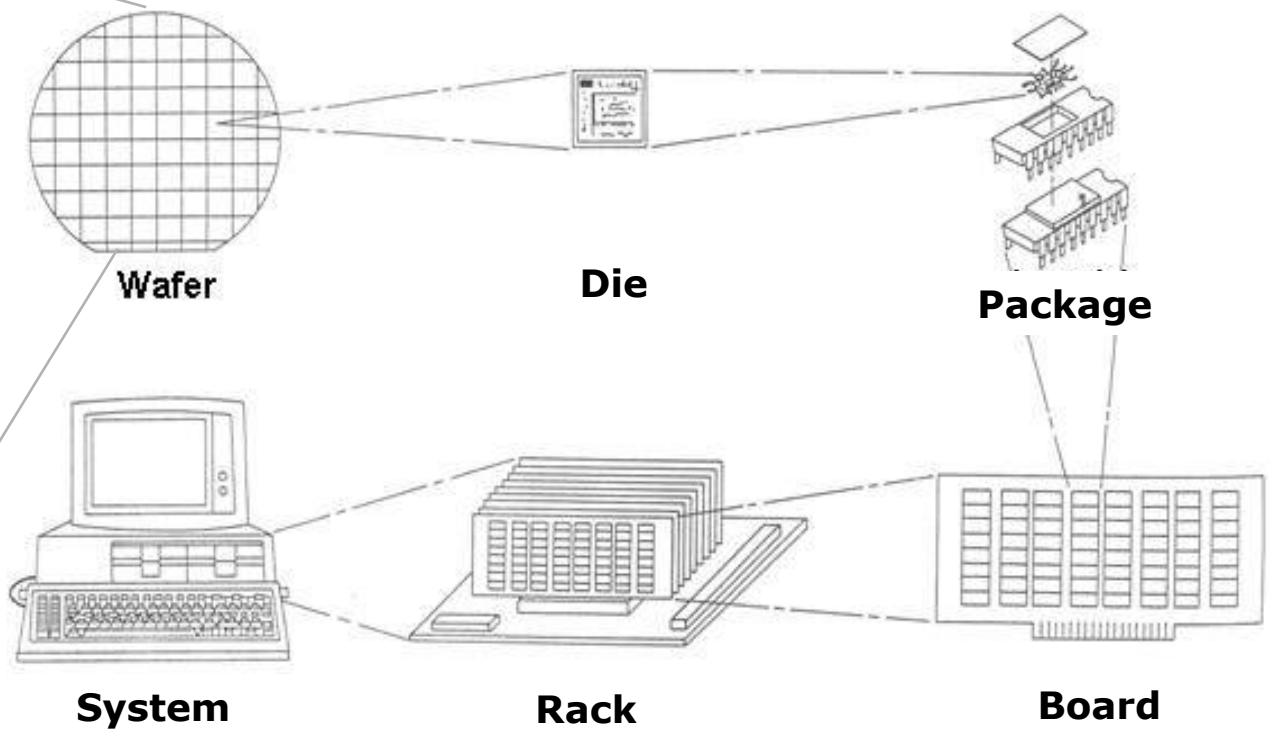
Source: E.Beyne IMEC.

Traditional Interconnect Hierarchy

On-chip
Wiring Hierarchy

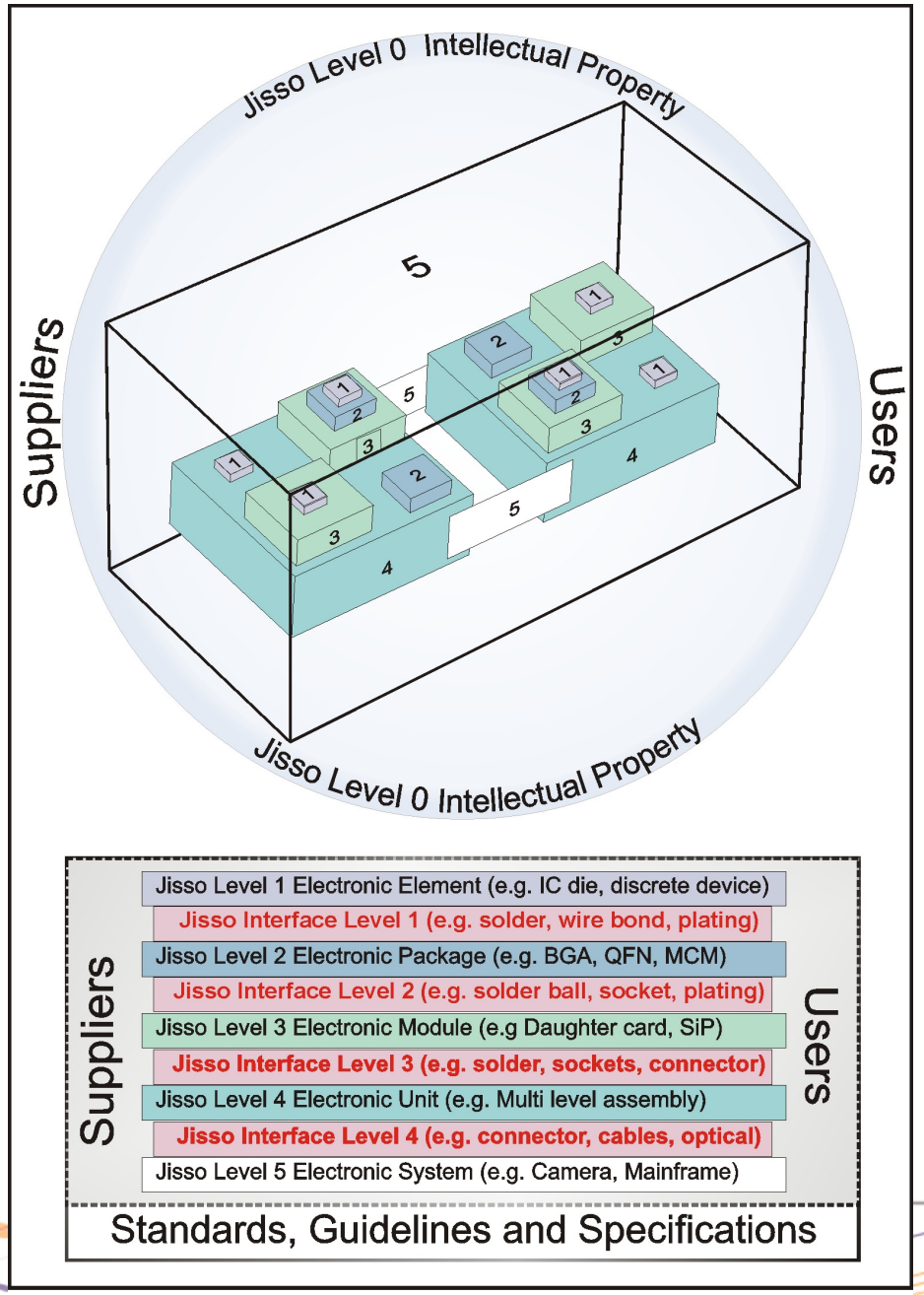


System-level wiring hierarchy
Traditional view

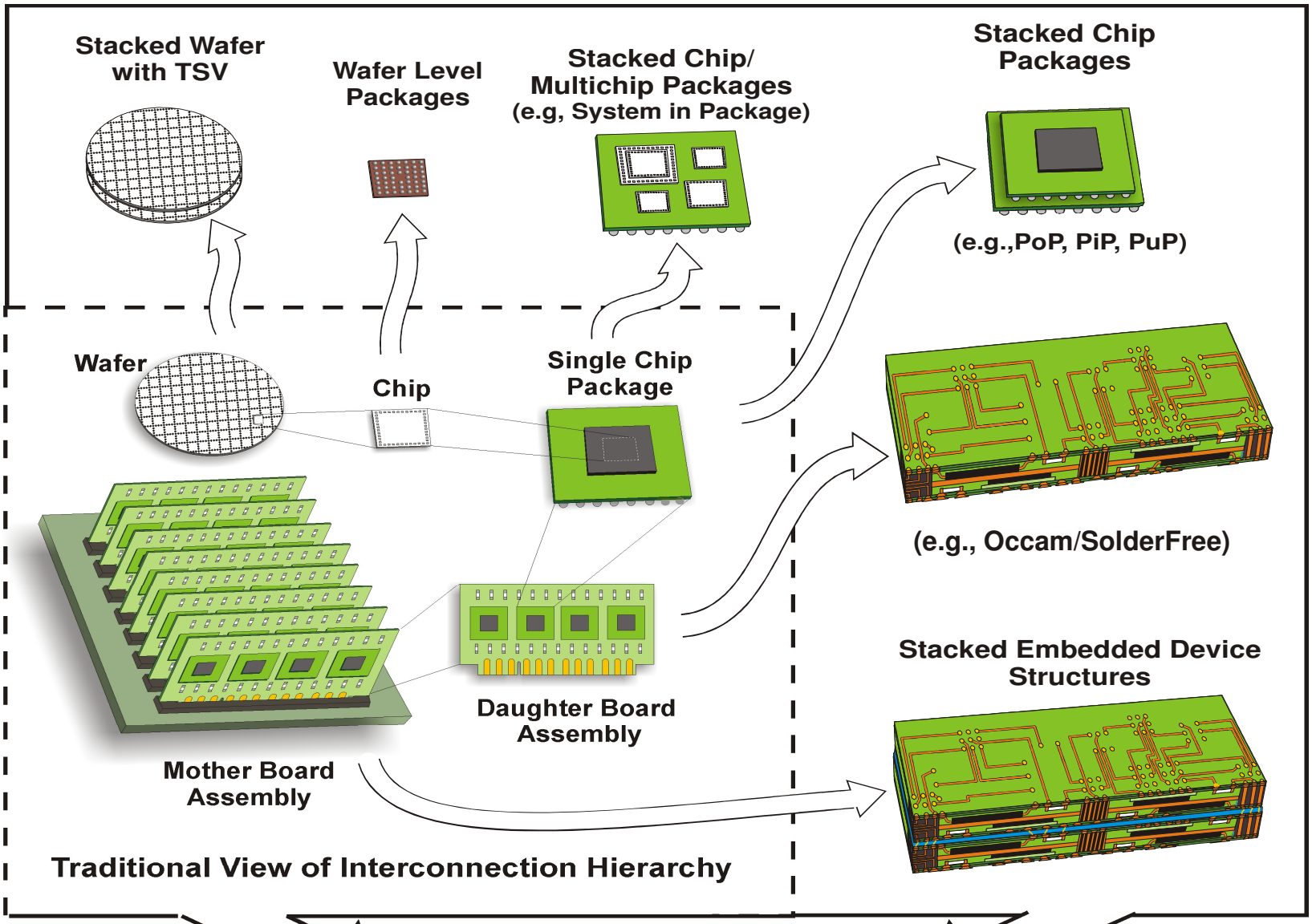


Source: E.Beyne IMEC.

Jisso Concept and Hierarchy



Evolving Interconnection Levels



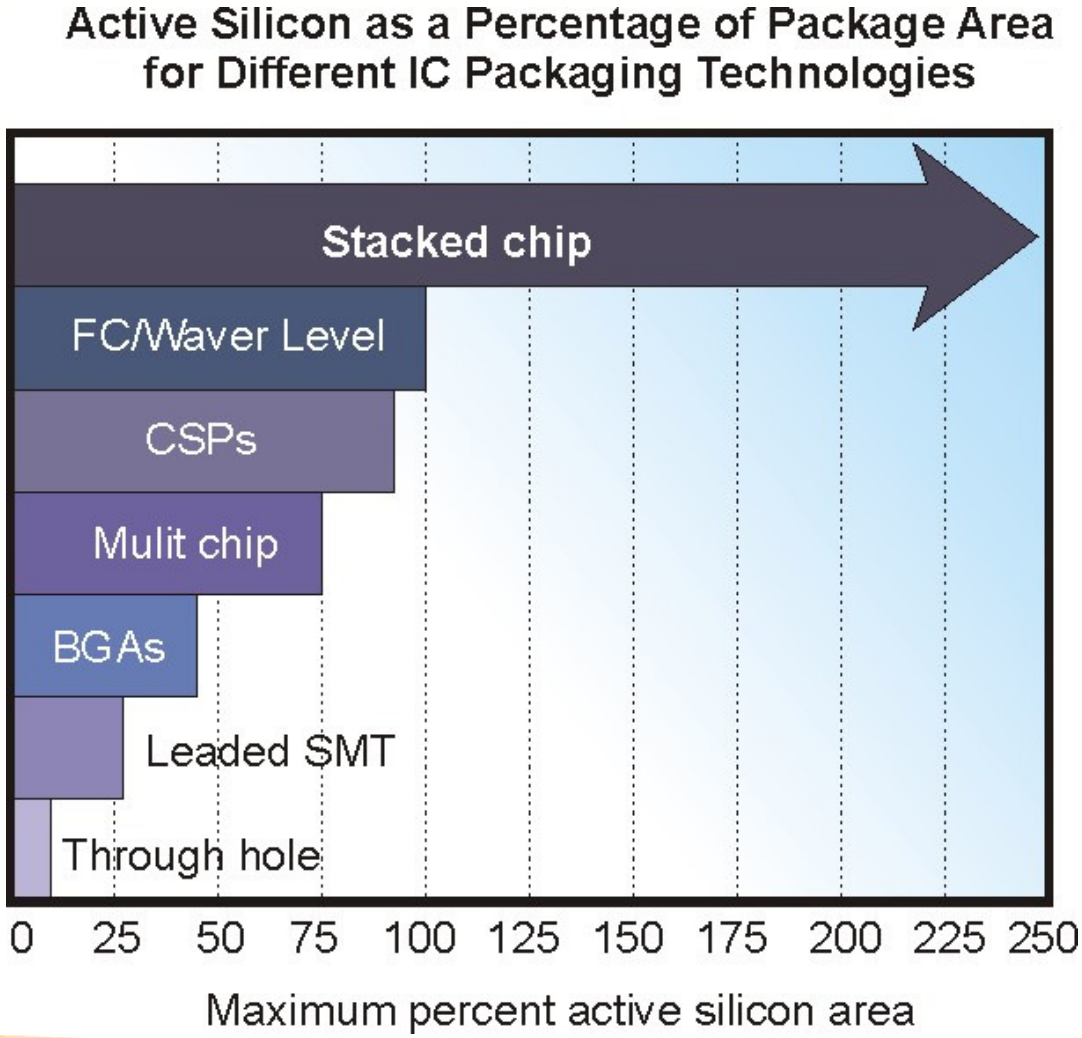
3D Interconnection Technologies:

- Stacked chips…
- Stacked packages…
- Stacked wafers…

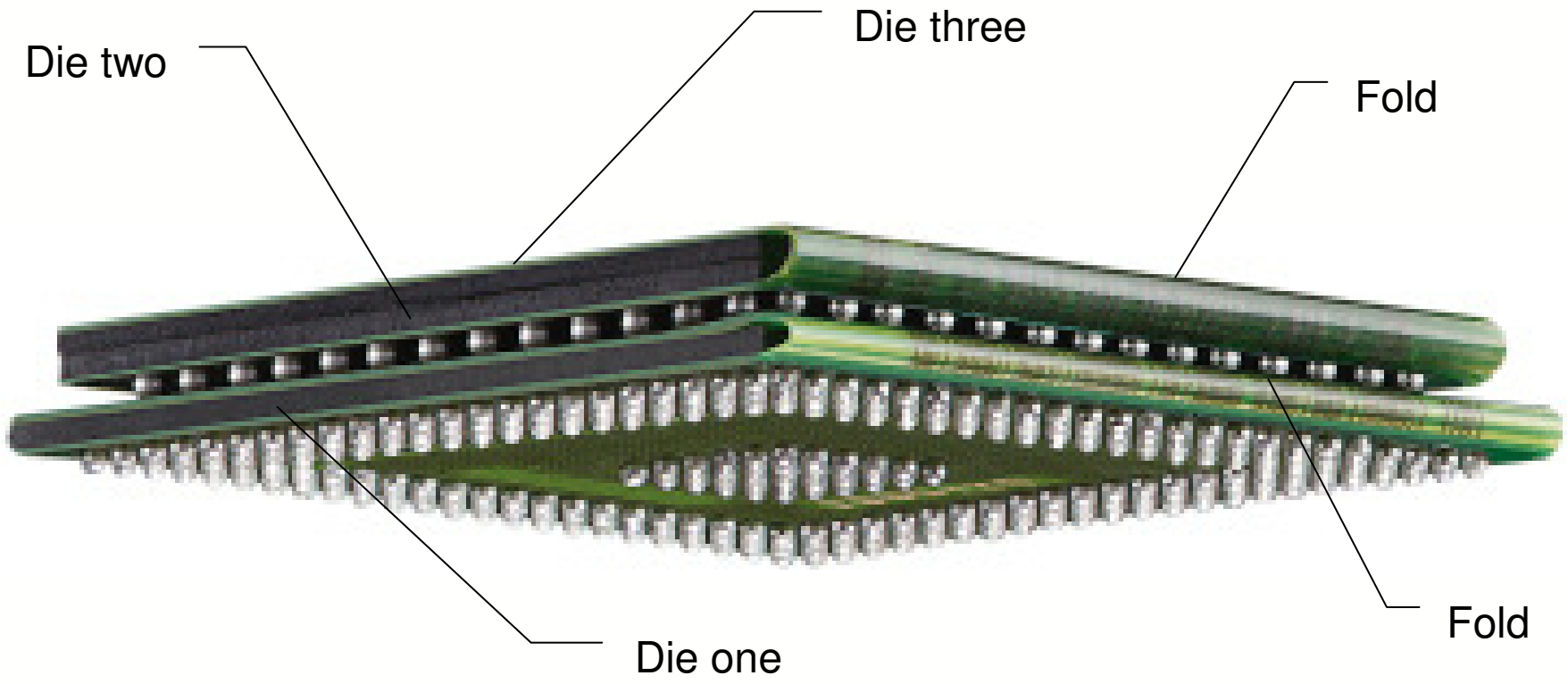
3D… For Better or Worse?

- **Benefits**
  - Greater function in smaller package
  - Mixed technology solution
  - Greater versatility
  - Can use lower power
  - Potential to design simpler better performing systems
- **Concerns**
  - Known good die imperative - is it possible?
  - Mechanical stresses need to be considered
  - Stacking die increases thermal density
  - Transistors will wear out sooner shortening product lifetime

3D Stacking Advantage



Stacked Fold Over

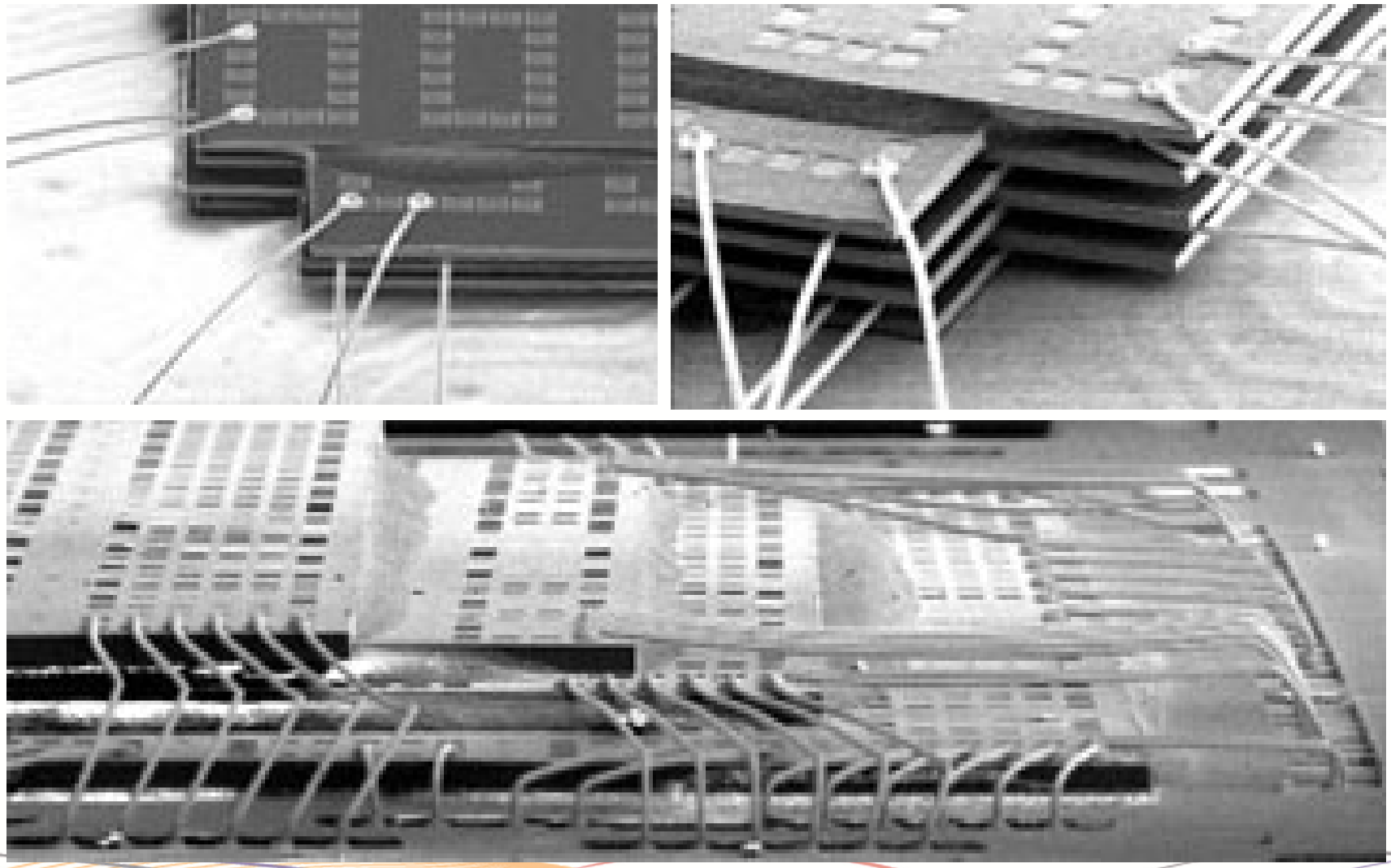


Source Intel

Stacked Chip Packages

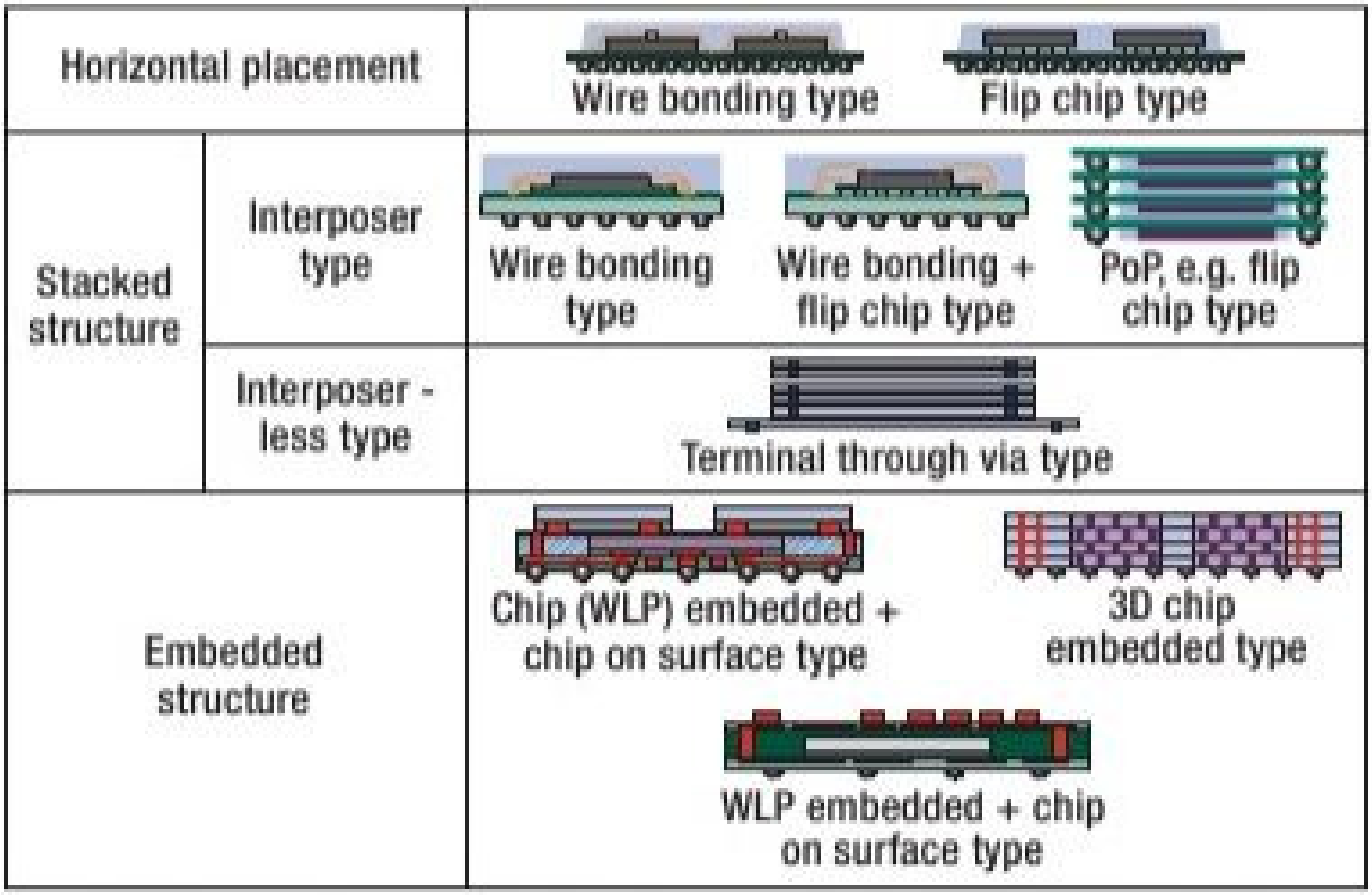
- Higher density packaging scheme
  - Helps reduce size
  - Reduced I/O at board level
  - Used to create system in a package
    - Classic example: Hearing aids have been packaged with IC dice in stacked form in 1980's
  - Current uses, Flash/SRAM, DSP/Flash, others

Stacked Chip Structures



Source: Intel

3D Packaging Variations

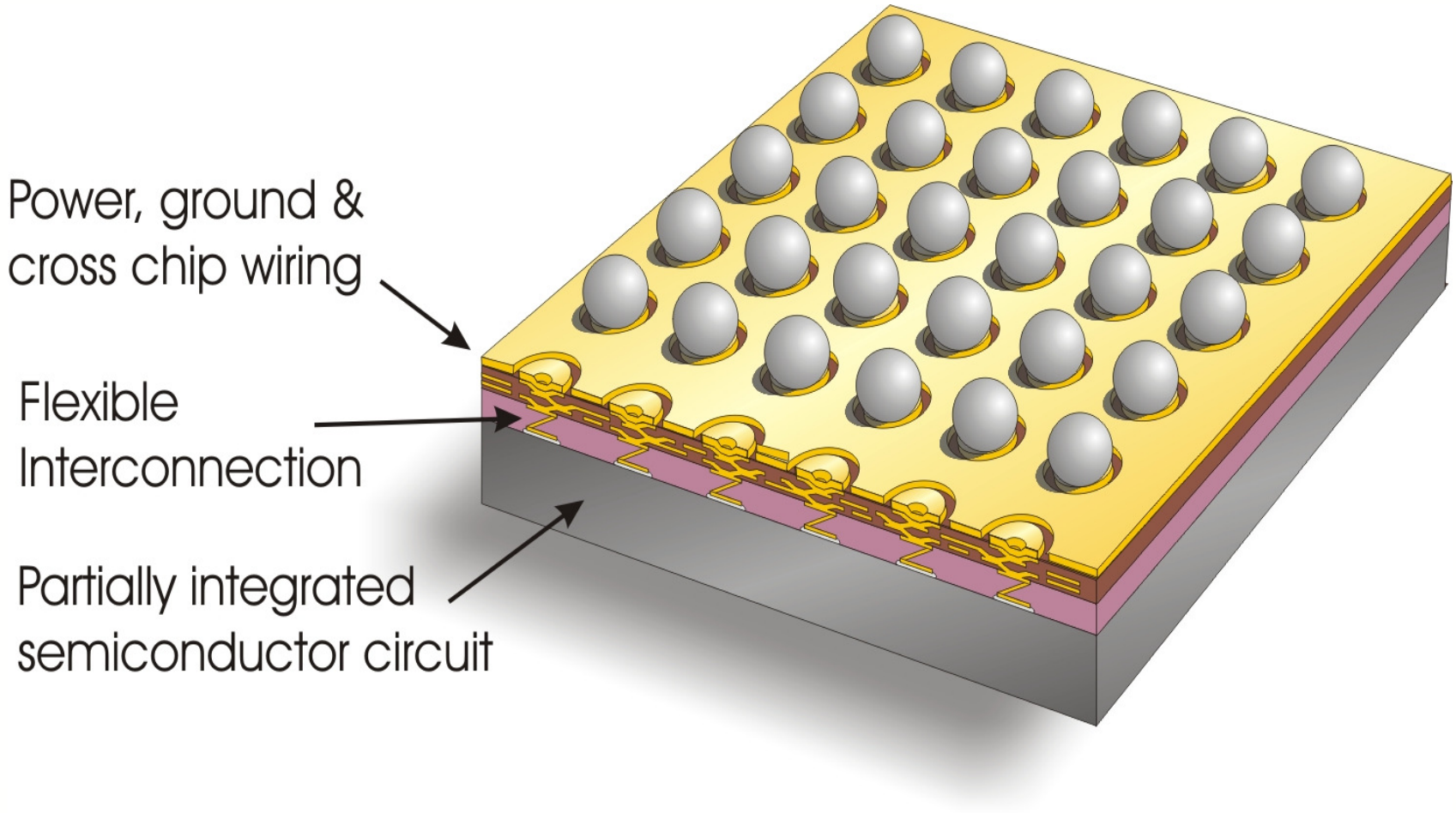


Multi-Die 3D Package Challenge

Multiple die packages must address key logistics issues:

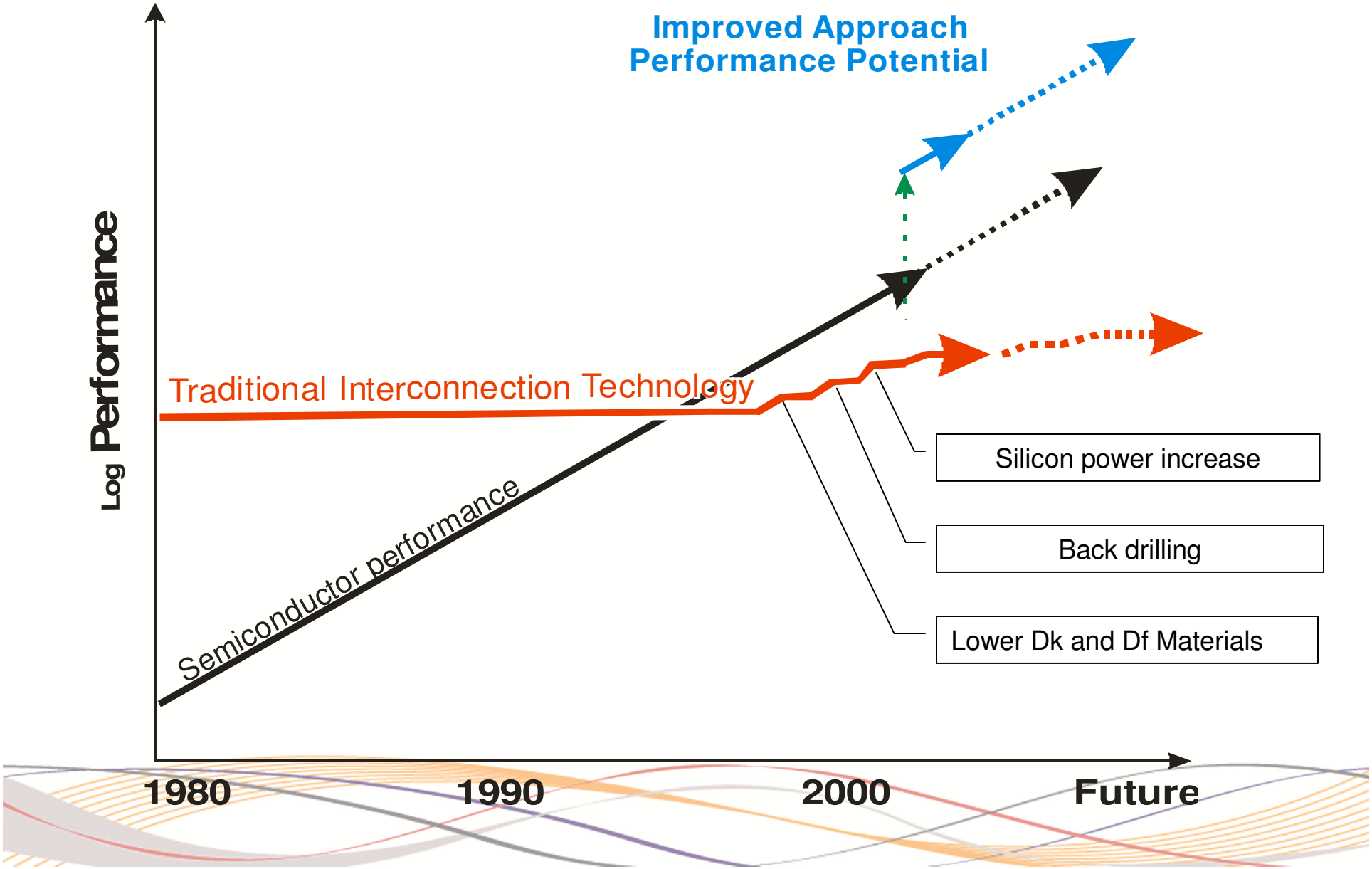
- ✓ Accommodate incompatible die shrinks
- ✓ Simplify management of multiple IC vendors
- ✓ Enable package level test and burn-in
- ✓ Allow the combining of high and low yield devices
- ✓ Contribute to product quality and reliability
- ✓ Maximize configuration flexibility
- ✓ Minimize time to market and risk

The Fusion of Silicon and Package

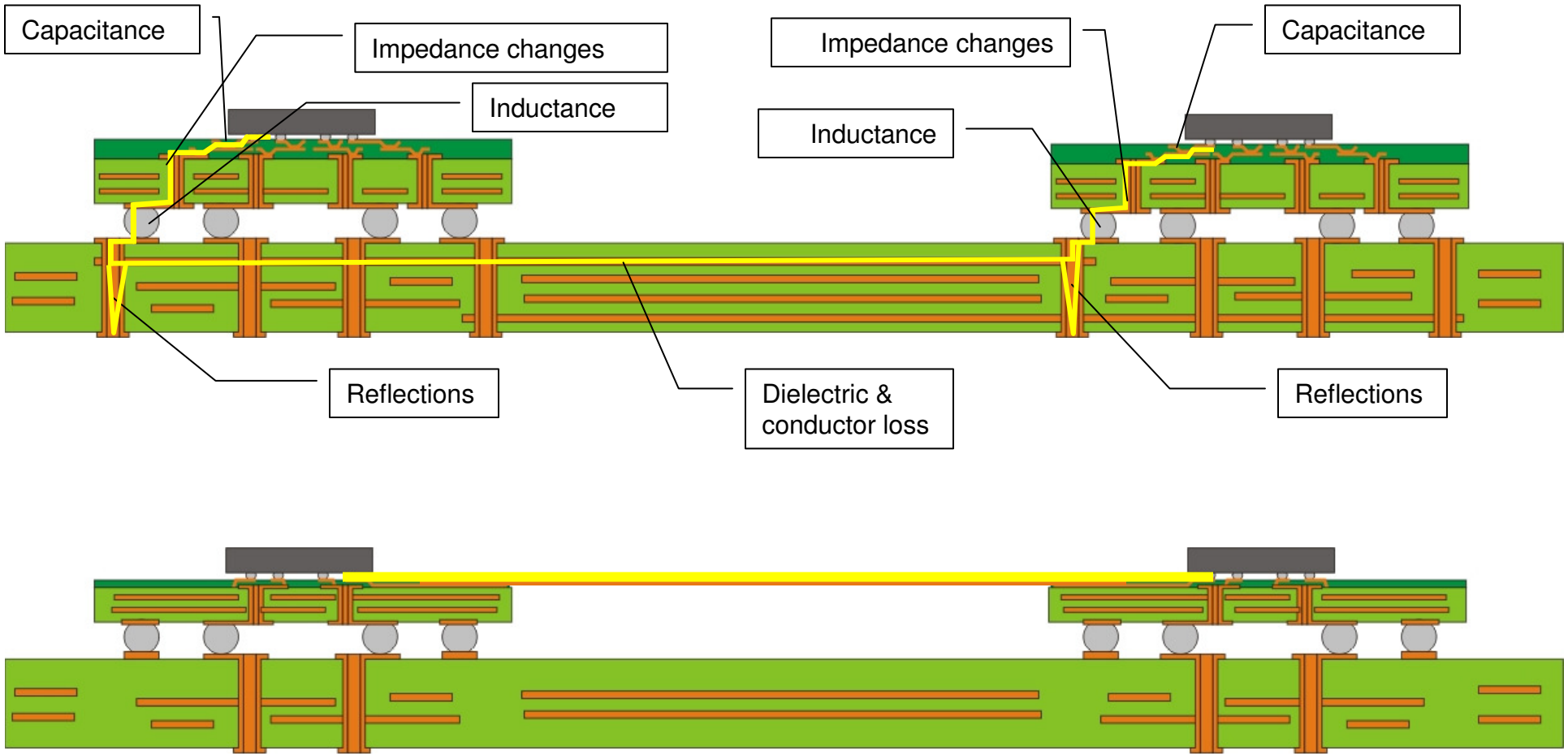


Prospective 3D Interconnection Solutions

Jumping the Interconnect Gap

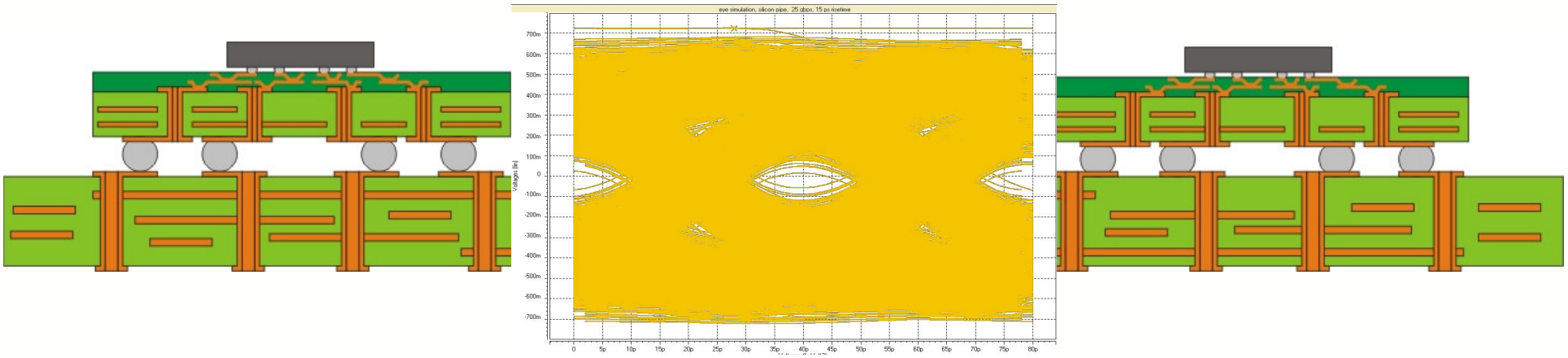


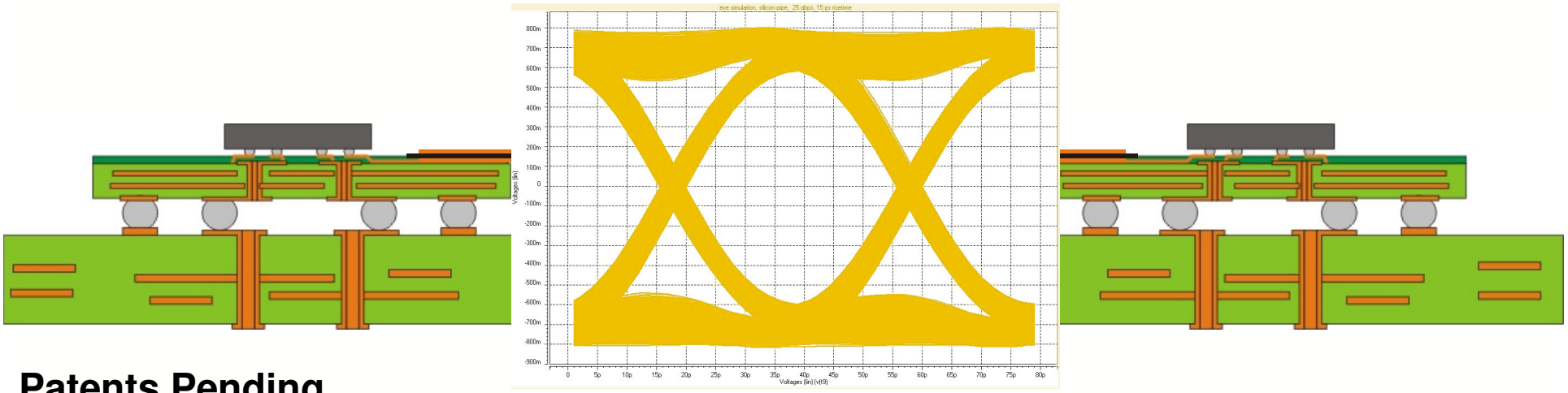
Redefining the Channel



Patents Pending

Eye Diagram Comparison





Patents Pending

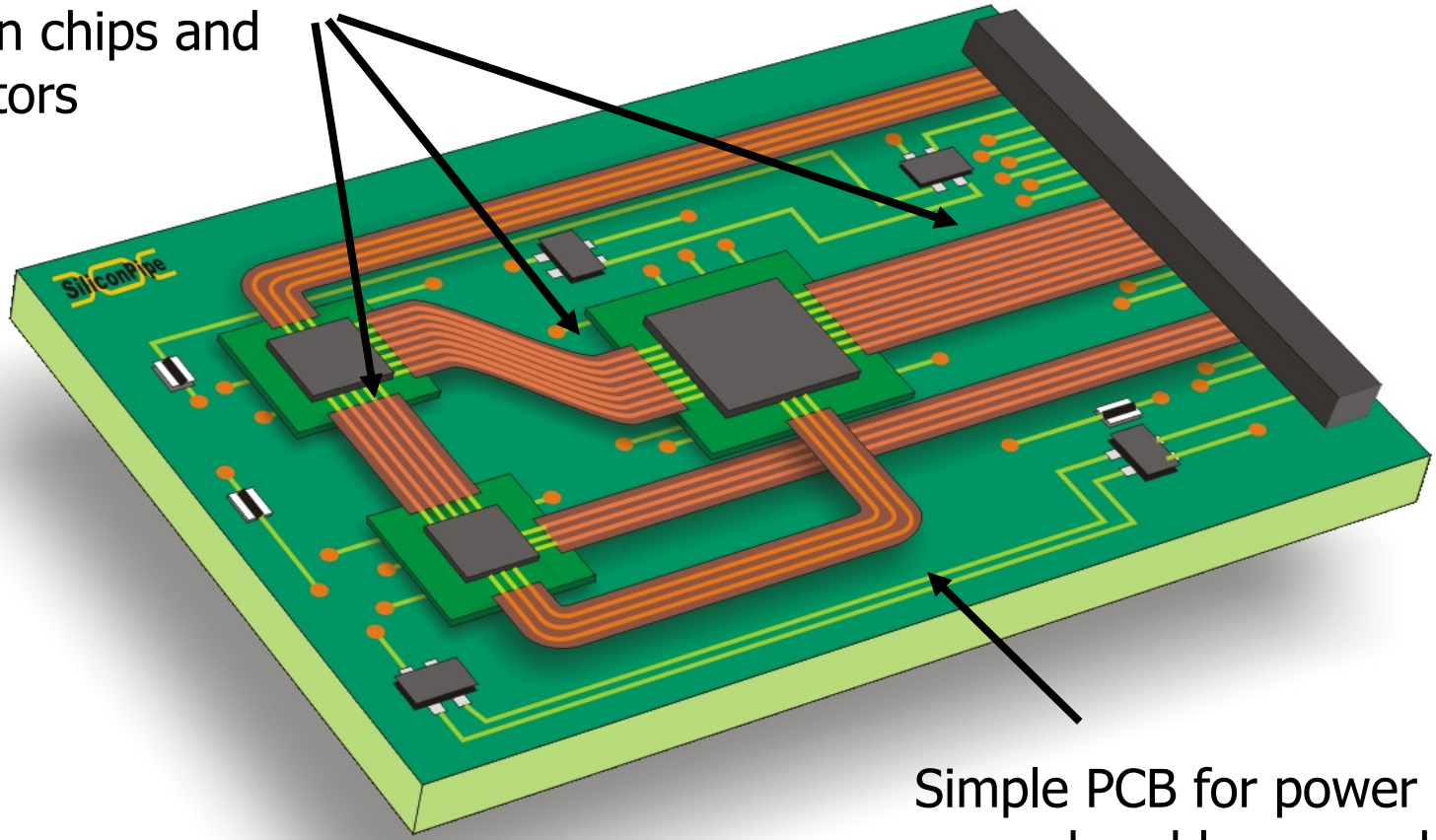
20Gbps High Speed Copper Channel

Technological Advantages...

- High speed flex based channel technology is simple
- Low power, non-enhanced, link between packages can be made over extended distance, with near zero skew at speeds to >20Gbps per channel.
- Interconnection architecture can be standardized
- Applicable to various die sizes and performances
- Increased design flexibility and customization for performance
- Full compatibility with existing packaging assembly
- Chip interconnections are standard in the package assembly can built as a commodity item using all standard materials

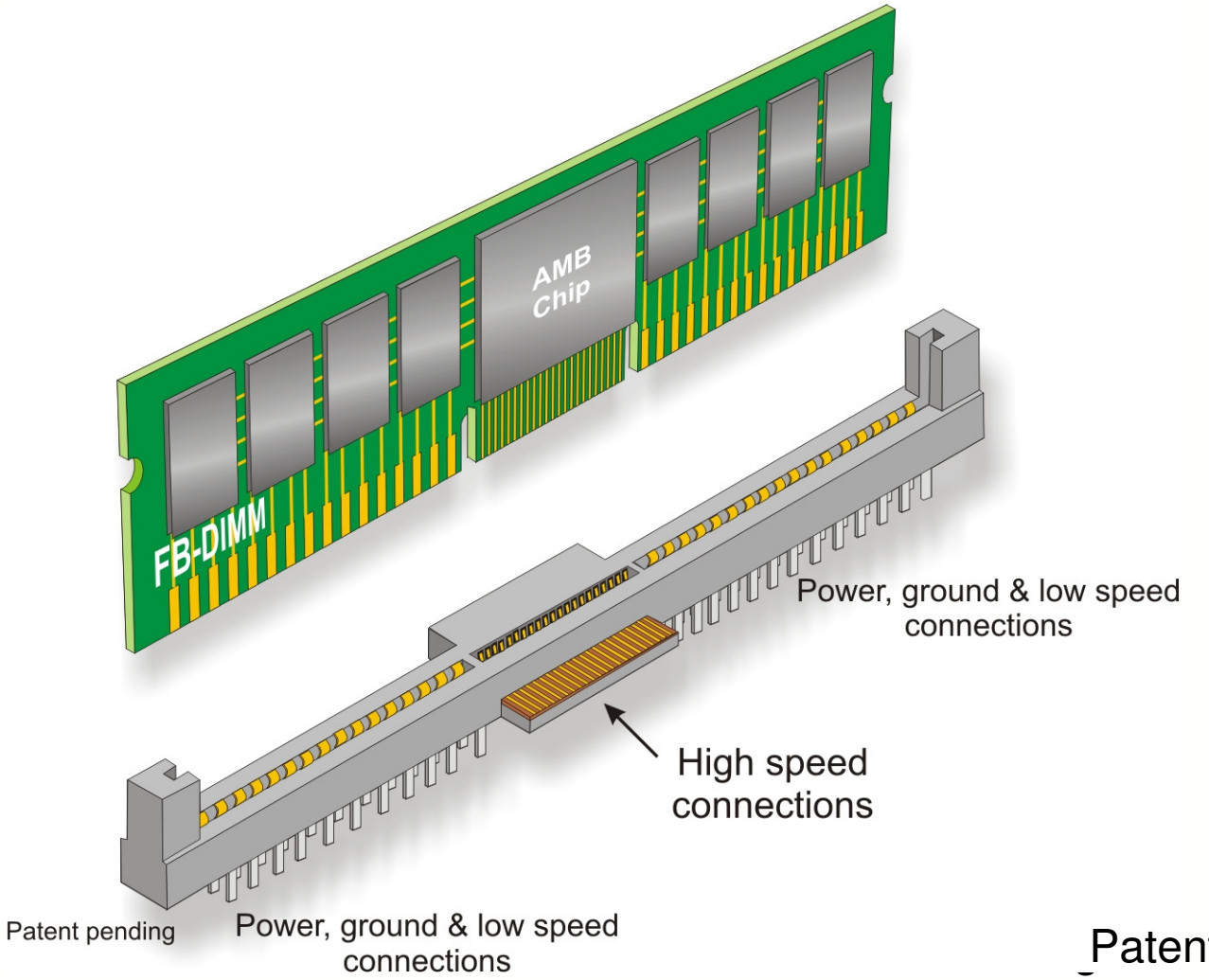
Rethinking Circuit Design in 3D

High speed data channel between chips and connectors



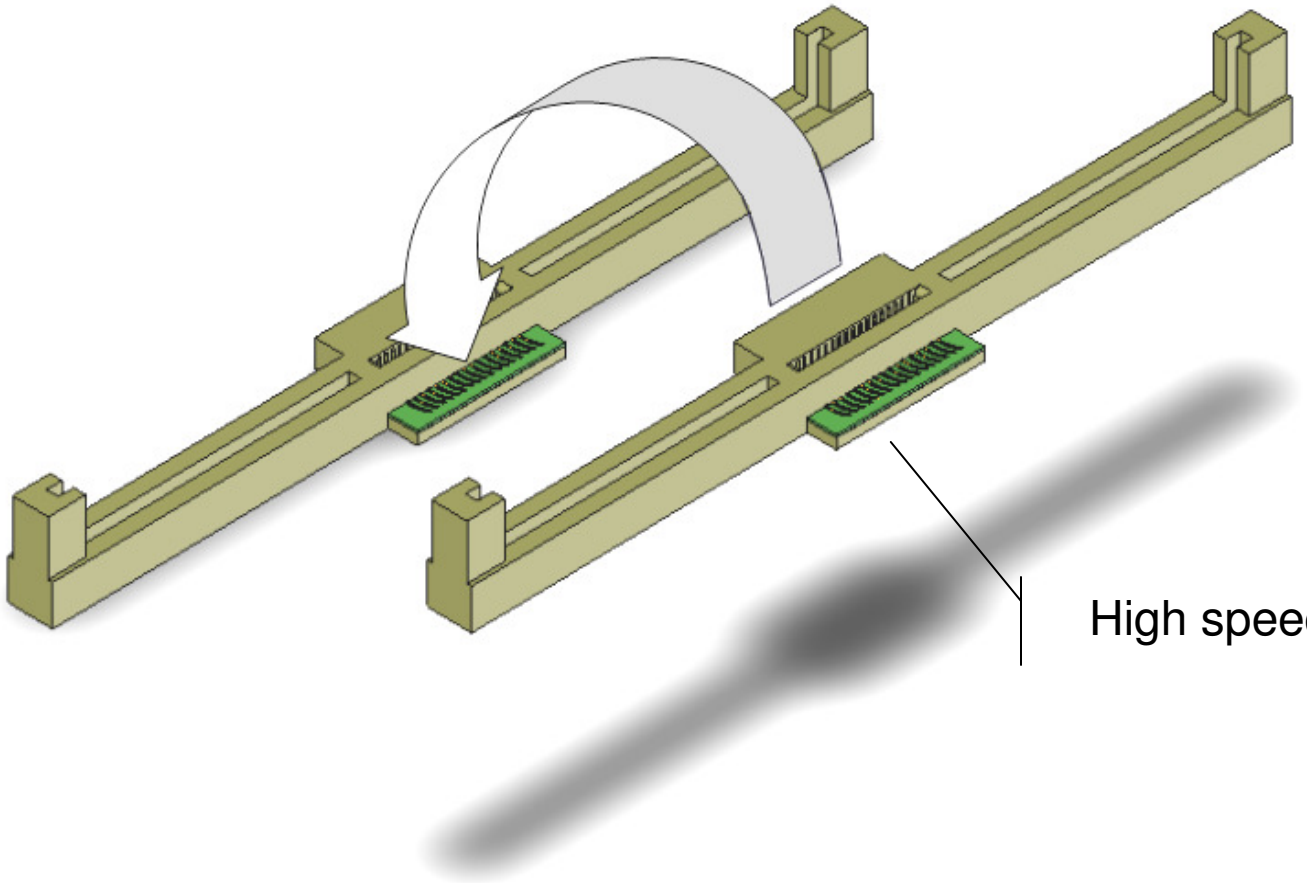
Patented

Application – FB-DIMM



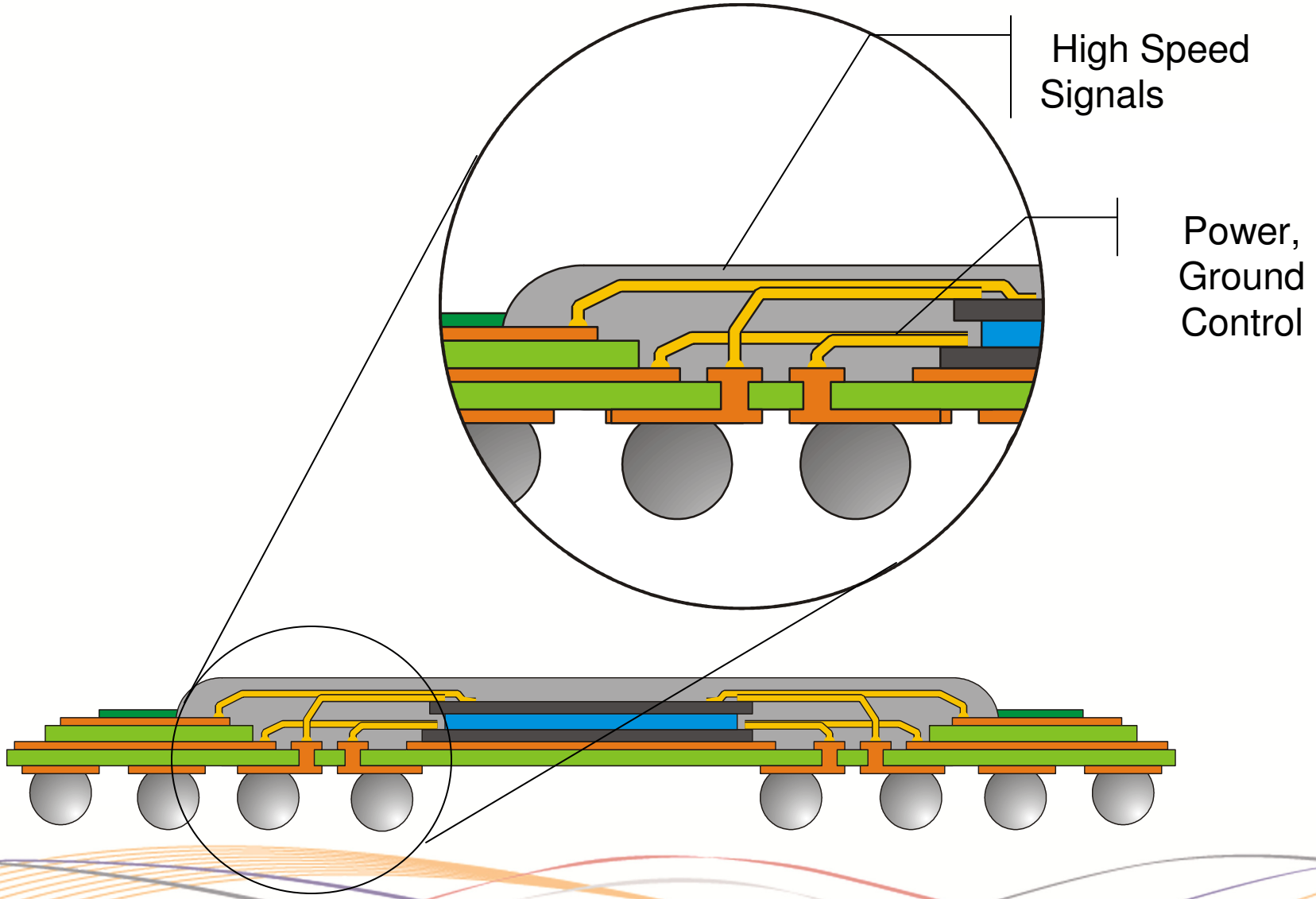
Patented

Connector to Connector Speed Link

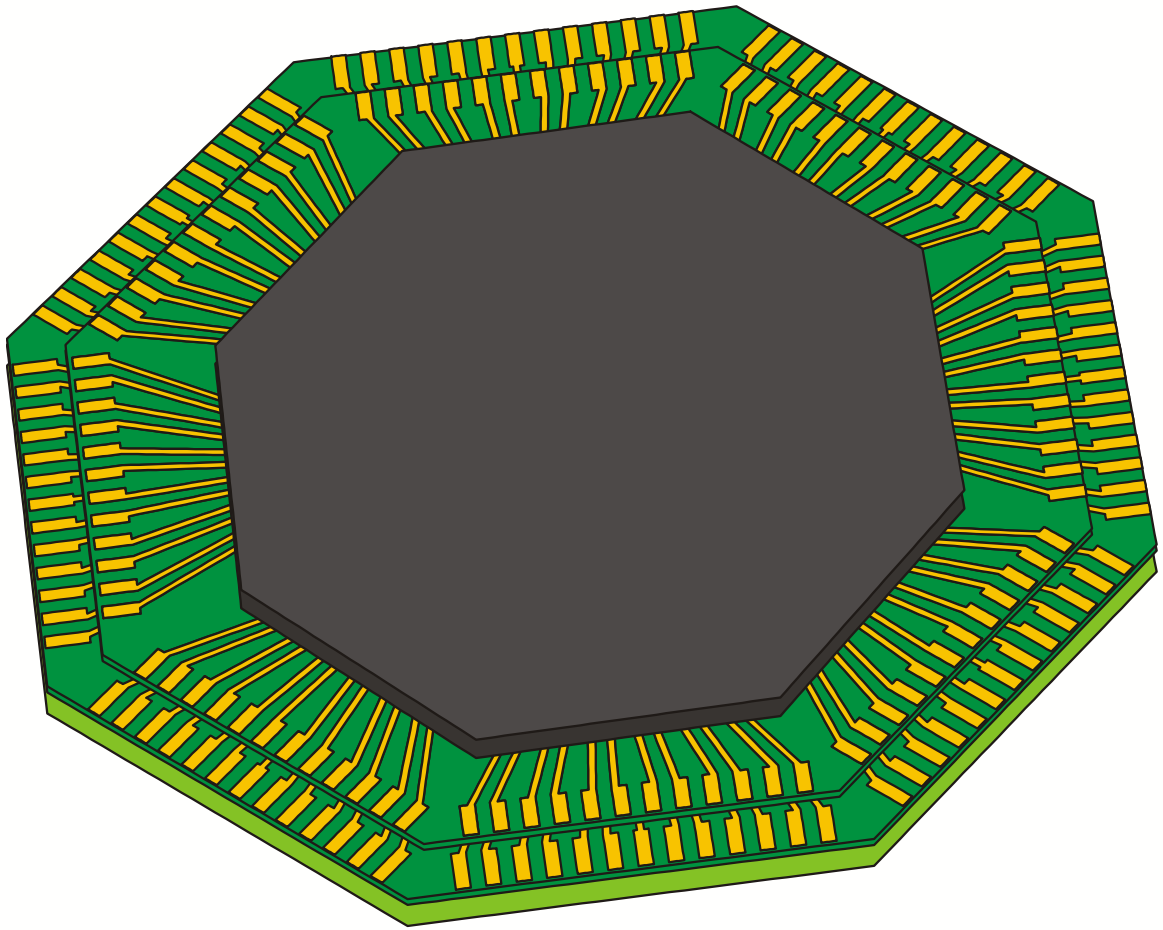


Patented

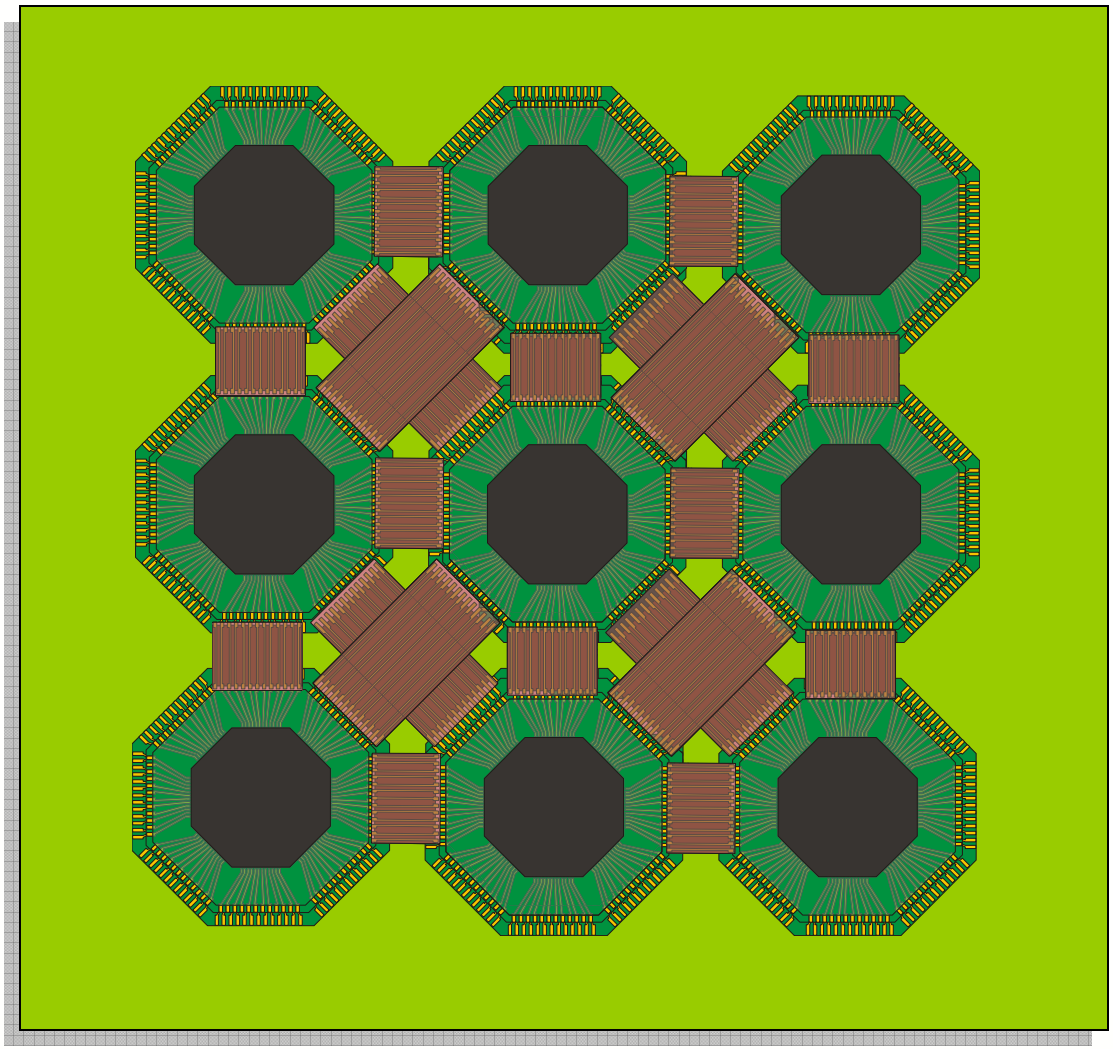
No Vias in Critical Paths of Chips



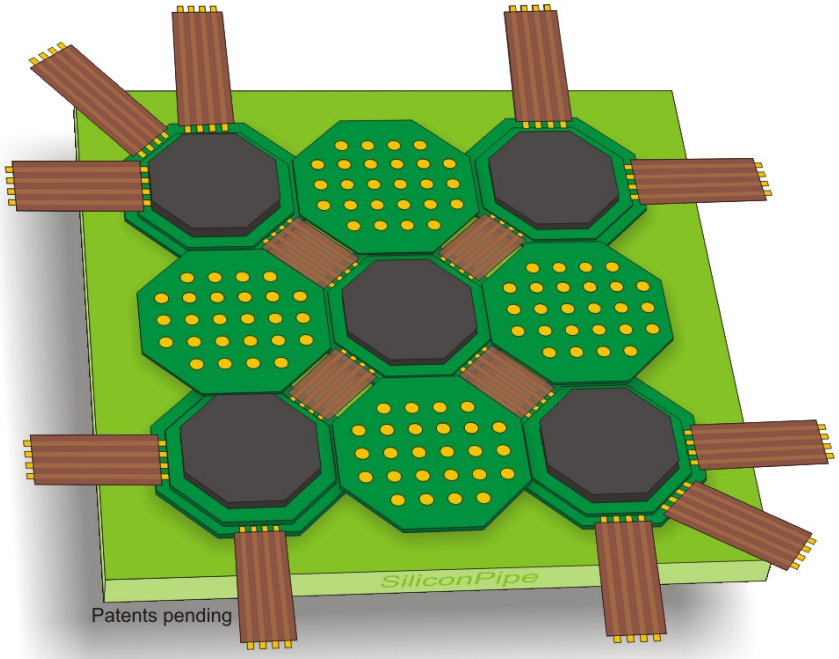
Prospective Stair Step SiP



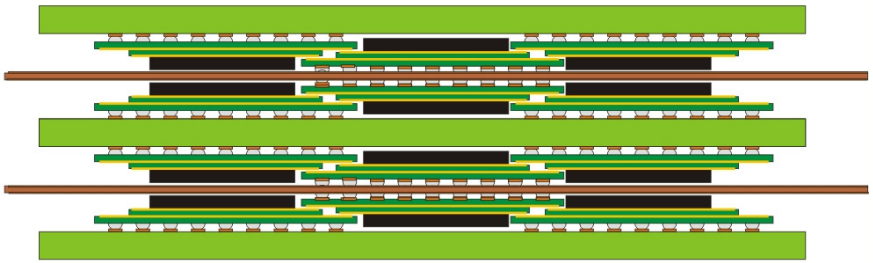
3D Interconnection Possibilities



Topographic Freedom

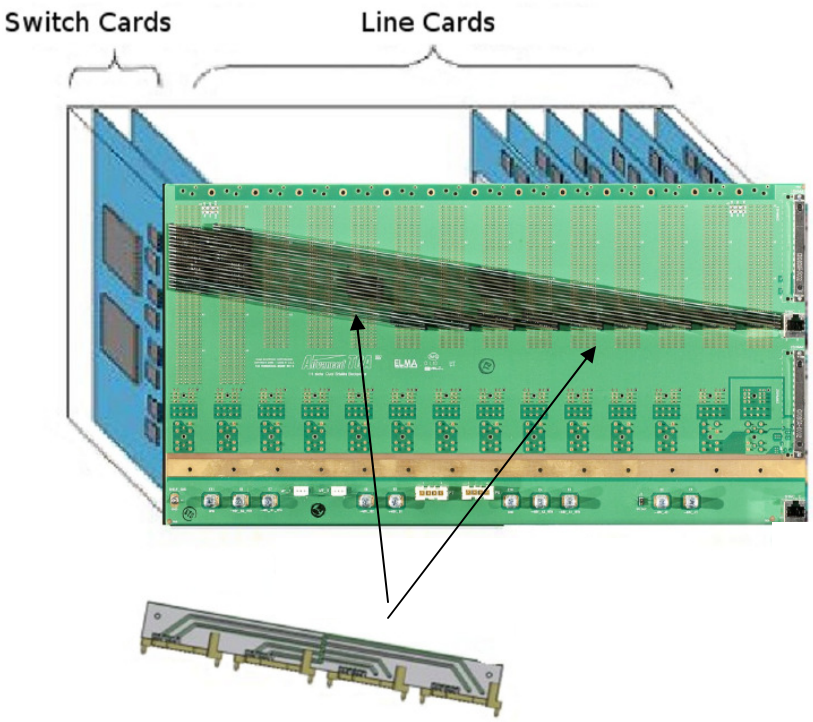


Flex for power, ground and high speed signals

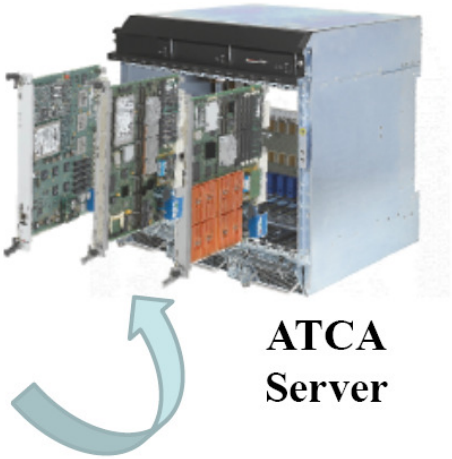


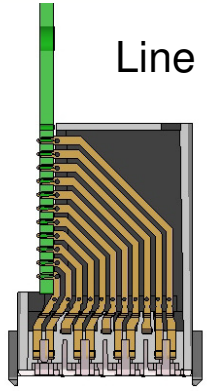
3D stacked circuit and package assemblies

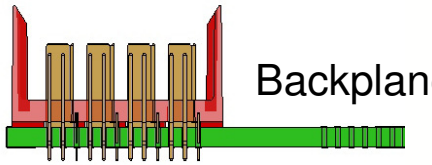
High Speed Orthogonal Links

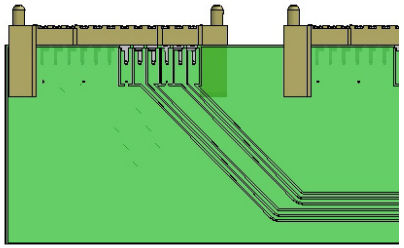


Out of plane 3D links





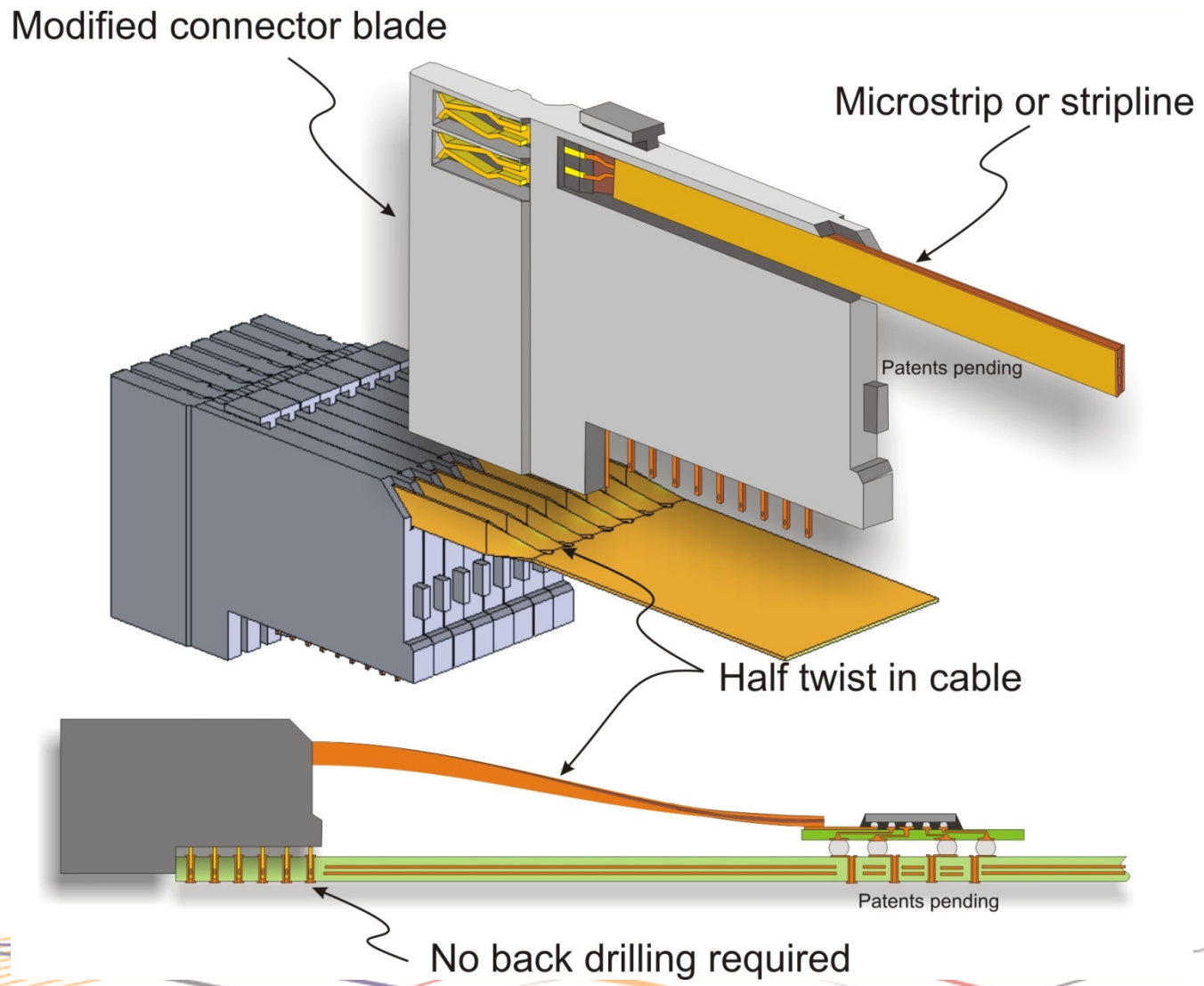




Out of plane links

Source: Z-plane, Inc

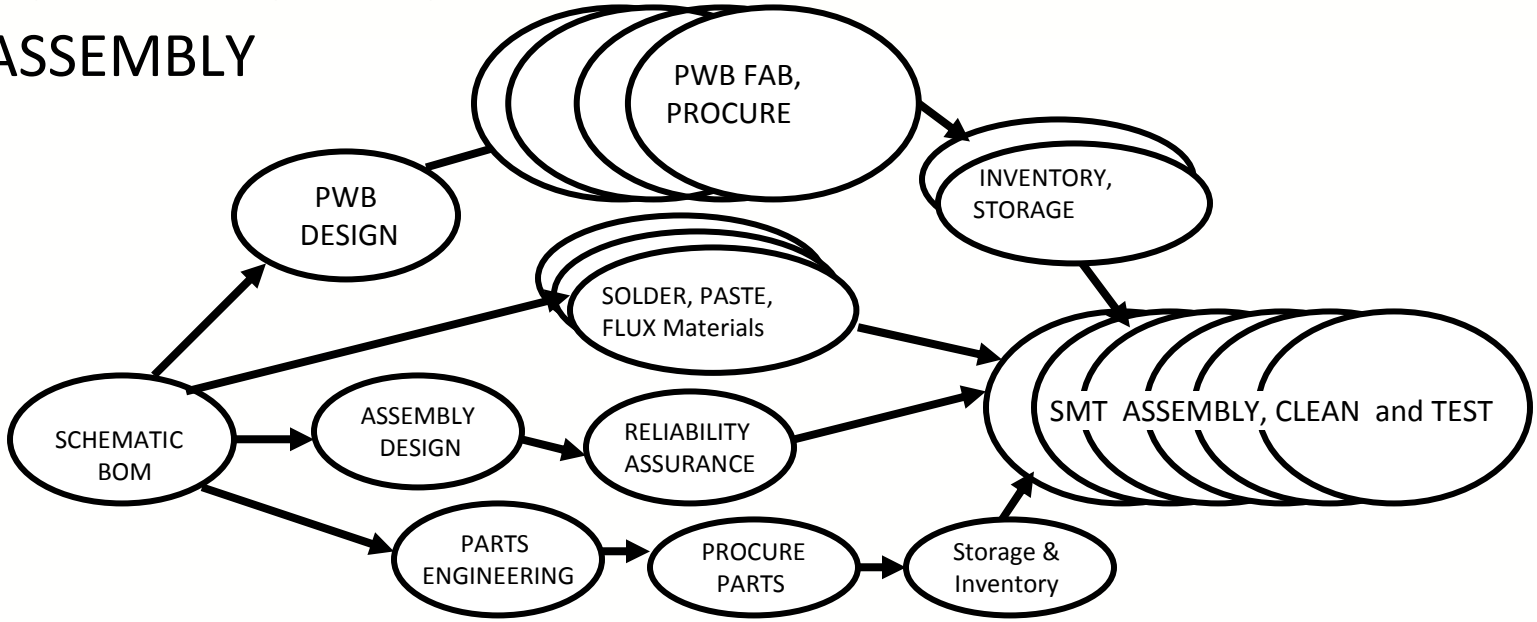
Direct Path Line Card Application



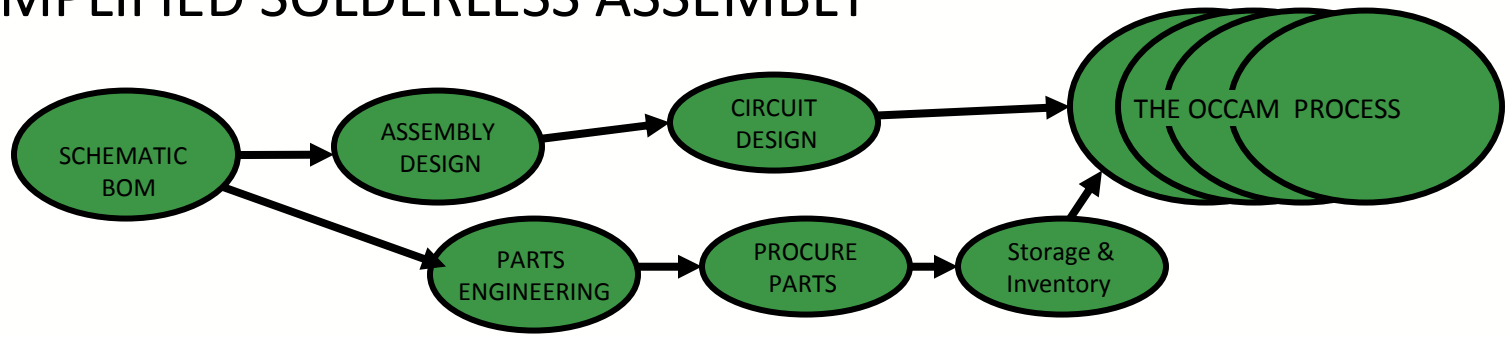
Patented

Solderless Assembly for Electronics (SAFE)

CONVENTIONAL SMT ASSEMBLY



SIMPLIFIED SOLDERLESS ASSEMBLY



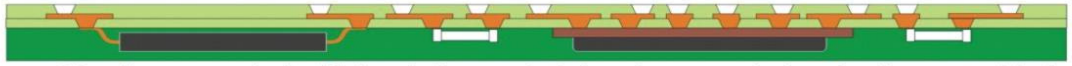
Sample Process Sequence

Tested and burned in components bonded to temporary or permanent base

Components and base are overmolded with insulating material

Assembly is inverted and component leads are accessed (e.g. By laser drilling)

Vias are plated along with circuit layer



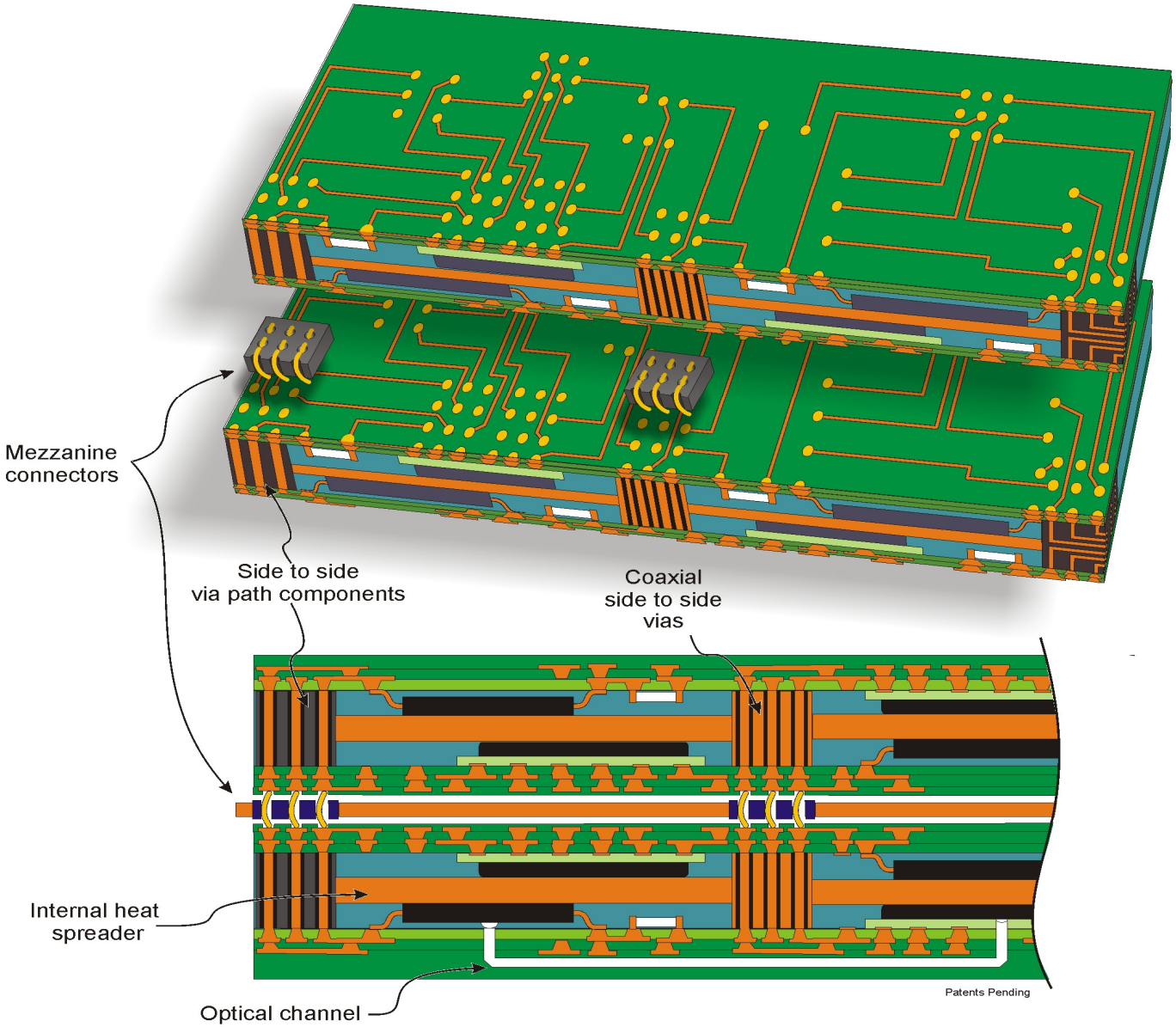
Circuits are coated with insulating material and access to terminations provided

Additional circuits are plated and additional layers built up to create needed connections

Final assembly circuits not needed for interconnection are protected with insulation

Reliability Improvement Potential With Solderless Alloy Free Electronics (SAFE)

- Simple structures with fewer elements
- Lower temperature processing avoids thermal damage caused by soldering
- Components are fully encapsulated increasing shock and vibration immunity
- Hermetic structure possibilities with full metal jacket protection
- Total EMI and ESD protection possibilities
- Integral heat spreader improves device life


Mezzanine connectors
Side to side via path components
Coaxial side to side vias
Internal heat spreader
Optical channel
Patents Pending

Summary

3D solutions have been used since the earliest days of electronics but there have been steady improvements in interconnection technologies to make products better, faster, smaller, lighter and cheaper and 3D will see increased use in the decades yet to come.