PCB Design Perfection Starts in the Cad Library Part 1 – The 1608 (Eia 0603) Chip Component

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ABSTRACT
The CAD library is the starting point that affects every process from PCB layout through PCB manufacturing and assembly. There are dozens of things to consider when creating a CAD library that are often overlooked or not even considered that will directly affect the quality of the part placement, via fanout, trace routing, post processing, fabrication and assembly processes. Part 1 of this paper describes every aspect that should be considered when creating chip CAD library parts and the impact that each feature of the CAD library has in the PCB process.

INTRODUCTION:
This paper is Part 1 of a series that is intended as an introduction to creating a high quality CAD library. We will review the elements of each component family on Tom Hausherr's blog. We need to address questions like:

- Why do we snap the lands (pads) to a 0.1mm grid?
- Why is the assembly outline different than the silkscreen outline?
- Why do we snap the via fanout to a 1 mm grid?
- Why is it important to use metric units when creating your CAD library?
- What is the IPC-7351B standard and why is it important?

All of the components and their related land patterns can be found in the free LP Viewer that you can download at www.mentor.com/go/lpwizard.

I will never forget my friend Wolfgang's description of a PCB design error: "A small error on an ugly PCB layout is a big deal, but the same exact error on a nice looking PCB layout is minor issue".

Every good PCB designer has the heart of an artist and the mind of a mathematician and each PCB design is a different piece of art with mechanical precision. A good PCB designer takes pride in their workmanship as they strive to make each new PCB layout more perfect than the last. After 35 years of laying out over 2,000 PCB designs I can say without any reservation that PCB design perfection starts in the CAD library.

One of the secrets of today is that 90% of all component manufacturers are providing their component package dimensions in metric units. Texas Instruments only provides metric units for all 982 of their component packages. TI is following the metric mandate by all world standards organizations and 99% of all world governments. So the CAD library should also be built using metric units. Using metric units for PCB design layout is the future, so you should transition to metric as soon as possible and quit wasting your time building an Imperial unit working environment. The longer you wait to transition the harder it becomes. If you're a PCB design artist in search of perfection, this paper will clearly illustrate why metric units for PCB layout is vastly superior. Let's start with the IPC7351B Standard.

IPC-7351B standard uses a 3-Tier CAD library system:
1. Least – for cell phones and hand held devices
2. Nominal – for controlled environment desktop
3. Most – for Military and Medical applications

I will be using the Nominal environment for the examples.

There are three types of CAD library parts; Through-hole, Surface Mount or a combination of the two technologies. SMD and PTH CAD libraries are distinctively different but the same basic rules apply to both technologies, "snap" and "round-off" CAD library land (pad) shapes to 0.05 mm increments. We need to discuss why this is so important and pictures are worth 1,000 words. Also, trying to create a paper that goes through the entire list of standard component families can turn into a 100 page book really fast. I also want to hear your feedback on these very important issues.

After all, we're talking about our favorite subject "PCB Design Perfection" and if it starts at the CAD library, we need an open forum for discussion.

I'm going to give you a sample of the subject in this paper and then start posting all the other data at **http://blogs.mentor.com/tom-hausherr/**. Each component family will have a dedicated post. Chip components are the majority of the parts on a normal PCB layout. Chip components have a "Wraparound" lead form. The last PCB layout I did had 698 capacitors, 386 chip resistors and 81 chip inductors. The entire design had 1,250 parts and 1,165 or 93% were chip components. So it is very important that we address chip components first. The majority of chip components are metric by design. i.e.: 90% of all chip component dimensions are whole metric values. See Figure 1 for the dimensions of a standard 1608 (EIA 0603) component superimposed with its related land pattern and placement courtyard excess of 0.25 mm. Notice that the placement courtyard is 3.0 mm X 1.5 mm. This is perfect for placing this land pattern using a 0.5 mm grid system. They all line up perfectly.

The land size and centric placement are rounded in 0.05 mm increments to enhance trace routing using a 0.05 mm routing snap grid and trace widths in 0.25 mm increments.

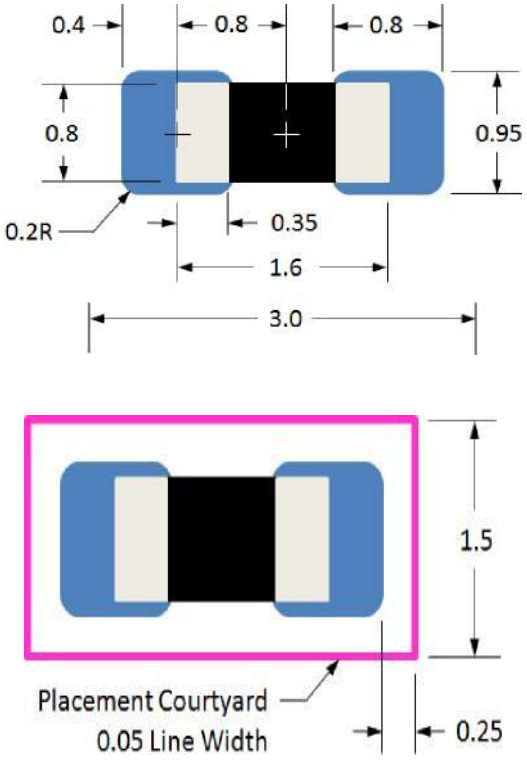

Figure 1

Figure 2 illustrates four of the most popular trace/space routing technologies that use a 0.05 mm routing grid. The 6 most popular metric trace widths rounded in 0.25 mm increments –

1. 0.075 mm (3 mils)
2. 0.1 mm (4 mils)
3. 0.125 mm (5 mils)
4. 0.15 mm (6 mils)
5. 0.2 mm (8 mils)
6. 0.25 mm (10 mils)

The main point that I am trying to make here is that using a PCB design grid system is best when using most CAD tools. One of the exceptions to this is the Expedition Enterprise CAD tool that handles gridless solutions effortlessly. But for everyone else in the industry, building CAD libraries, part placement, via fanout and trace routing using specific snap grids greatly enhances the speed and quality of the PCB layout.

The standard universal grid system to in 2010 is 0.05 mm but at times 0.025 mm increments need to be used specifically for trace/space rules.

The next generation of grid systems in the near future will be 0.01 mm, which I refer to as "high resolution". There will never be a need to go more than 2 places to the right of the decimal point for any PCB design feature values.

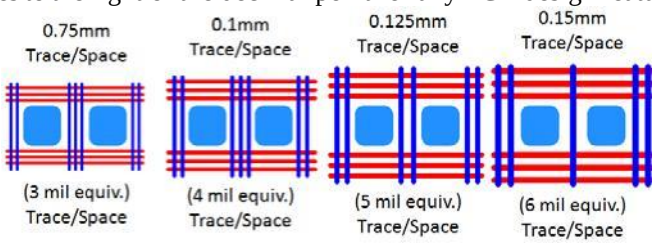

Figure 2

The same chip component technology can be applied to every chip resistor and capacitor used in the industry today. The most relevant aspect of this technology is that a 0.1 mm placement grid and a 0.05 mm routing grid system produces optimized results regardless of the trace/space technology because the land (pad) center snap grid is 0.05 mm from the origin and the land (pad) size round-off values are in 0.05mm increments.

Let's talk about via fanout solutions for the same 1608 (EIA 0603) chip capacitor. In Figure 3 you can see 2 different fanout options and one is superior to the other. The fanout coming out the top has all the key features.

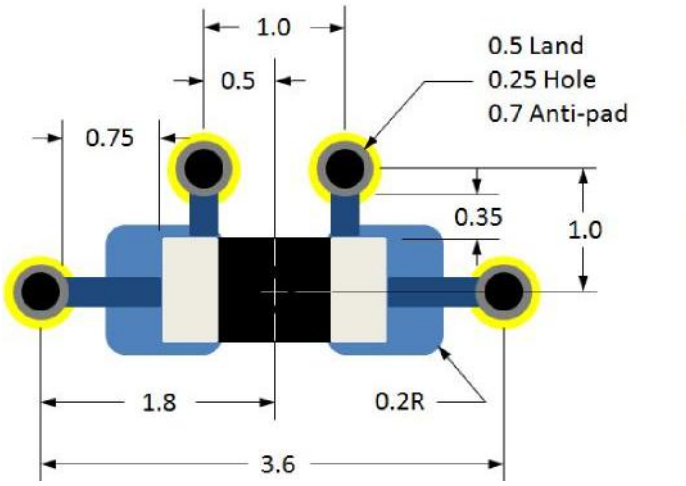

Figure 3

The vias are 0.4 mm closer to the capacitor component terminals than the typical right/left fanout which decreases impedance and increases capacitance. Also, the top fanout vias snap to a 1 mm grid because the 1608 land pattern was snapped to a 0.5 mm grid system. The 0.5 mm via land (pad) diameter with 0.25 mm hole size and 0.7 mm plane anti-pad is perfect for 0.1mm trace/space technology. See Figure 4 for the routing solutions. The trace width for the power fanout is 0.3 mm.

Figure 3

Figure 3 clearly illustrates the superior routing channels between two vias placed on a 1 mm snap grid. This same example can be used for all Chip and Molded Body Resistors and Capacitors. It is important to note that the plane anti-pad clearance does not infringe on the trace. The trace requires a clean uninterrupted return path on the adjacent reference plane. This via land, hole size and trace/space technology is very easy to manufacturer and does not require additional fabrication cost.

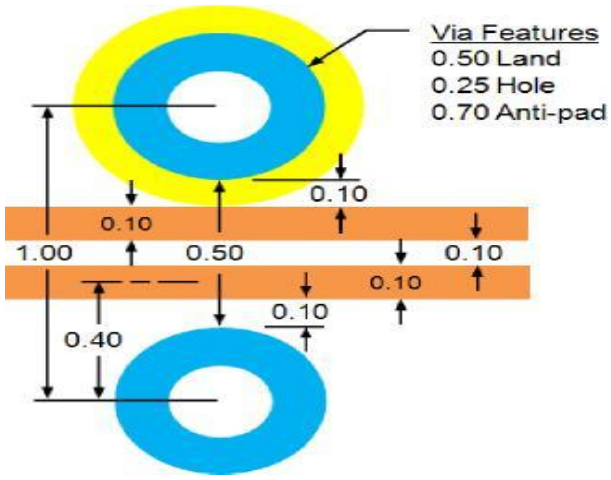

Figure 4

The part placement of the 1608 can use a 0.5 mm snap grid and the placement courtyards can be placed side by side. The via fanout can be a 1 mm snap grid when exiting the side of the land pattern, otherwise when exiting the top and bottom, a 0.1mm snap grid can be used.

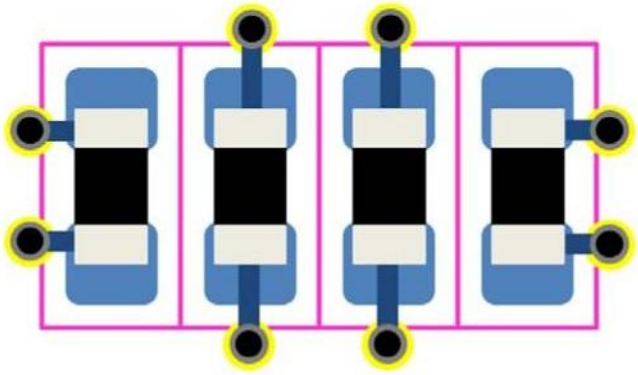

Figure 5

See Figure 5 for the placement and fanout example for the 1608 chip components.

The IPC-7351B standard when a chip component size is less than 1.6 mm X 0.8 mm there are 7 rule changes that every PCB designer or CAD librarian must be aware of:

1. The Land (pad) snap grid changes from 0.1 mm to 0.02 mm
2. The land size round-off changes from 0.05 mm to 0.01 mm
3. The Toe goal changes from 0.35 mm to 0.2 mm
4. The corner radius changes from 0.2 mm to 0.15 mm
5. The courtyard excess changes from 0.25 mm to 0.15 mm.
   When entering the component min/max dimensions the "Nominal" Terminal dimensions are used for both the min & max fields
6. The part placement grid changes from 0.5 mm to 0.1 mm

Here are some basic guidelines and drafting recommendations for your Chip and Molded Body CAD library.

1. Pad Spacing with DRC Checking and Pad Trimming when necessary

a. Default Land to Land (inside to inside) Clearance is 0.2 mm
b. Default Silkscreen to Land Clearance is 0.25 mm

2. Four Outlines
   a. Silkscreen
      i. Silkscreen to exposed copper clearance setting defaults to 0.25 mm
      ii. Auto-trim feature to avoid exposed copper
      iii. Outline size can be set to Nominal or Maximum component body
      iv. Line Width default is 0.2 mm
      v. Snap grid is 0.1 mm
   b. Assembly
      i. Outline size can be set to Nominal or Maximum component body
      ii. Line Width default is 0.1 mm
      iii. Snap grid is 0.1 mm
   c. Placement Courtyard adjustable sizing for IPC 3-Tier environment levels
      i. Default outline size is set to Maximum component body
      ii. Line Width default is 0.05 mm
      iii. Snap grid is 0.1 mm
   d. 3D Model Outline
      i. Default outline size is set to Maximum component body
      ii. Line Width default is 0.001 mm
      ii. Outline snaps to real maximum component outline (gridless)

3. Polarity Marking
   a. Silkscreen
      i. Default size is 0.5 mm minimum
   b. Assembly
      i. Default size is 1 mm minimum

4. Two Reference Designators with center/center justification (Ref Des Origin), right reading orthogonal, located at the land pattern origin with Height 1.5 mm and line width 10% of Height
   a. Silkscreen
   b. Assembly with automatic sizing for miniature parts (1005 & 0603)

5. IPC Zero Component Orientations
   a. 2-pin parts have Pin 1 on left

Go to http://blogs.mentor.com/tom-hausherr/ to read the remainder of this series of PCB Design Perfection Starts at the CAD Library. We're going to cover other Chip components and then Molded Body components and then SOT (Small Outline Transistor) component families next. I will elaborate on land pattern creation of all standard components.

PCB Design Perfection Starts in the CAD Library

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Anatomy of a CAD Library

- IPC-7351B 3-Tier Library System
- Land Pattern Naming Convention
- Component Lead Styles
- Solder Joint Analysis & Manufacturing Tolerances
- Padstacks
- Placement Courtyard
- Silkscreen & Assembly Outlines and Polarity marks
- Zero Component Orientation
- Land Pattern Origins
- Reference Designators
- 3D Modeling

3-Tier Library System

- Three land pattern geometry variations are supplied for each of the device families; Maximum Land Protrusion (Density Level A), Nominal Land Protrusion (Density Level B) and Least Land Protrusion (Density Level C).
- **Density Level A:** Maximum (Most) Land Protrusion – For low-density product applications, the 'maximum' land pattern condition has been developed to accommodate wave or flow solder of leadless chip devices and leaded gull- wing devices. The geometry furnished for these devices, as well as inward and “J”-formed lead contact device families, may provide a wider process window for reflow solder processes as well.

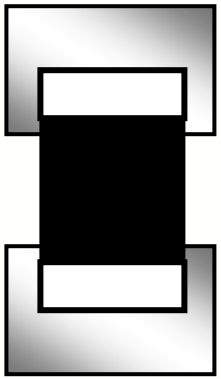
3-Tier Library System

- **Density Level B**: Median (Nominal) Land Protrusion – Products with a moderate level of component density may consider adapting the 'median' land pattern geometry
- The median land patterns furnished for all device families will provide a robust solder attachment condition for reflow solder processes and should provide a condition suitable for wave or reflow soldering of leadless chip and leaded Gull Wing type devices

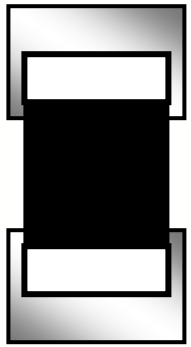
3-Tier Library System

- **Density Level C**: Minimum (Least) Land Protrusion – High component density typical of portable and hand-held product applications may consider the 'minimum' land pattern geometry variation
- Selection of the minimum land pattern geometry may not be suitable for all product use categories. The use of classes of performance 1, 2, and 3 is combined with that of component density levels A, B, and C in explaining the condition of an electronic assembly
- As an example, combining the description as Levels 1A or 3B or 2C, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular assembly.

3-Tier Land Pattern Variations



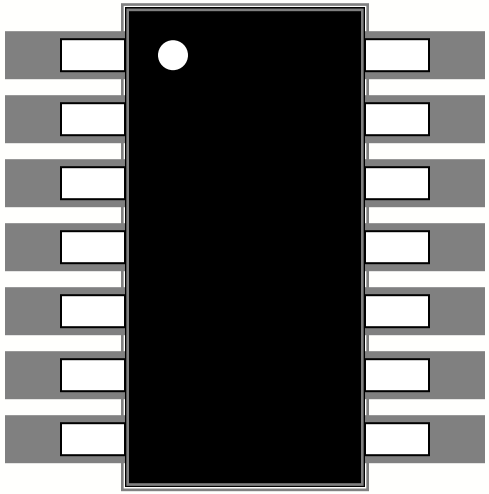
Density Level A
Very Robust
Solder Joint



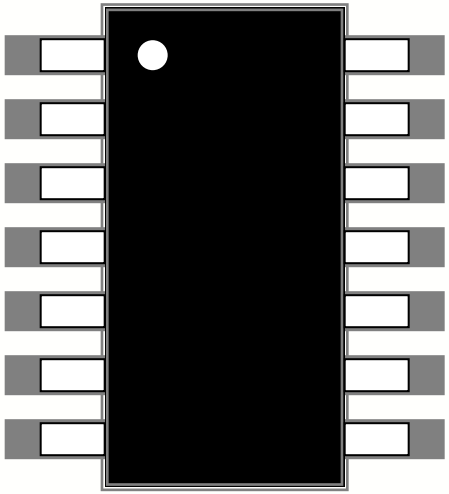
Density Level B
General Purpose
Solder Joint

Density Level C
Minimal Solder Joint
High Density
Applications

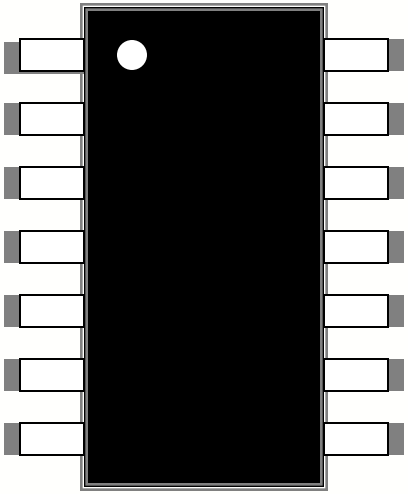
3-Tier Land Pattern Variations



Density Level A
Very Robust
Solder Joint



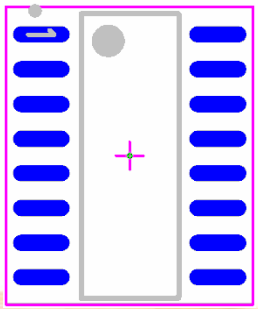
Density Level B
General Purpose
Solder Joint

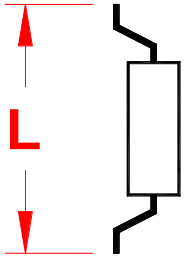


Density Level C
Minimal Solder Joint
High Density
Applications

IPC-7351 Naming Convention

Family	Pitch	Lead Span	Pin Qty
SOIC	1.27	7.10	14
SOP	0.80	7.10	14
SOP	0.65	7.10	14
SOP	0.50	7.10	14
SOP	0.40	7.10	14





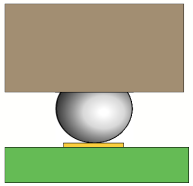
Note: An Odd Pin Qty = Thermal Tab in Center

IPC-7351 Naming Convention

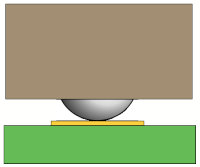
- SOP = Small Outline Package
- Pitch = Two places past both sides of the decimal point followed by a “P” (50P = 0.50mm)
- Lead Span = Two places past both sides of the decimal point followed by a “X” (710 = 7.10mm)
- Height = Two places past both sides of the decimal point followed by a “-” (120- = 1.20mm)
- Naming Convention for Gull Wing Lead Parts:
- **Component Family + Pitch + Lead Span X Height - Pin Qty + Environment Level** (L, N or M)
- Example: **SOP50P710X120-14N**

Component Lead Styles

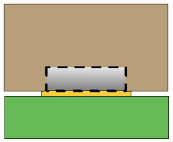
Ball Grid Array



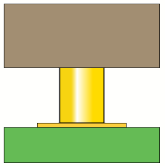
Bump Grid Array



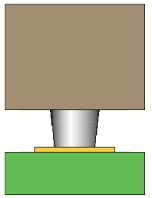
Bottom Grid Array



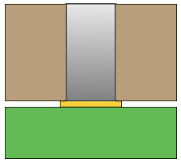
Column Grid Array



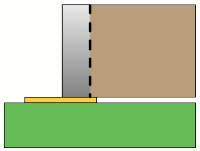
Pillar Grid Array



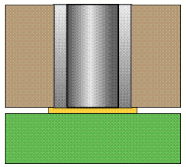
Flat Side



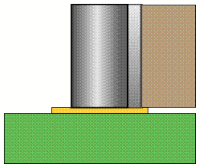
Convex Side



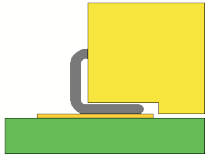
Concave Side



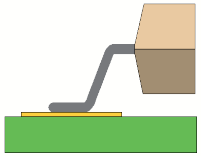
Corner Concave



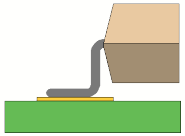
Inward L



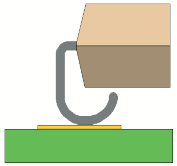
Gull Wing



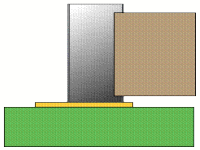
Outward L



J-Lead

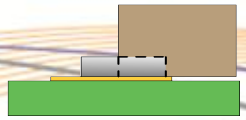


End Cap

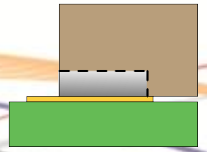


Under Body L

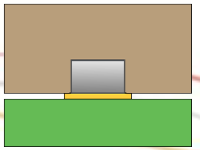
Flat



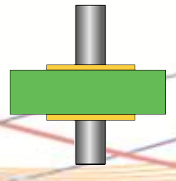
Flat Bottom



No-Lead



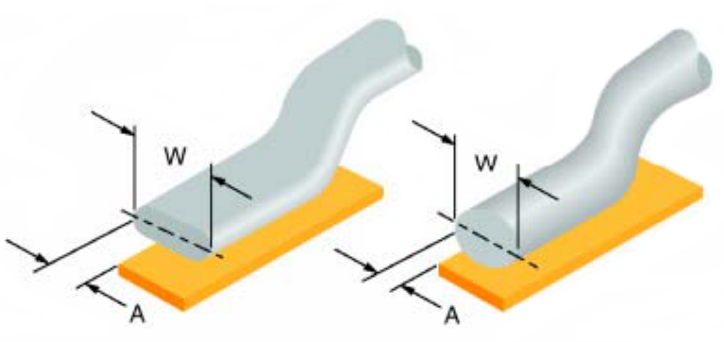
Through-hole



Solder Joint Analysis

- Solder Joint Toe, Heel and Side Goal
  - The chart below provides an example of the Gull Wing component lead Solder Joint Goal

Round or Flattened Leads



Round or flattened (coined) leads (unit: mm)

Land pattern characteristics	**Maximum Level 1**	**Median Level 2**	**Minimum Level 3**
Toe-land protrusion	1,0	0,65	0,2
Heel-land protrusion	0,5	0,35	0,2
Side-land protrusion	0,1	0,1	0,1
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0.5	Nearest 0.5	nearest 0.05

Manufacturing Tolerances

- Fabrication Tolerances
- Assembly Tolerances
- Component Terminal Tolerances
- Land Placement Round-off
- Land Size Round-off

Land Pattern Equations

- $Z_{max} = L_{min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$
- $G_{min} = S_{max} - 2J_H - \sqrt{C_L^2 + F^2 + P^2}$
- $X_{max} = W_{min} + 2J_S + \sqrt{C_L^2 + F^2 + P^2}$

- ***where***
  - ***Z is the overall length of land pattern;***
  - ***G is the distance between lands of the pattern;***
  - ***X is the width of land pattern;***

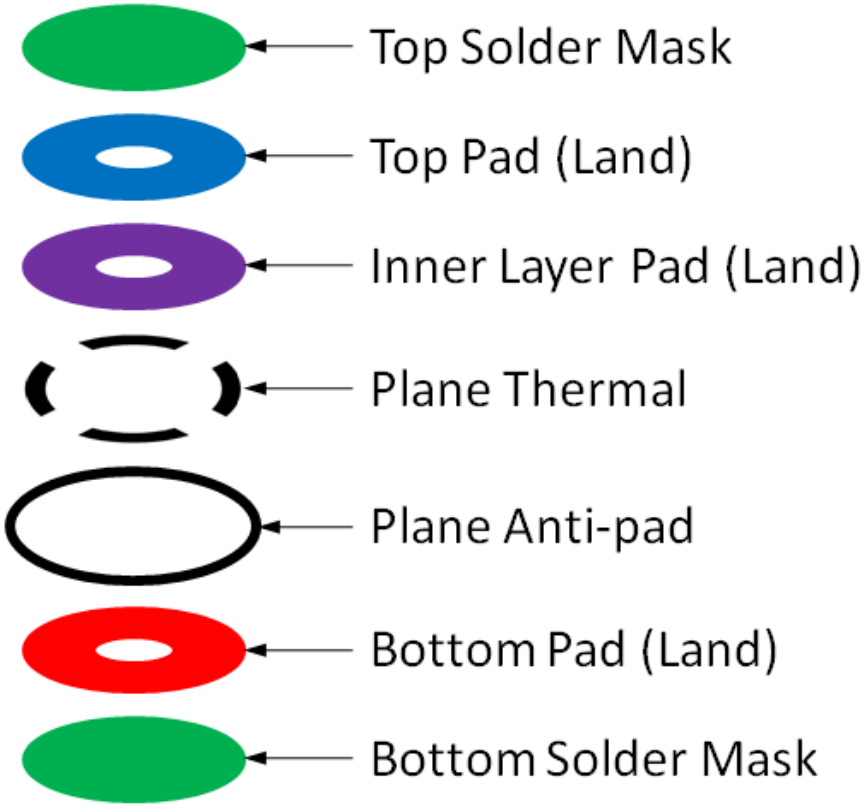
Describe “Duplication” of Fabrication Tolerance

SMD Padstacks

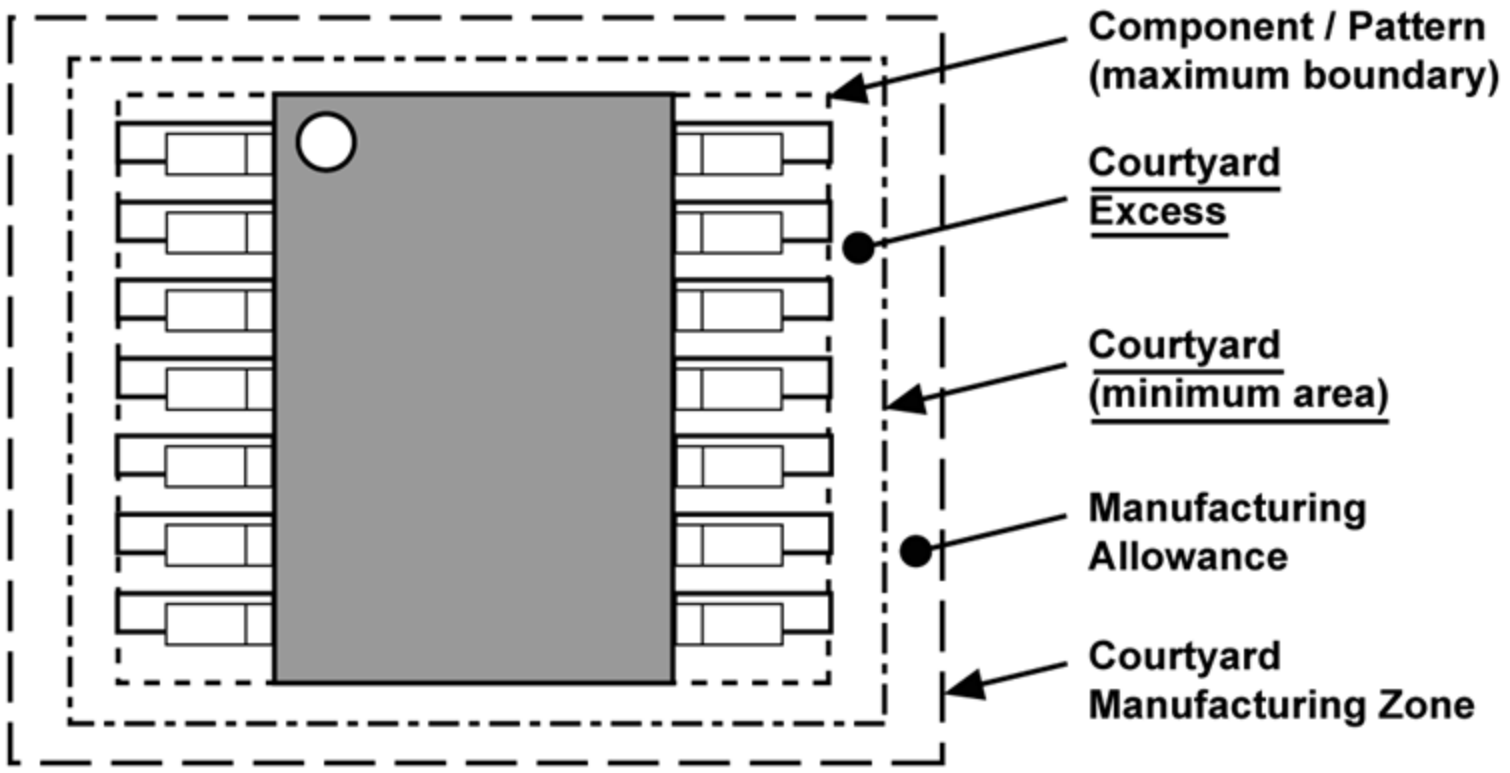
- The surface mount component padstack consists of a solder pad, solder mask and solder paste
- The solder mask and paste mask size are typically the same as the pad size
- **Solder Mask** – Allow the PC Board manufacturer to expand the solder mask size according to the trace/space DRC rule technology that the PCB designer used in the PCB design the layout
- **Solder Paste** – Allow the stencil manufacturer to over/under size the solder paste to match the specifications of the assembly shop that the paste mask stencil is being made for

PTH Padstacks

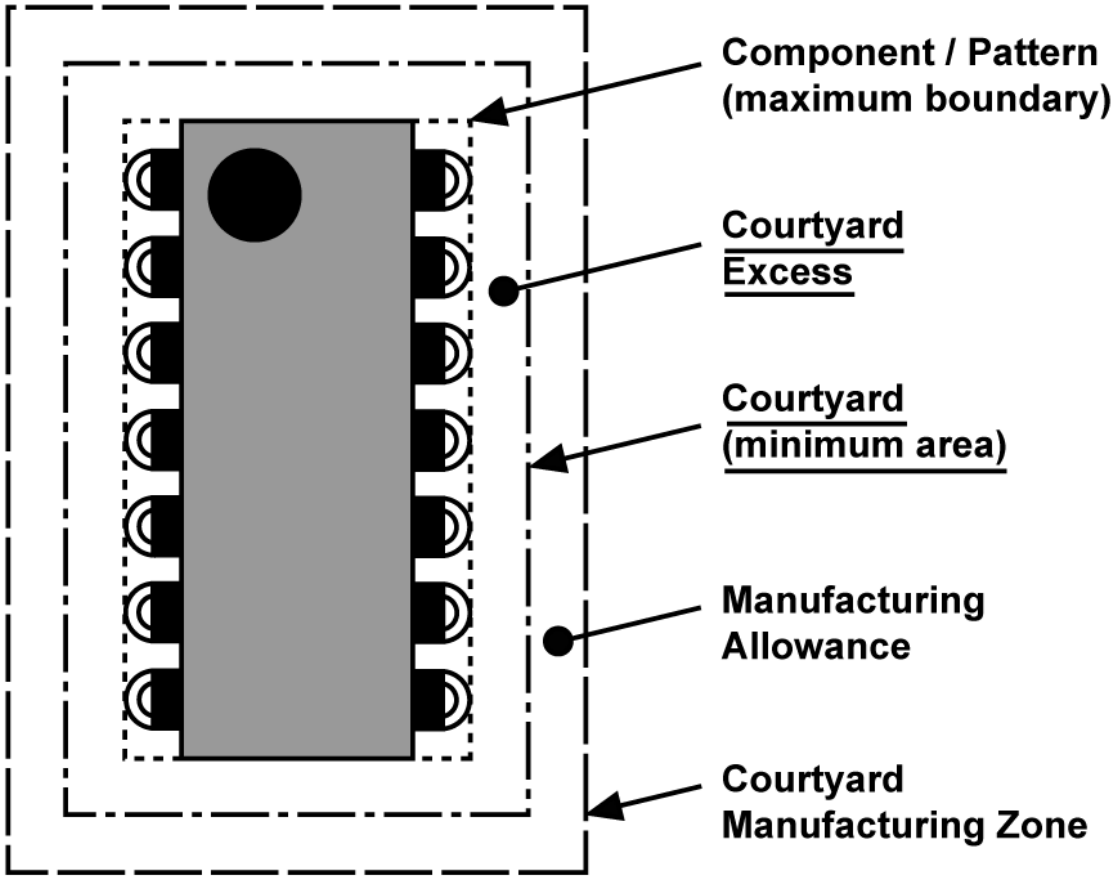
- This is what a typical Through Hole Padstack is built like:
  - Top Solder Mask
  - Top Pad
  - Inner Layer Pad
  - Plane Thermal Relief
  - Plane Anti-pad
  - Bottom Pad
  - Bottom Solder Mask
  - Drilled Hole



SMT Placement Courtyard



PTH Placement Courtyard



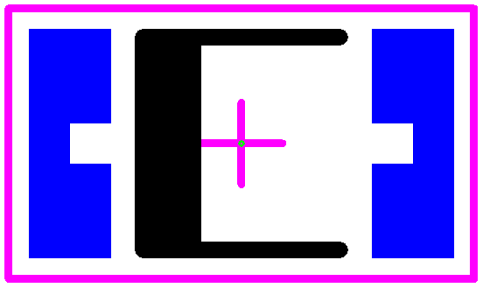
Silkscreen Outlines

- Silkscreen outlines are used for cosmetic purposes only and are really not required by manufacturing
- The silkscreen can be drawn by the PCB designer very complex to illustrate their creative talent or very simple. In the end, it really doesn’t matter because you can only see it when the physical PC board passes between the fabrication facilities to the assembly shop.
- Once the parts are assembled, all the silkscreen outlines are covered up and cannot be seen.
- When PCB designers start to use all the principles discussed in this presentation, the manufacturing assembly process can be fully automated and silkscreen component outlines will not be required

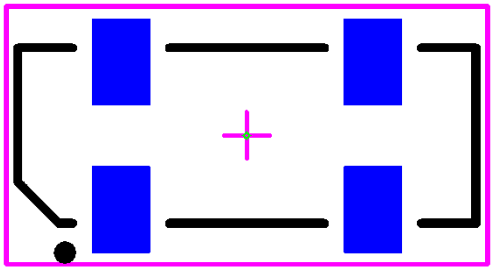
Silkscreen Outlines

- The term Polarity Marking came from its use to identify the Positive Pin on a “Polarized” capacitor. But polarity marking is also used on Diodes to indicate the Cathode Pin
- Polarity Markings are also used when there is a potential for inverting the part placement in the assembly process that would result in a malfunction of the component

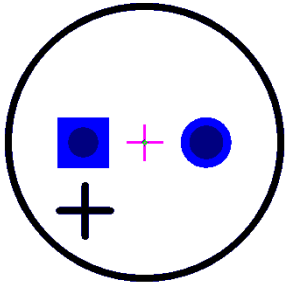
MELF DIODE



OSCILLATOR

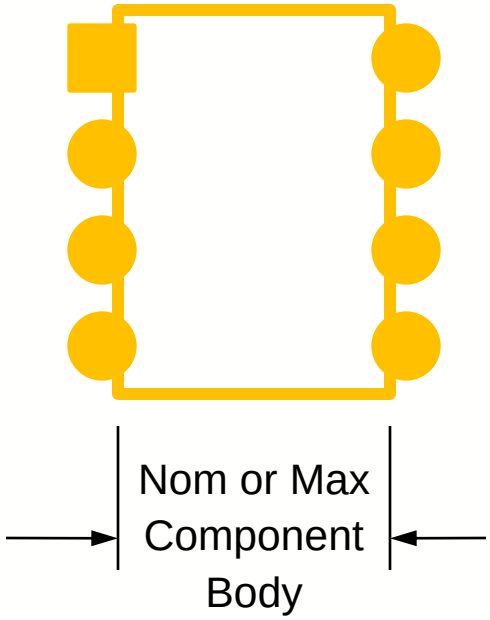


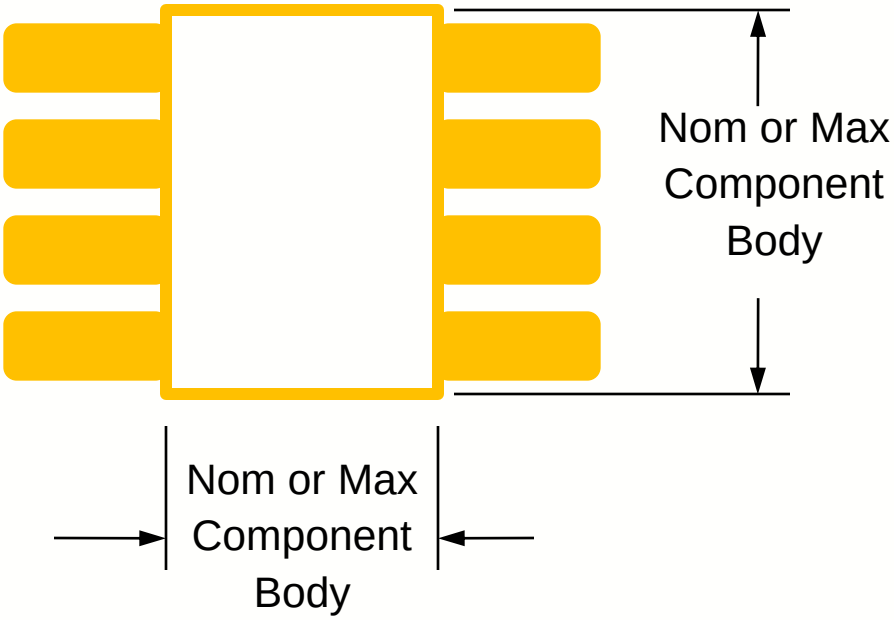
CAPACITOR



Assembly Outlines

Assembly Line Widths: Min. 0.01mm, Nom. 0.1mm, Max. 0.25mm

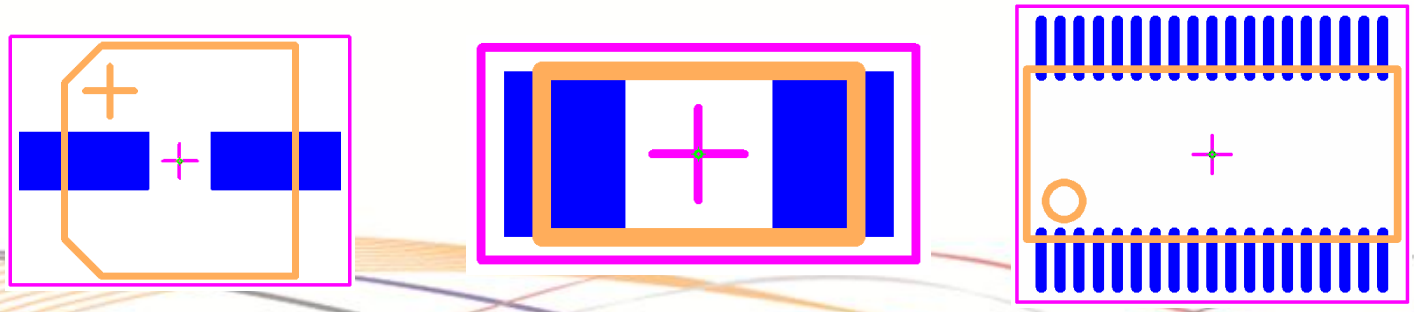




Assembly Outlines

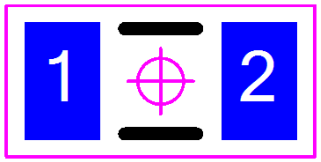
- The assembly drawing outline should represent the maximum outline of the component body
- Unlike the silkscreen outline which has to be created to avoid solder pads (a fake component outline)
- The assembly outline only gets placed on an assembly drawing that goes to the assembly shop

Sample of assembly drawing component outlines in relationship to the solder pad

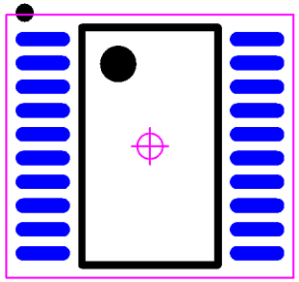


Zero Component Orientation

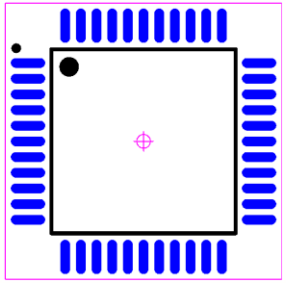
- Chip Capacitors, Resistors and Inductors
  - Pin 1 on Left



- Molded Capacitors, Resistors and Inductors
  - Pin 1 (Positive or Cathode) on Left
- MELF Resistors and Diodes
  - Pin 1 (Positive or Cathode) on Left



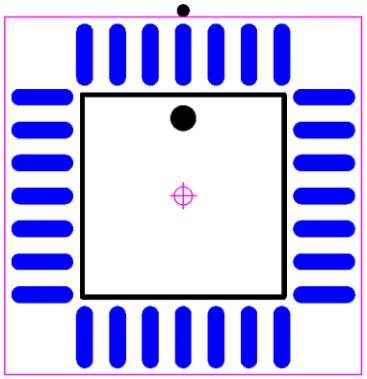
- SOT Devices SOT23, SOT223, SOT89, SOT143
  - Upper Left
- TO252 & TO263 (DPAK Type) Devices
  - Upper Left

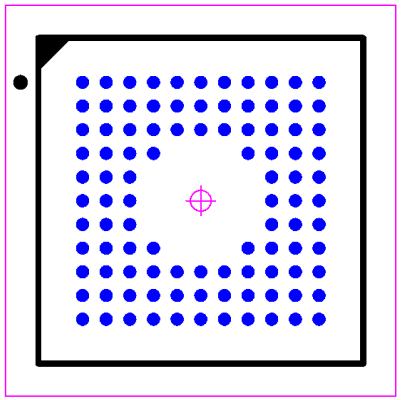


- Small Outline Gull Wing IC's – SOIC & SOP
  - Upper Left

Zero Component Orientation

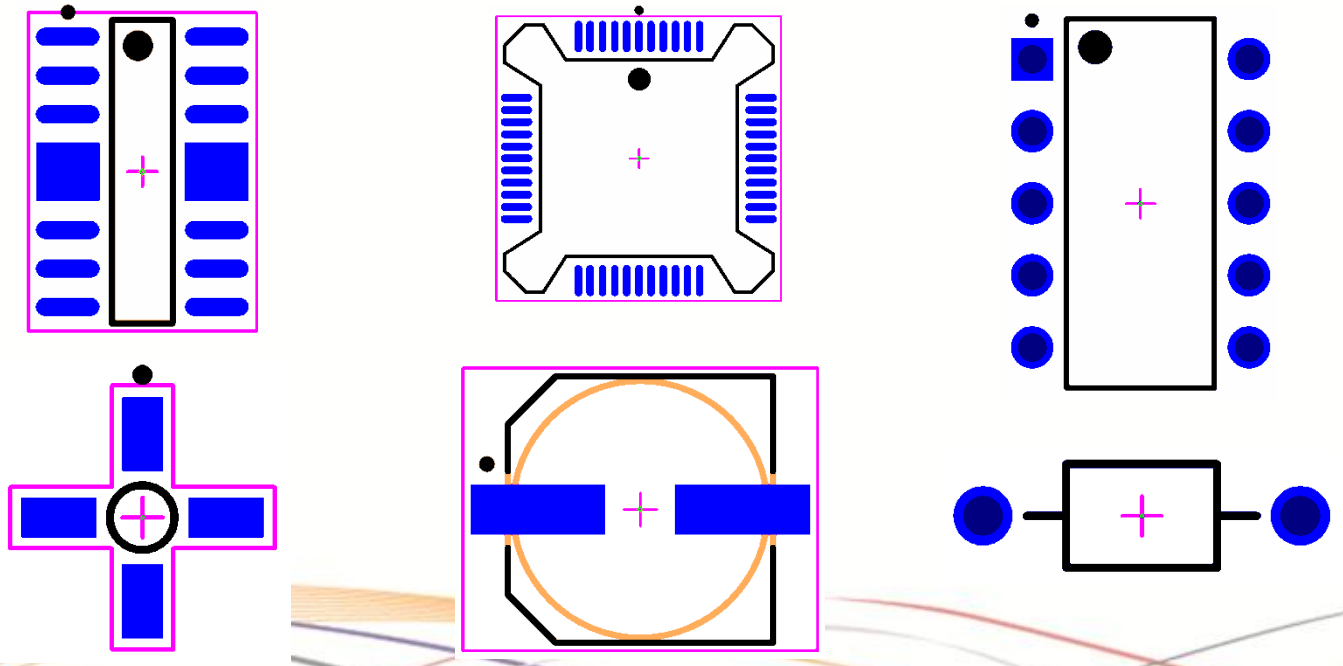
- Small Outline J Lead ICs (SOJ)
  - Pin 1 Upper Left
- Quad Flat Pack ICs (PQFP, SQFP)
  - Pin 1 Upper Left
- Ceramic Quad Flat Packs (CQFP)
  - Pin 1 Upper Left
- Bumper Quad Flat Pack ICs (BQFP)
  - Pin 1 Top Center
- Plastic Leaded Chip Carriers (PLCC)
  - Pin 1 Top Center
- Leadless Chip Carriers (LCC)
  - Pin 1 Top Center
- Quad Flat No-Lead ICs (QFN)
  - Pin 1 Upper Left
- Ball Grid Arrays (BGA)
  - Pin A1 Upper Left





Land Pattern Origins

- The land pattern origin is the component “Center of Gravity” so in most cases it’s the Center of the library part.
- An example of where it’s not the center is the DPAK or TO-252 component.



Reference Designators

Ref Des Heights: Min. 1.0mm, Nom. 1.5mm, Max. 2.5mm

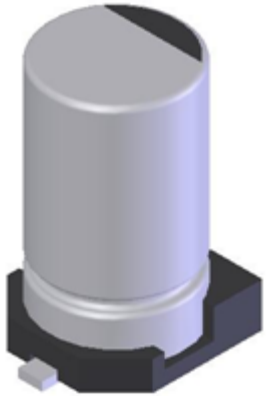
- The Ref Des line width is normally 10% of the height. This is to prevent the bleeding of characters.
- The Silkscreen Ref Des is placed inside the land pattern until after Part Placement is completed and then they are relocated outside the component

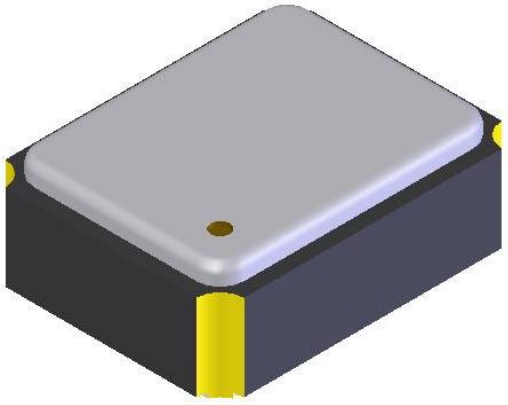
Reference Designators

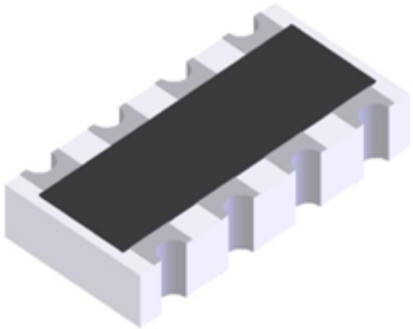
A	separable assembly
AR	amplifier
AT	attenuator; isolator
B	blower, motor
BT	battery
C	capacitor
CB	circuit breaker
CP	connector adapter, coupling
CN	capacitor network
D or **CR**	diode
D or **VR**	breakdown diode
DC	directional coupler
DL	delay line
DS	display, lamp
E	terminal
F	fuse
FD	fiducial
FL	filter
G	generator, oscillator
GN	general network
H	hardware
HY	circulator, directional coupler
J	connector, jack, female
K	contactor, relay
L	coil, inductor, bead, ferrite bead
LS	loudspeaker, buzzer
M	meter
MG	motor-generator
MH	mounting hole
MK	microphone
MP	mechanical part
P	connector, plug, male
PS	power supply
Q	transistor
R	resistor
RN	resistor network
RT	thermistor
S	switch
T	transformer
TB	terminal board, terminal strip
TC	thermocouple
TP	test point, In-circuit test points
TZ	transzorb
U	inseparable assembly, IC pkg
V	electron tube
VR	voltage regulator
W	wire, cable, cable assembly
X	fuseholder, lampholder, socket
Y	crystal, magnetostriction oscillator
Z	miscellaneous

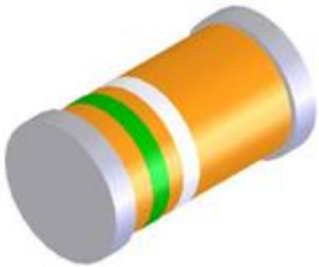
3D Modeling

- Every CAD tool has a different approach to handling 3D Models of component data. Some are much more elaborate than others.
- The CAD Library of the Future will have 3D Model attributes built into every land pattern to use as a mechanical drafting aid for the reduction of errors in product packaging









Questions?