Low Cost Electrical Specifications for Design and Manufacture of GHz Boards

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Abstract
Test and quality coverage for an assembled printed circuit board is becoming increasingly more expensive and complex as digital electronics moves well into the gigahertz era. Traditional tools like time domain (TD) statistical simulation and Bit Error Rate Testers (BERT) are presently used to verify and test gigabaud digital designs. Unfortunately not only is a very high level of technical experience is required, but just the logistics of the setup can be monumental. The proposal is to use a few simple scalar metrics like signal to noise ratio (SNR) to let the quality of a board stand simply on its own electrical merits. These new metrics are much easier to acquire from scattering parameters than traditional simulation or BERT testing.

They are an outgrowth of the IEEE 10 Gigabit per second backplane standard work.
Context and usage models are presented as discussion of frequency domain (FD) interconnect metrics are developed. One such usage is that electrical board quality can be mapped on a trace by trace basis in terms of an associated scalar electrical quality factor or metric. These metrics may become the basis of an "exchange metric" between customer and vendor.

Introduction
Prior to the last decade signaling speeds for the critical routing on printed circuit boards (PCB) were mostly below 100 Megahertz. A board manufactures assured a board will work by determining if nets are connected and parts inserted correctly. Designers assured a board's signaling would work by verifying setup and hold times were met. The designer or signal integrity engineer may have performed simulation for one or two cycles that mostly considered reflections and propagation time. Tools soon became available to examine every network on a PCB. The signal integrity green-light for a design depended on the set up and hold time margin observed. Once the first boards were received by designers signal quality was assured by probing the pins of IC's to make sure there were no set up and hold time violations.

Once the signaling speeds exceeded 1 GHz a number of interesting things began to happen to simulation and measurement. More than a few cycles were required for analysis because the signal settling time significantly exceeded the bit period. This resulted in inter-symbol interference (ISI) which caused jitter and signal loss to became a significant concern. Silicon jitter, once a budget bucket, moved in as a major contributor to signal degradation. The signal quality factor graduated from set up and hold margin to the likelihood of an error occurring, measured as a bit error ratio (BER). At these speeds, signals measured at the pins of a device are not representative of whether data is received correctly. Transmitters and receivers begin to employ a gamut of signal processing techniques themselves to aid in the reception of a signal. So, even measurements at a die pad may not be sufficient to determine whether data is received correctly. Luckily there are a number of accurate simulation and measurement tools available for signaling speeds exceeding 1 GHz.

Successful signal analysis requires an understanding of signal processing and channel component to silicon interactions. This precision comes at a price. The speed of board densification keeps accelerating. The value of evaluating a single case with great accuracy becomes limited to special cases. A complete design analysis with all its variation becomes a necessity. Urgency of answering the question of, "How do we know the board design is good?" continues to grow. Overcoming signaling analysis and measurement challenges is a daily event in electronic companies today.

Board assemblies have independent electrical characteristics that are a direct result of manufacturing and PCB design choices. It is those characteristics that interact with chips resulting in acceptable data transmission.
If we assume "good" chips are used, the quality of the board can be ascertained with just its electrical characteristics. In the same way short/open tests are used insure circuit are connected correctly and impedance testing is used to mange transmission line reflections, the addition of "clean signal interconnect" metrics and chip performance metrics can insure successful data transmission.

The subject of this paper is the specification of "clean signal interconnect" metrics that are pertinent to transmission on FR-4 and other board material that extend to signal speeds exceeding 1 Gigahertz. This is in contrast to board validation utilizing simulation.

Ecosystem Readiness

Board manufacture involves a number of different vendors and customers. **Error! Reference source not found.** is an illustration of the intricacy between various parties and their relation to electrical specification.

Table 1 Electrical Requirement Ecosystem

Aspects of Electrical Requirements	End User	OEM/ODM	PCB Assembler	PCB fabricator	Laminate supplier	Base Material Supplier
Electrical requirement	Meets performance expectations	BER	Signal quality connectivity and mounting	Impedance, trace loss, and connectivity	Finished Material Properties	Base Material Properties
Design	-	Assembled Boards	Assembled Boards	Bare Boards	laminates	Bulk material
Layout	-	Design	Approve			
Stackup and materials	-	May recommend	Design	Approve		
Design verification	-	Define rules and Simulate to verify Spec.	Practice rules	Stackup Planning Tools	Rely on materials	Various tools
Physical Test	-	System Test, BER	TDR, Loss. Opens, shorts test, ICT	TDR, Loss. Opens, shorts test	Rely on materials	Various VNA method

It is easy to lose sight of the real end goal and the relation to a satisfied end user. Does failing an impedance requirement suggest a given board will not work? Does passing an impedance requirement suggest a product is electrically OK? Will a low loss material insure system operation? Each is important in the compartmentalized world of design. There are a few areas where efficiency improvements would help reduce the cost and effort of designing and delivering quality products. Three boxes in **Error! Reference source not found.** involve assuring a design is sufficient (design verification) and associated testing assures this. Presently methods for assurance are complex and costly. So far design rules have proven to be of limited effectiveness since there are few proven ways to determine severity and tradeoff interrelations.

Historically TD simulation and verification are prior to productiztion. The FD metric for channel electrical specifications provides a low cost and effective alternative for the physical test and validation blocks highlighted in Table 1.

Traditional Simulation and Validation Strategies

Design Verification, Post Layout:

It is important to understand what a time domain (TD) simulation does. A single simulation can accurately predict an expected BER by taking in interconnect models and processing them with silicon transmitter and receiver, clocking performance, and transmission data. The results of a simulation are most often represented with a BER eye using one of the three methods described in [1]. The caveat is that the results apply to one set of buffers, one channel, and one set of clock characteristics. High model quality is required to produce good results.

Physical Test:
Finished board validation can use a similar BER metric to assure acceptable performance. There are also number of self test and stressing options available to electrically validate signal quality such as tools internal to silicon to margin timing and voltage. Sometimes an external pattern generator and Bit Error Ratio Tester (BERT) are connected to partially assembled boards to determine acceptable signal quality. Now what is the issue with this? It seems pretty straightforward. Performing this operation on one signal line on board is quite doable. However that is insufficient to qualify the design, as evident after root causing failing boards in the lab. The typical simulation methods suggest exquisite electrical modeling for all the signal nets, which is often time consuming, costly and even impractical in most designs. Good validation requires a significant investment in software test script and data analysis software. The costs of electrically testing partially assembled boards with BERTs and scopes are skyrocketing as we move in to the >1GHz era. The issue is that many of the best methods of simulation and validation/test only look at one line at a time. How can an entire product composed of hundreds or thousands of lines be tested. Factoring in manufacturing and environment conditions can add up to 20 factors per line that affect performance. There have been a number of time domain methods employed to mitigate the risk of variation which used Monte Carlo analysis, design of experiments (DOE) or other statistical methods. They are still expensive even though these methods reduce the problem from "n cubed" to "n" iterations. Even these DOE and other case variation methods can be victim to escapes due to resonance. It was show in [2] that indications of questionable designs can be detected in the FD even without substantial design analysis cases

The allure of single test perfection may produce a false sense of security when utilizing statistical methods to assure a successful product. Once risk is acknowledged the door is opened for other ways of thinking. On such method uses features in the frequency domain to create scalar metrics that can be used for electrical quality assessment. The story of these metrics starts with communication theory.

Communication Theory
Anecdotal examples can be explained with simple communication theory. A paraphrase [4] of the Shannon-Hartley theorem [3] suggests an upper bound on transferred data of a given channel.

[4]"Considering all possible multi-level and multi-phase encoding techniques, the Shannon–Hartley theorem states the channel capacity C, meaning the theoretical tightest upper bound on the information rate (excluding error correcting codes) of clean (or arbitrarily low bit error rate) data that can be sent with a given average signal power S through an analog communication channel subject to additive white Gaussian noise of power N, is:

(1) $$C = B \log_2\left(1 + \frac{S}{N}\right)$$

where

C is the channel capacity in bits per second;

B is the bandwidth of the channel in hertz (passband bandwidth in case of a modulated signal);

S is the total received signal power over the bandwidth (in case of a modulated signal, often denoted C, i.e. modulated carrier), measured in watt or volt^2;

N is the total noise or interference power over the bandwidth, measured in watt or volt^2; and

S/N is the signal-to-noise ratio (SNR) or the carrier-to-noise ratio (CNR) of the communication signal to the Gaussian noise interference expressed as a linear power ratio (not as logarithmic decibels)."

The reason for mentioning this fundamental work is to tie SNR to total noise power and consider this can be represented as additive white Gaussian noise (AWGN). Later discussions illustrate how to determine an equivalent sigma for an AWGN source which can be determined from the integration of total noise spectrum equating to total power.

Shannon makes no attempt to define BER. For binary transmission the bit error rate (ratio) BER can be defined in terms of SNR.[5]

(2) $$BER = \frac{1}{2}\sqrt{efrc(SNR)}$$ (SNR is expressed in terms of V^2_{total}/V^2_{noise})

Working this backwards, knowledge of BER can be used to determine a minimum SNR for the channel between devices.. Transmitter and receiver equalization increase SNR.Jitter and receiver acquisition uncertainty reduce SNR. Once transmitter equalization, receiver equalization, and jitter are taken into account, an initial estimate for a minimum channel SNR requirement may be determined. In other words adding SNR bonuses and penalties to the initial minimum SNR is a method to estimate the budget for channel SNR.

It is convenient to think of the total received power as an attenuation of transmitted power. In this way an integration of insertion loss convolved with normalized data patterns can be used to represent the "S" in the SNR in equation 1. A first order estimate may use the insertion loss at Nyquist frequency. However, as suggested later the normalized pulse height may be a better estimate. It is customary to represent both SNR and insertion loss in dB. Logarithmic identities then allow for arithmetic adjustment of SNR with dB penalties from insertion loss impairments. In the same way equalization, coding and other factors may provide an SNR bonus. An SNR bonus lowers the minimum SNR while an SNR penalty raises it.

Effective use of equation 2 often requires conversion of jitter expressed in UI to dB or a voltage^2 ratio. Figure1 is a simple depiction of a signal as a sine wave at a receiver and the same signal shifted by certain amount (TjUI) which approximates a the signal with a the maximum jitter. The right most graph illustrates a signal locus representing an eye closed by the shifted waveform.

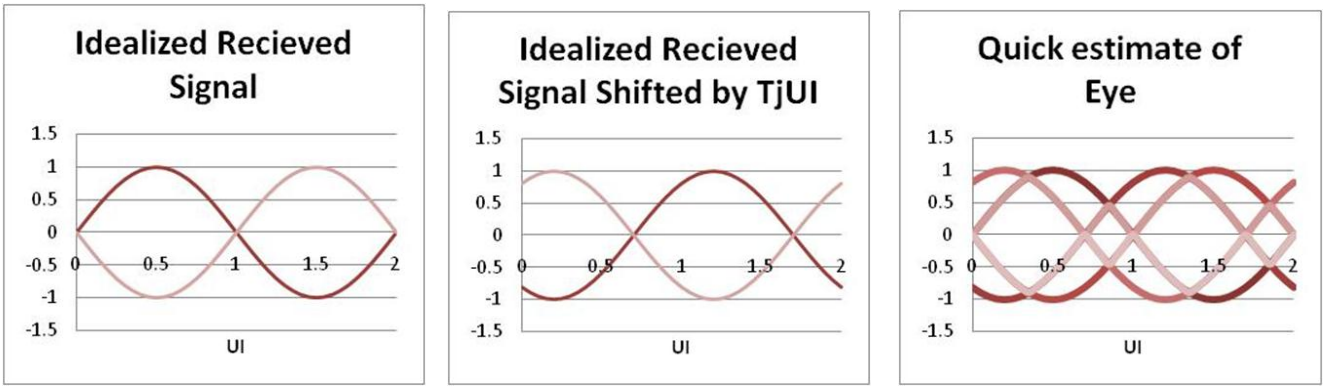

Figure 1 Simple Estimation: Converting Jitter to Loss

In that case the following is a geometric estimate of the SNR impact of total jitter expressed in dB.

(3) $$SNR_{penalty(Tj)} = -20 * \log10(\sin(\frac{1-Tj_{ui}}{2} * \pi))$$

Using equation 2 a BER of 10^{-12} requires an SNR greater than 8.5 dB. Using equation 3 a total transmit and receiv**e** jitter of 0.7 UI converts to a 6.9 dB loss penalty to SNR. That would mean the channel SNR would need to be greater than 8.5 dB + 6.9 dB = 15.4 dB. However other factors like receiver uncertainties were not considered here.

Channel Metrics

SNR is a frequency domain (FD) metric which can be used to judge channel performance. The task at hand is to convert from board design data into a board channel characteristics, namely channel SNR. Figure 2 shows how s-parameters may be

extracted from board and package layout files then processed to portray the FD SNR metric graphic representation for an entire DDR bus.

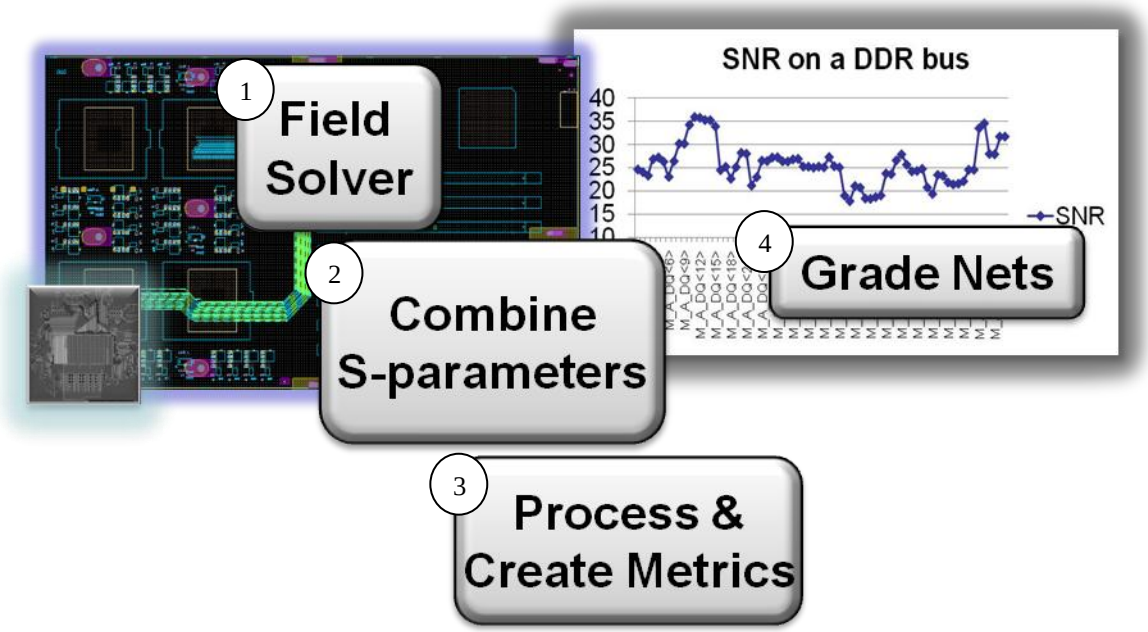

Figure 2 Usage model for clean signal interconnect FD metrics

DDR Frequency Domain (FD) Metric Analysis Example

Reduced complexity and faster evaluation of post layout verification positions the FD metrics approach to be preferred over traditional time consuming time domain (TD) simulations. The efficiency of FD metrics over TD metrics is discussed later. Figure 3 describes a real world example for a DDR interface. The Y axis corresponds to SNR and the X-axis corresponds to each signal net. The nets with low SNR are circled in red it is common to see this limit the bus performance on an un-tuned design. The board designers are surprised on how well the FD metric quickly diagnoses board designs that failing in operation. In this case the low SNR lines are attributed to poor vertical path with a fewer ground return via. The enabling feature is simplicity. The FD process in Figure 2 can be rapidly cycled a number of times by the layout engineer. A signal integrity engineer is not required for the iterations. The cause and effect relation to FD metrics empowers quick and efficient design iteration by the layout engineer.

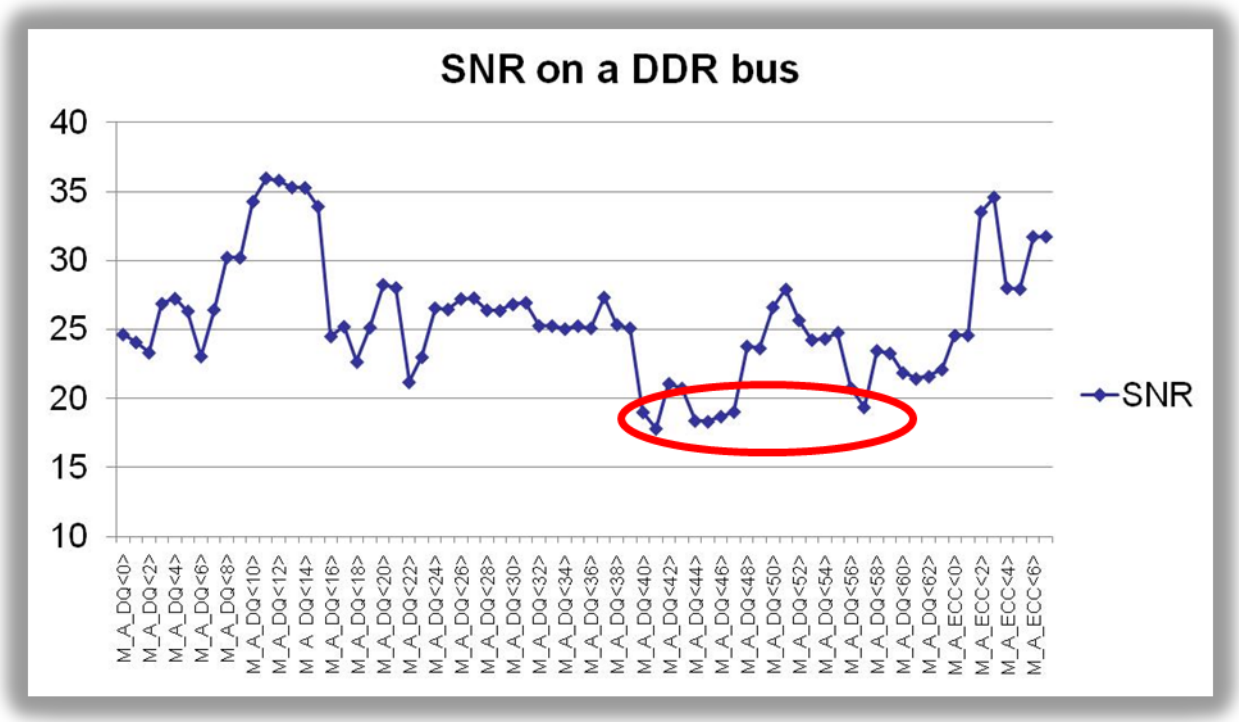

Figure 3 SNR (FD metric) Histogram for DDR routing on a PC Board

Root causing the low performing nets is faster and easier in FD than in TD simulation. Nets contributing to poor SNR are easy to identify with simple sorting methods.

Continuous Improvement of Layout, Using FD Analysis

Early on in the development this work was used to identify and rectify issues with a DDR design. A process was developed to input board and package layout files and produce s-parameters as in Figure 2. The s-parameters were processed with a tool that reported a simplified version of the crosstalk metric [6] which is one component of SNR. The results were impressive when used to analyze a failing product and compare crosstalk to a passing reference design.

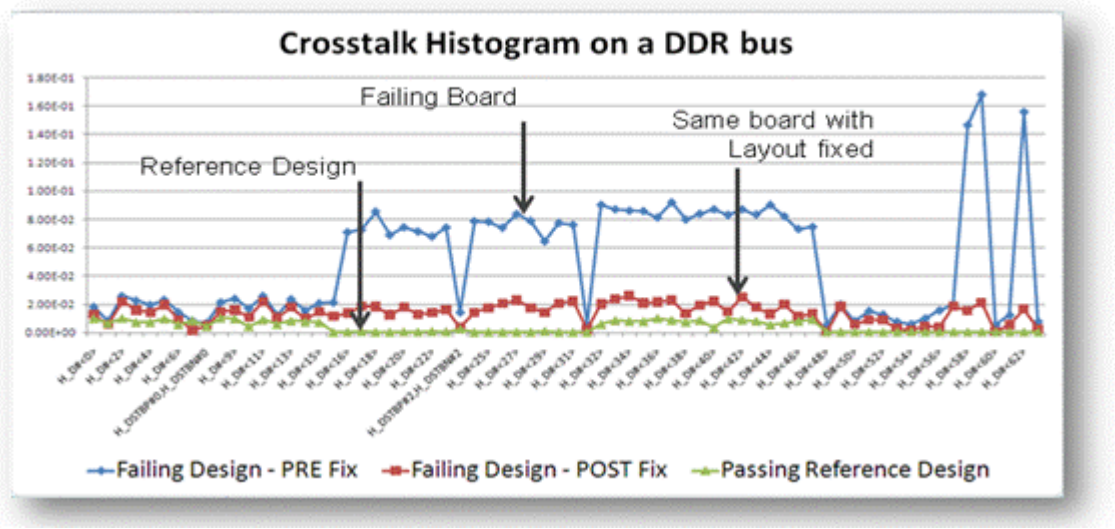

Figure 4 DDR Board Design Iteration Crosstalk Comparison

Figure 4 depicts a DDR network for 3 boards on the X axis and crosstalk power on the Y axis. It is easy to see that quite a few routes on the failing product board had high crosstalk. The layout was extracted and converted into representative s-parameters. A tool imported the s-parameters and produced the data on Figure 4. Layout engineers with limited SI skill ran the tool. After a number of iterations through the process, taking only a few hours per iteration, the layout engineer produced a good design, shown in red. Once these changes were incorporated into the board design the failures on the product board disappeared. The issue here was that one set of lines were all on a particular layer and consequent not referenced properly.
One discovery was that the s-parameters used for accurate FD Metrics do not appear to require the same quality level as those needed for an accurate time domain simulation. This could be attributed in part to an averaging nature of the FD parameters.

Computing SNR from Channel S-parameters

The interesting point taken from the previous section is that SNR can be defined in terms of peak signal and additive white Gaussian noise (AWGN). The challenge is then to convert the s-parameter of the channel to an AWGN equivalent and to also convert to the peak signal measured at the receiver. Initially average loss of the channel at the Nyquist frequency was considered adequate. Some analysis showed pulse height to be a much better indicator.[7] If only poor quality s-parameters those lacking some measure of causality, stability or passivity, are available the former loss metric may be used, but it will yield lower SNR values. The following section will detail how to acquire an effective AGWN sigma (RMS) for both insertion loss and crosstalk noise.

A channel may be represented with "thru" s-parameters (S21) and crosstalk s-parameters (S21xtk) which are functions of frequency. A differential example is illustrated using respective terminology of SDD21 and SDD21xtk. There are a number of modeling tools that may be used to convert a board design into s-parameters.

Healey [8] has shown that a crosstalk response can be spectrally colored using a power spectral weighting function (PWF) and may be defined as frequency product of data rate spectral content, the spectral content due to rise-fall time (T_{rf}), the spectral content due to receiver bandwidth ($frcv_{bw}$), and additionally a high pass factor (C_f) for coding or an AGC.

$$PWF(f_n) = SINC^2(f_n \cdot UI * \pi) \cdot \frac{1}{1+\left(f_n \cdot \frac{Trf}{0.2365}\right)^4} \cdot \frac{1}{1+\left(\frac{f_n}{frcv_{bw}}\right)^8} \cdot \left(\frac{f_n}{f_n + \frac{Cf}{UI}}\right)^2 \tag{7}$$

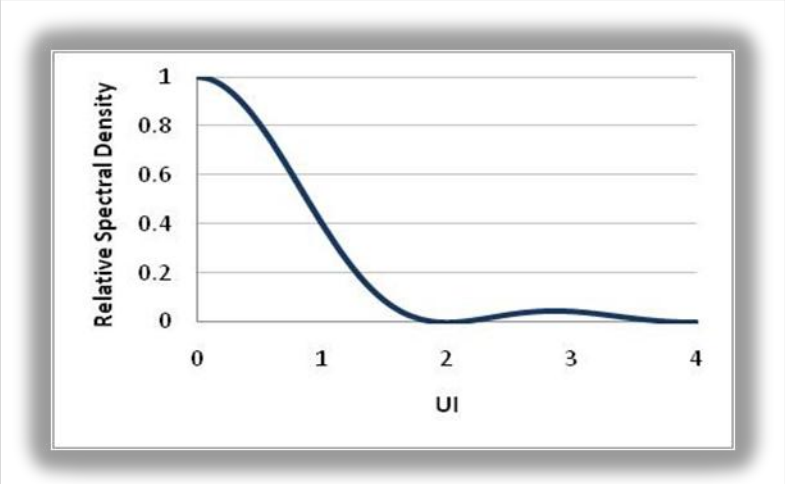

Figure 5 Example of Power Weighting Function for PRBS data

A dominant factor in (7) is the spectral constant of the PRBS data represented as the $sinc^2$ function as show in Figure 5.

Using the PWF is then possible to find the average crosstalk σ_{icn} across the spectrum relative to the data rate similar to that described in [8] by numerical integrating the sum of crosstalk power and converting back to an equivalent voltage using the square root.

(8) $$\sigma_{icn} = \sqrt{\frac{2 \cdot \Delta f \cdot \sum_{n} PWF(f_n) \cdot \sum_{x} A_x^2 \left| SDD21xtk_x(f_n) \right|^2}{F2 - F1}}$$

The Ax factor above apportions the crosstalk in relation whether it is near end or far end. In most situations far end crosstalk is derived from buffers that are in the same chip. For that case A_x is 1. Most other crosstalk may be considered near end and the factor for A_x would be the ratio of the maximum aggressor amplitude to the minimum amplitude of the victim's driver. The resultant voltage σ_{icn} is the voltage that would drive an AWGN source and could equivalently replace the crosstalk signals.

Crosstalk noise and noise due to reflections on the channel will combine to a total noise required for the SNR calculation. Determining the noise due channel reflection requires a few more steps before integration. As will be discussed later the insertion loss deviation (ILD) affects channel performance. A better parameter is insertion loss noise (ILN) which is similar but is actual deviation from the insertion loss fit and not the dB difference.

The insertion loss fit (ILfit(f))in dB is determined as follows:

(9) $$ILfit(f) = \alpha 0 + \alpha 1 \cdot \sqrt{f} + \alpha 2 \cdot f + \alpha 3 \cdot 10^{\frac{-8*\sin(\pi * f * UI)^2}{20}} + \alpha 4 \cdot 10^{\frac{-8*\sin(2\pi * f * UI)^2}{20}}$$

The form of the IL fit includes a transmission line contour($\alpha 0$, $\alpha 0$) and two feed forward equalizer contour terms($\alpha 3$, $\alpha 4$). Other types of fits are possible. The fit in (9) assume reasonable inter-symbol interference (ISI) is equalized due to insertion loss dispersion.

A set of frequency vectors are created for the means squared fit.

(10) $$\overline{F} = \left[1, \sqrt{f_n}, f_n, 10^{\frac{-8*\sin(\pi * f_n * UI)^2}{20}}, 10^{\frac{-8*\sin(2\pi * f_n * UI)^2}{20}} \right] \quad for\ n,\ \Delta f\ uniform\ samples\ f_1 < f < f_2$$

The coefficients for equation 10 are determined by combining the IL and the frequency vectors.

(11) $$\vec{\alpha} = (\overline{F}^T \cdot \overline{F})^{-1} \cdot \overline{F}^T \cdot \vec{IL}$$

Once the ILfit is determined the insertion loss noise, ILN, is calculated.

(12) $$ILN(f_n) = \left| sdd21(f_n) \right| - 10^{\frac{ILfit(f_n)}{20}}$$

ILN is ISI that will not be equalized.

It was once thought that insertion loss deviation (ILD), equation 13, was the metric to be used to represent ISI that is not equalized. This is because it gives an intuitive feel for performance as will be illustrated later. However, ILD does not contain the proper frequency weighting but still gives a quick intuitive feel and is a great diagnostic tool.

(13) $$ILD(f_n) = IL(f_n) - ILfit(f_n)$$

In a manor similar to determining σ_{icn}, the equivalent AWGN voltage is calculated for the integrated insertion loss noise σ_{iiln} as follows. where F2=? and F1=? and Δf =

(14) $$\sigma_{ii\ln} = \sqrt{\frac{2 \cdot \Delta f \cdot \sum_n PWF(f_n) \cdot ILN(f_n)^2}{F2 - F1}}$$

The integrated insertion loss and integrated crosstalk terms are independent.

The SNR for the channel is determined by combining the integrated insertion loss and integrated crosstalk terms with the pulse height.

(15) $$SNR = 20 \cdot \log\left(\frac{Pulse\_Height}{\sqrt{\sigma_{icn}^2 + \sigma_{ii\ln}^2}}\right) = 10 * \log\left(\frac{Pulse\_Height^2}{\sigma_{icn}^2 + \sigma_{ii\ln}^2}\right)$$

Often jitter will not scale as the data rate increases. In this case, equation 3 may be combined with equation 15 resulting in a more realistic SNR for the entire system expressed in dB.

(16) $$SNR = 20 \cdot \log\left(\frac{Pulse\_Height}{\sqrt{\sigma_{icn}^2 + \sigma_{ii\ln}^2}}\right) + \mathrm{SNR\_penalty(Tj)}$$

Consider that σ_{icn} and σ_{iiln} are average total power quantities. Noise from other power sources may be included in the RSS (root sum squared) such as from other buses, power induced noise, or un-anticipated measured noise converted to power. This way a scope measurement of the RMS power of noise could be used to estimate the impact to SNR.

This is supported by Parseval's theorem [9] which shows that total power measured by integration in the time domain (TD) is the same as total power integrated in the frequency domain (FD).

Summary

The described frequency domain (FD) metrics are simple and tolerant enough of error to fit in to an ODM/OEM and PCB assembler repertoire of service level agreements. In the future this analysis could be a part of, or tied to, routing tools. Historically most of these tools have rules checking routines and report violations. However it is often an extensive process to determine severity of violations. FD scalar metrics holds the promise of estimating the severity of design violations and provide a signal integrity map of a board design.

Frequency domain metrics of SNR, insertion loss, and noise factors have been shown to be an attractive and efficient tool for reducing board design time and cost which could dovetail with tradition time domain channel analysis. They can stand on its

own electrical merits without needing buffer models, interface specification etc. Electrical validation (channel analysis) and test of a product in the time domain is a time consuming and costly proposition. The focus for this effort could in the future be limited to determining FD metric criteria for downstream design and manufacture.

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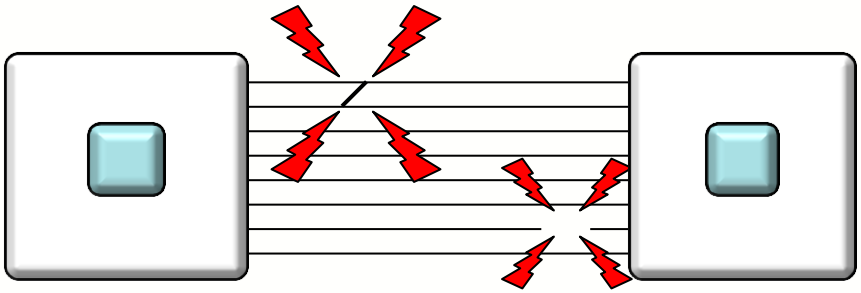
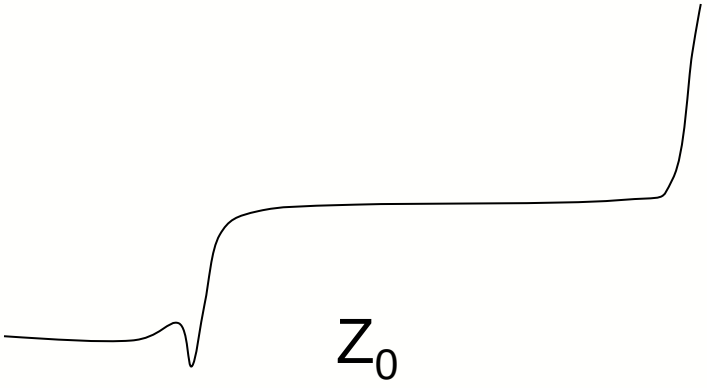
Agenda

- Digital Design & Quality Assurance
- Time Domain, Frequency Domain
- Frequency Domain Quality Metrics
- Frequency Domain Analyses (FDA)
- FDA in the PCB Ecosystem
- Summary

Electrical Manufacturing Board Quality: Circa 2000

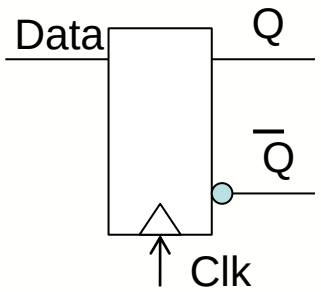
- Nets connected correctly
- Part are mounted correctly
- Impedance is with in expectations

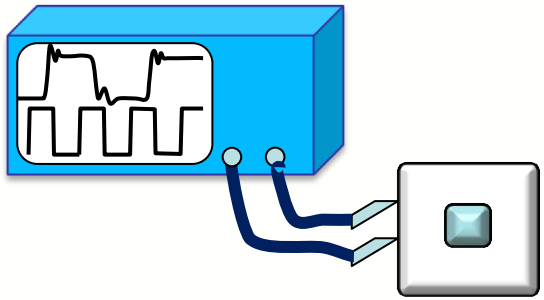


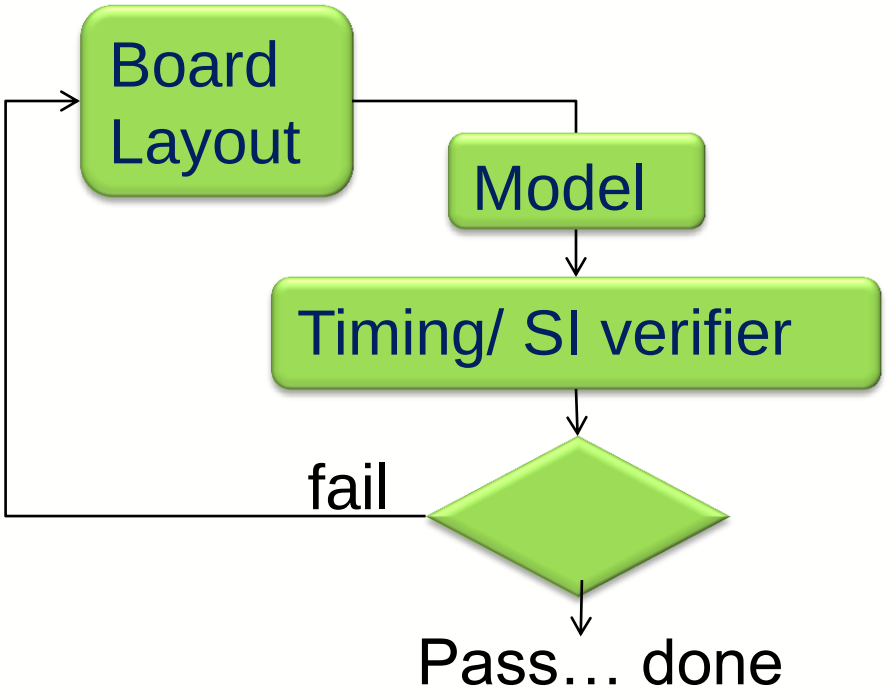


Design Quality: Circa 2000

- Design assures signals are received
- Set up & hold are verified
- Simulation and scope captures are the tools
  - Time Domain (TD) tools

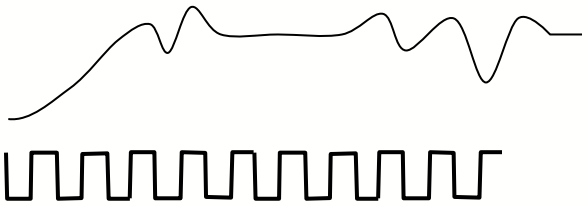


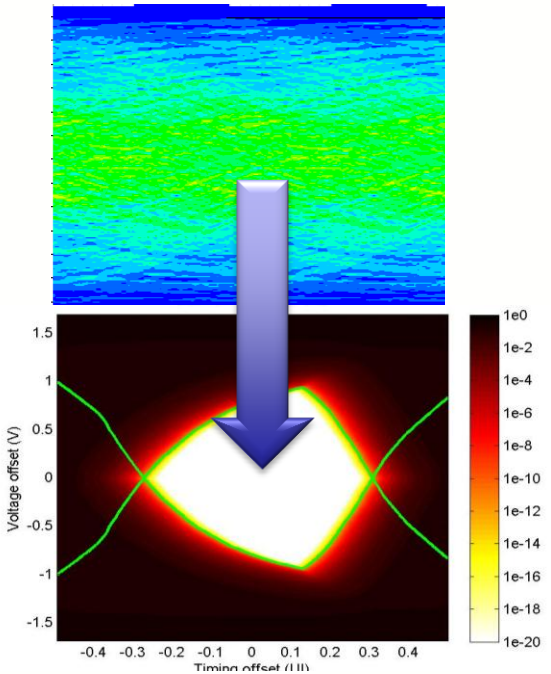




The Gigahertz Era

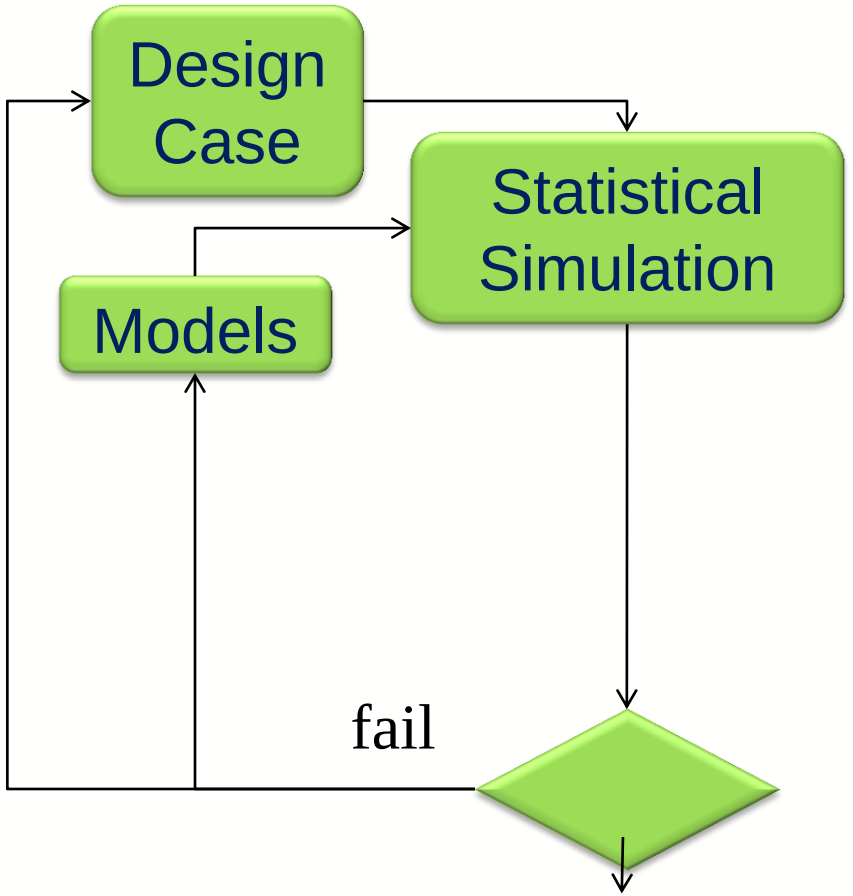
- Settling times are greater than the bit time
- The observed signals at pins of a device are not representative of signal at the die pads
- The eye at the die pad may be closed
- Sophisticated Time Domain (TD) signal processing is required to interpret signals
- Design Quality
  - Bit Error Ratio(BER) dominates the “end game”
  - Observation of billions of bits is required





TD Design Tools for Gigahertz Speeds

- The flow is not that different from years past
  - Only sophistication has changed
  - Full wave 3D models for connectors and via
  - Passive, stable, and causal transmission line models
  - Buffer models may be part of the simulator for equalization and clock data recovery
  - More silicon and board parameter interact



TD Analysis for GHz Speed:

Features/Parameters Interact, Complexity^3

Board feature interaction

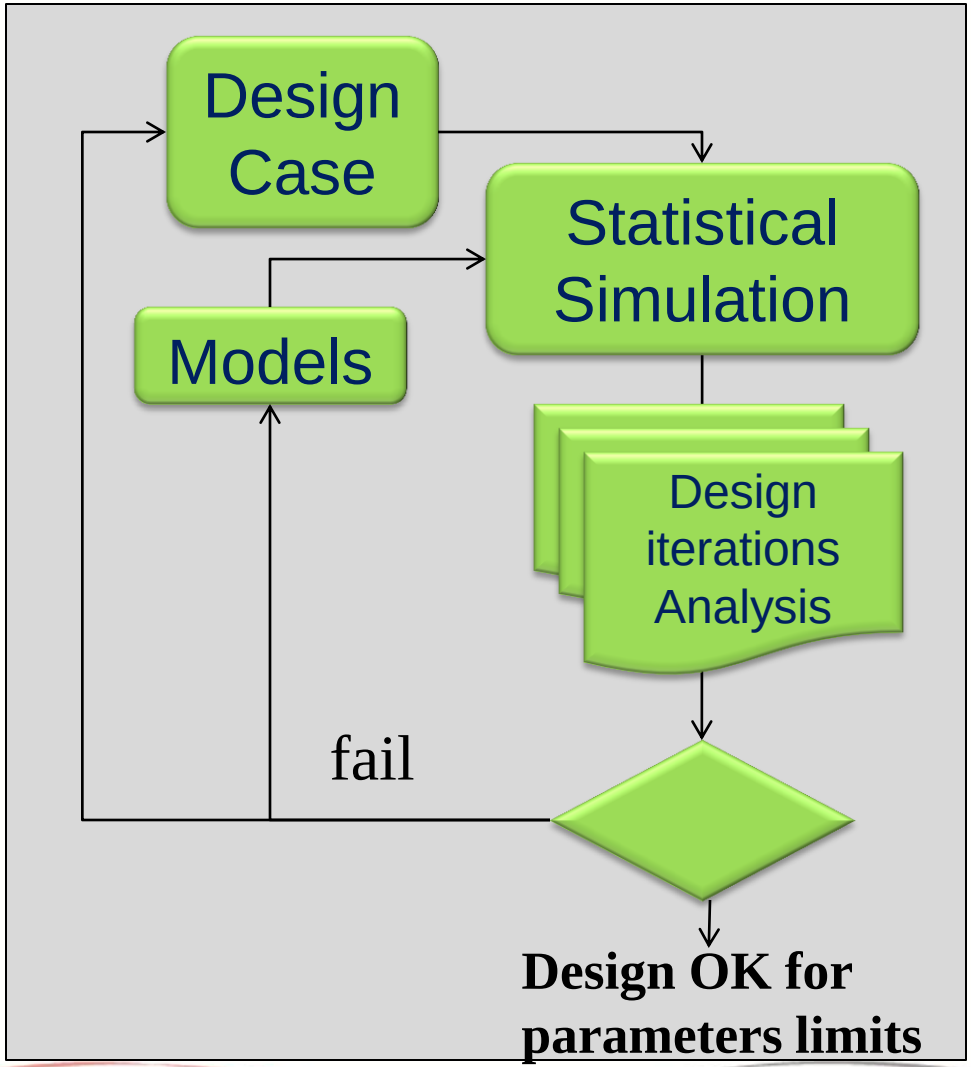
- Routed segment impedances
- Designs have many lengths and segments.
- Via design and placement
- Loss
- Connectors
- Package features
- Socket features

Chip feature interaction

- Equalization
- Buffer loading

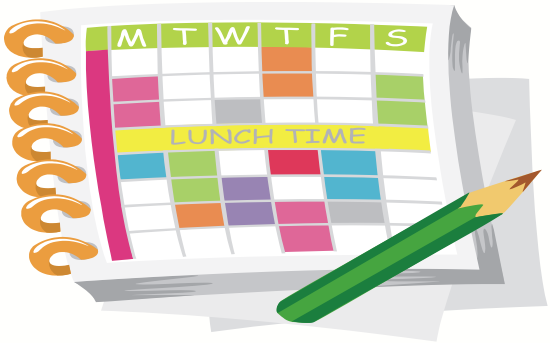
Tools to manage interaction

- Design of Experiments
- Monte Carlo
- Susceptible to misses/escapes



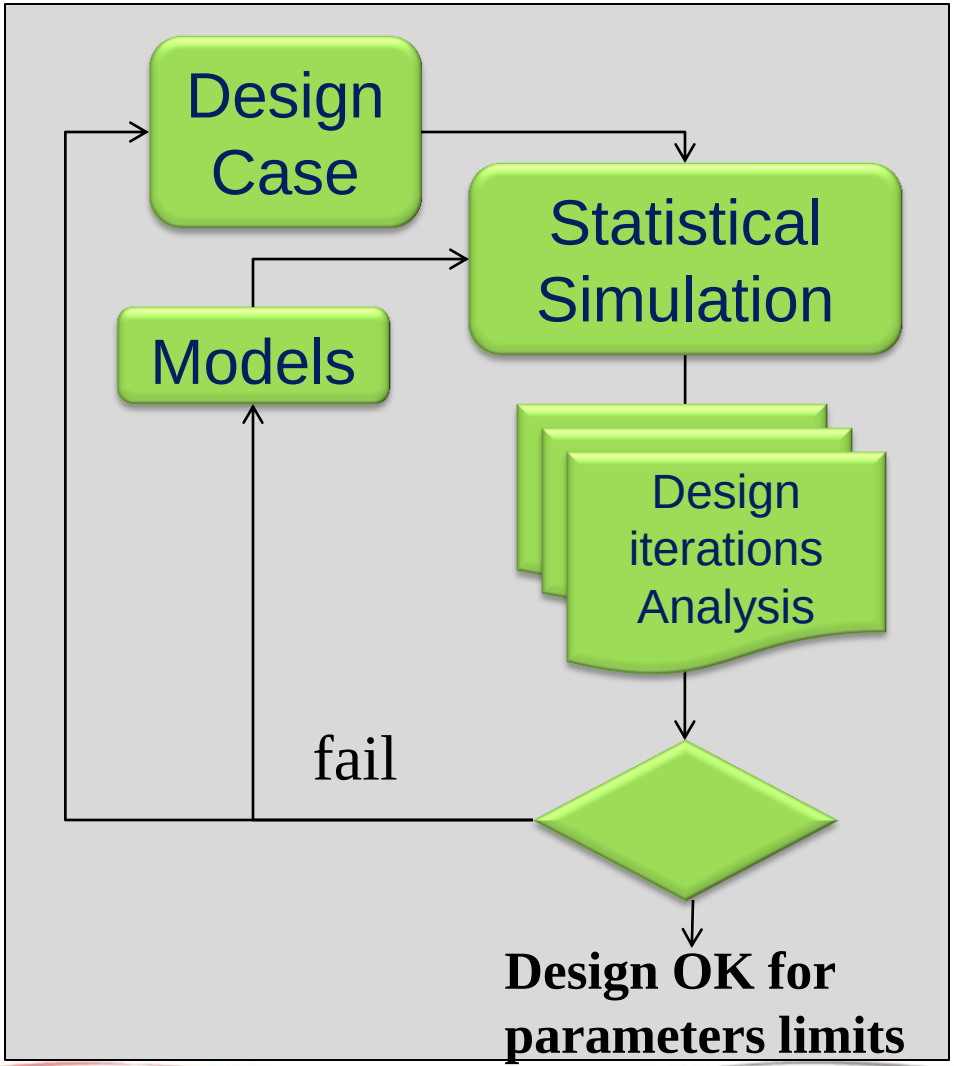
Business Impacts

Expertise



Time

Expense



Frequency Domain Design Tools for Gigahertz Speeds

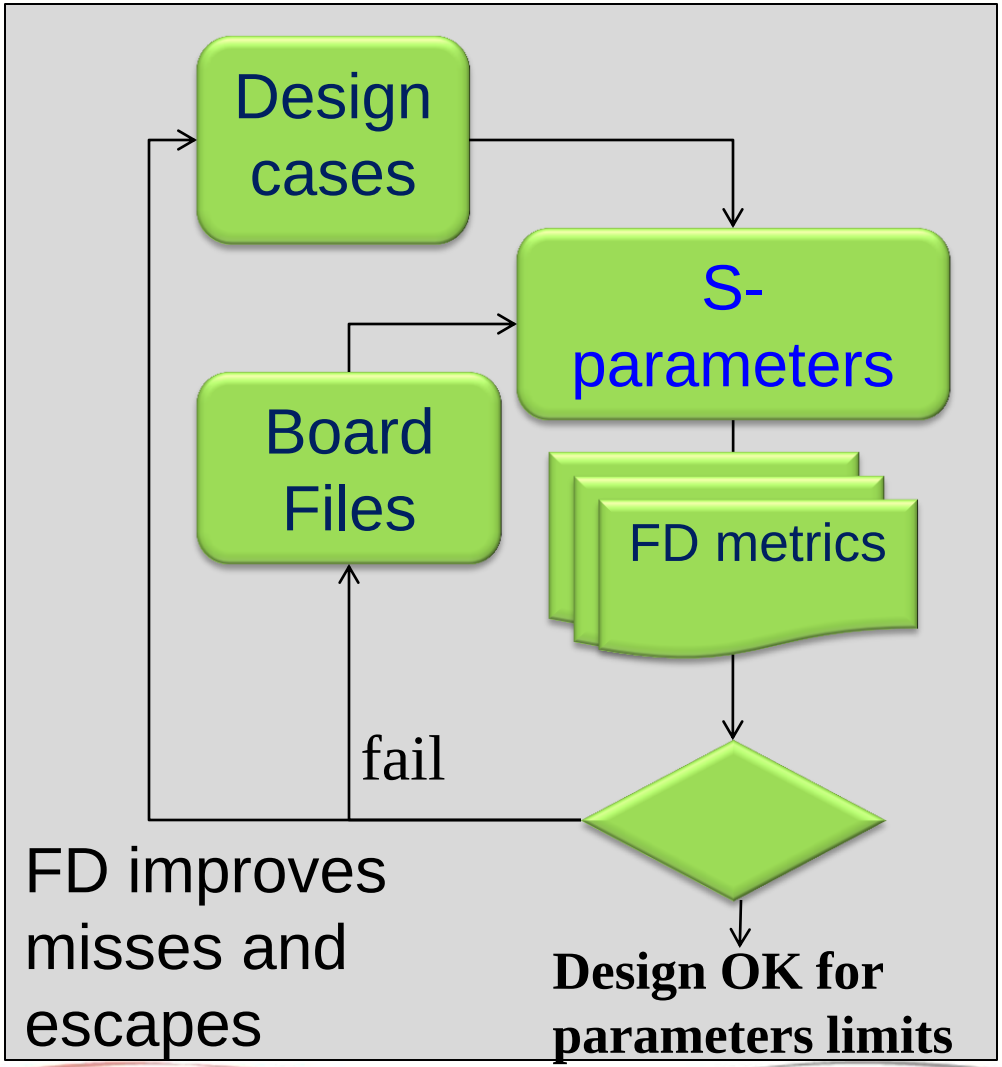
Expertise:

Layout Engineer
Makes Signal
Integrity Decisions

Time:

Hours not days

Expense:



Frequency Domain Metrics

- SNR is closely tied to Bit Error Ratio (performance)
- It has its roots in signaling and equivalent additive white Gaussian noise (AWGN) sources
- Task at hand is to convert a board design to a electrical quality metric

Bit Error Ratio (BER) and SNR

End User	OEM/ODM	PCB Assembler	PCB fabricator	Laminate supplier	Base Material Supplier
Meets performance expectations	**BER**	Signal quality connectivity and mounting	Impedance, trace loss, and connectivity	Finished Material Properties	Base Material Properties

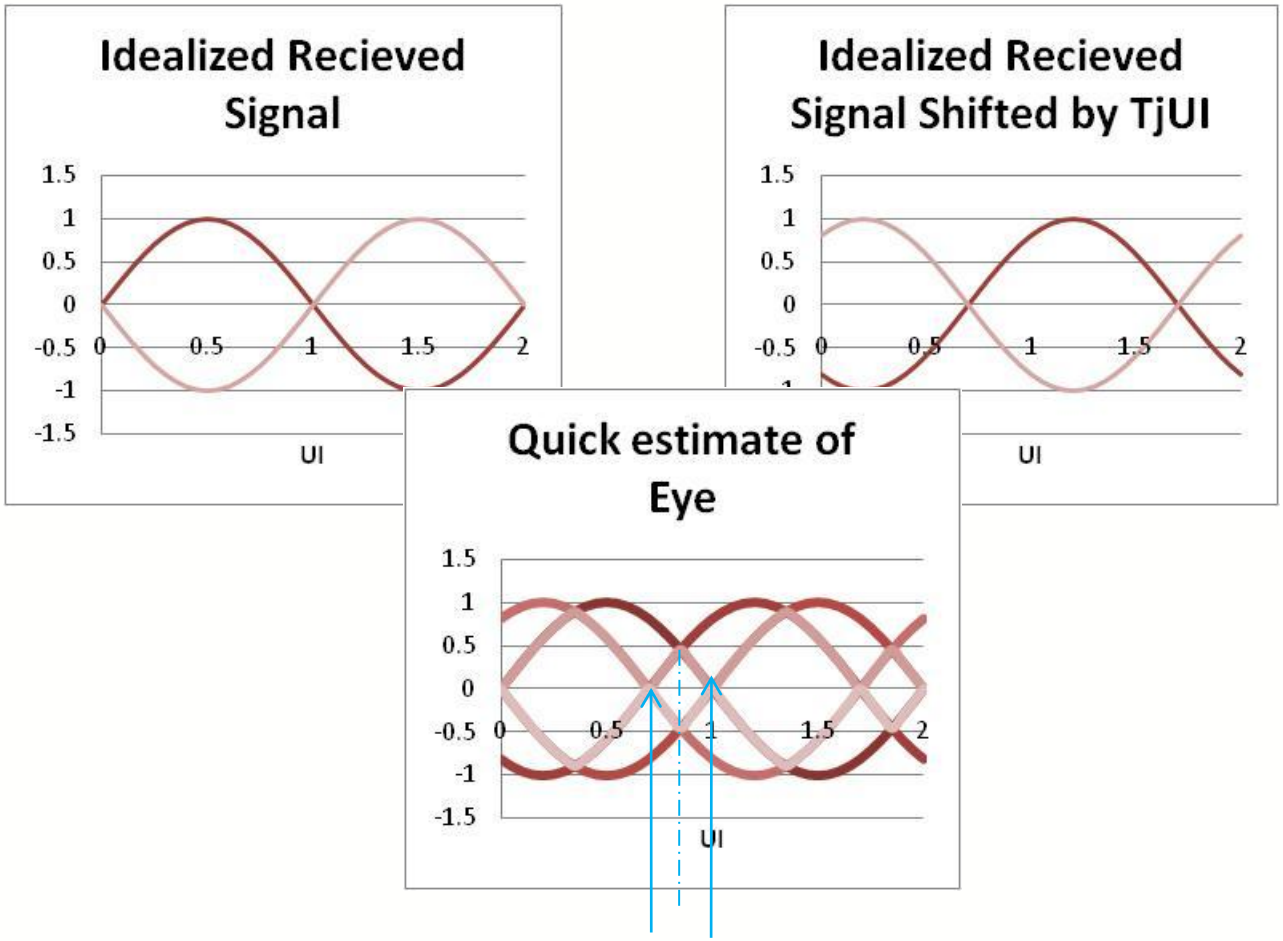
BER is determined by the SNR (signal to noise ratio)

$$BER = 1/2\sqrt{efrc(SNR)}$$

Signal-to-Noise (SNR) Requirement

- SNR is shared between
  - Channel
  - Electronics (silicon/chips)
  - Budgeting is possible when loss and SNR are expressed in dB
    - Ratios and products of logarithms arithmetically combine
- Many buses specify a maximum BER or 1e-12
- Working backward an SNR of 8.5 dB is required to support the BER of 1e-12
- The 8.5 dB does not accounting for clocking and buffers

Jitter as SNR Penalty



$$SNR\_penalty(Tj) = -20 * \log10\left(\sin\left(\frac{1 - Tj\_ui)}{2} * \pi\right)\right)$$

Channel SNR Floor

- 0.7 UI assigned to the total jitter equates 6.9 dB
- Minimum Channel SNR is 15.4 dB (8.5 dB + 6.9 dB)
- Does not include other silicon contributions

Developing Channel FD Metrics (S,N, SNR)

- (N) RMS voltage equivalent of power noise from:
  - Crosstalk
  - Reflections
  - Has the form:

$$\sigma = \sqrt{\frac{2 \cdot \Delta f \cdot \sum_{n} PWF(f_n) \cdot Quantity^2}{F2 - F1}}$$

Power Weighting Function

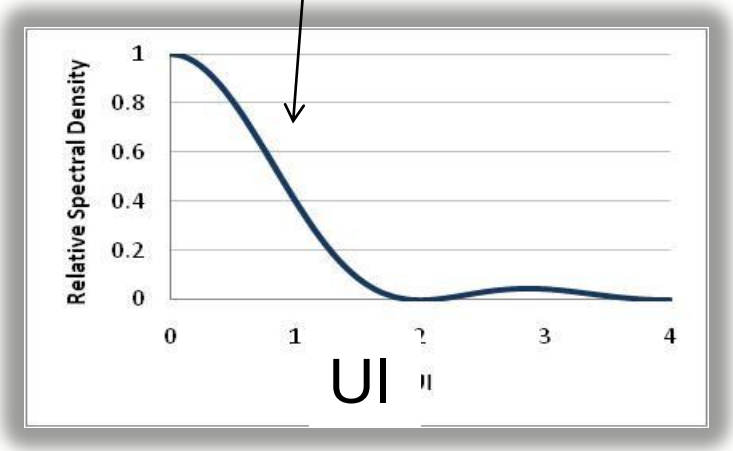
    - Tends to average imperfections because summing/averaging operation
- (S) Signal Power
- SNR determined from signal and noise power

Crosstalk is One Noise Source

- Crosstalk noise – sum of the power for all crosstalk terms

$$\sigma_{icn} = \sqrt{\frac{2 \cdot \Delta f \cdot \sum_{n} PWF(f_n) \cdot \sum_{x} A_x^2 \left| SDD21xtk_x(f_n) \right|^2}{F2 - F1}}$$

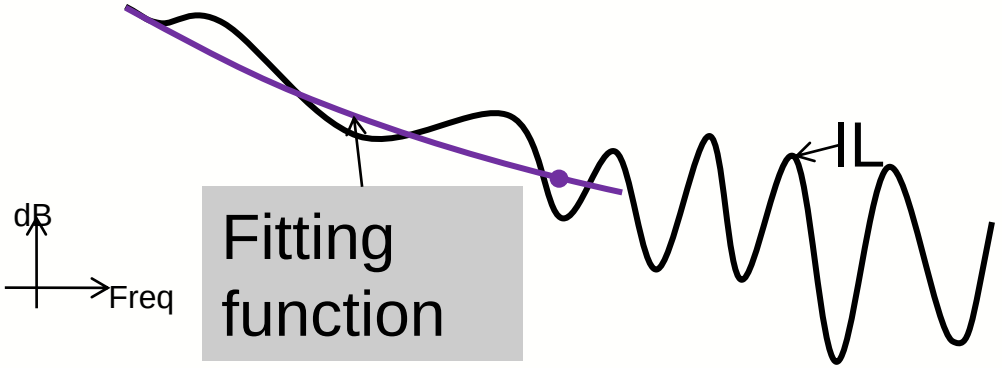
- Power averaged between F1 and F2



- SDD21xtk are crosstalk s-parameters reference to a victim
- Far and near end crosstalk is scaled by the Ax term

Reflections as Another Noise Source

- Find an average Insertion loss fit, ILfit



- Determine difference, which is insertion loss noise (ILN)

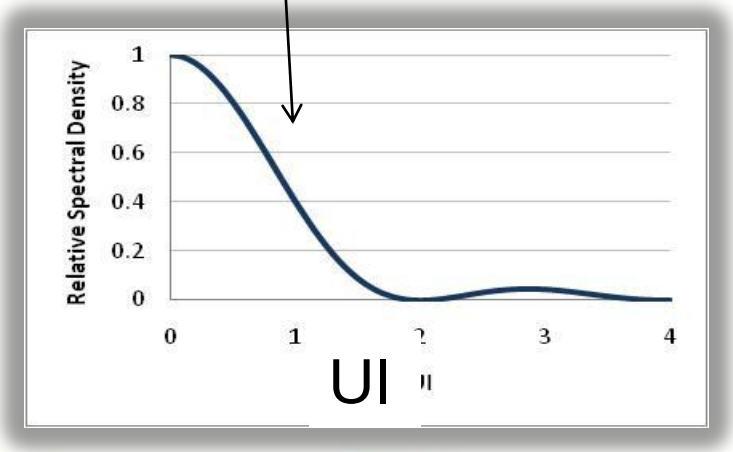
$$ILN(f_n) = \left|sdd21(f_n)\right| - 10^{\frac{ILfit(f_n)}{20}}$$

Equivalent Reflection One Noise Source

- Integrated Insertion loss noise (IILN)
  - Average power in the ISI that cannot be equalized
  - It too is colored by the spectrum of PWF

$$\sigma_{ii\ln} = \sqrt{\frac{2 \cdot \Delta f \cdot \sum_{n} PWF(f_n) \cdot ILN(f)^2}{F2 - F1}}$$

- Power averaged between F1 and F2



Total SNR

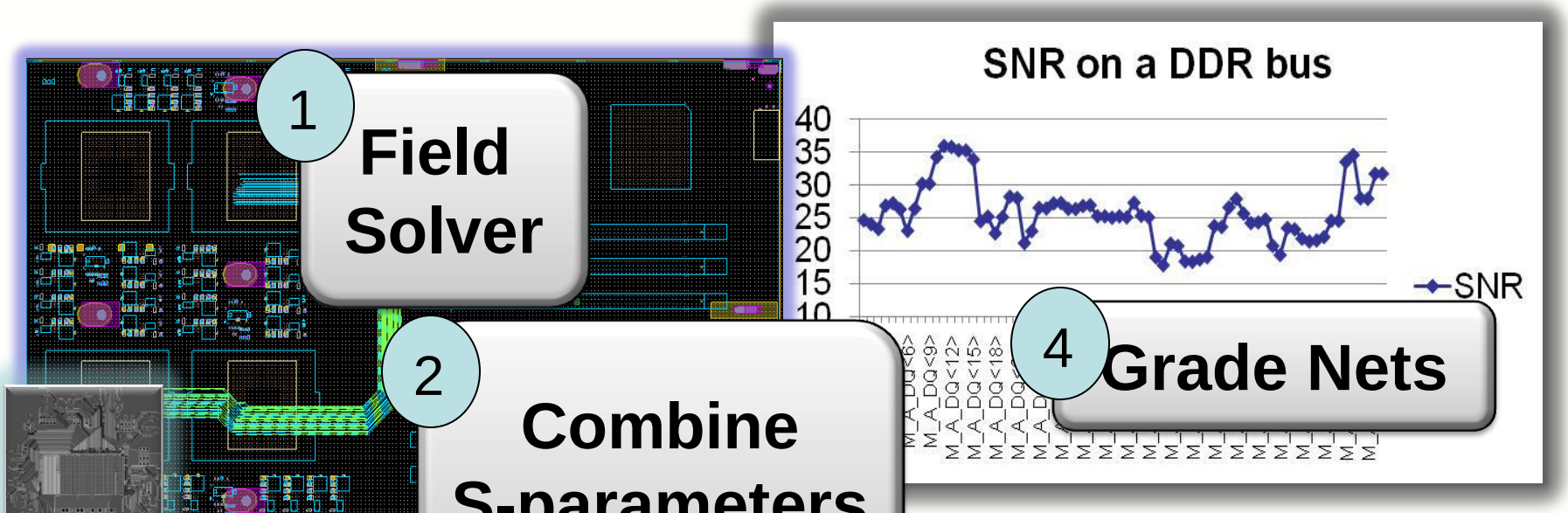
- The channel SNR can be determined from pulse height or loss at the Nyquist frequency and the noise sigma

$$SNR = 20 \cdot \log\left(\frac{Pulse\_Height}{\sqrt{\sigma_{icn}^2 + \sigma_{ii\ln}^2}}\right) = 10 * \log\left(\frac{Pulse\_Height^2}{\sigma_{icn}^2 + \sigma_{ii\ln}^2}\right)$$

- Or adding the jitter term, a system SNR may follow

$$SNR = 20 \cdot \log\left(\frac{Pulse\_Height}{\sqrt{\sigma_{icn}^2 + \sigma_{ii\ln}^2}}\right) + \mathrm{SNR\_penalty(Tj)}$$

FD Analysis using SNR



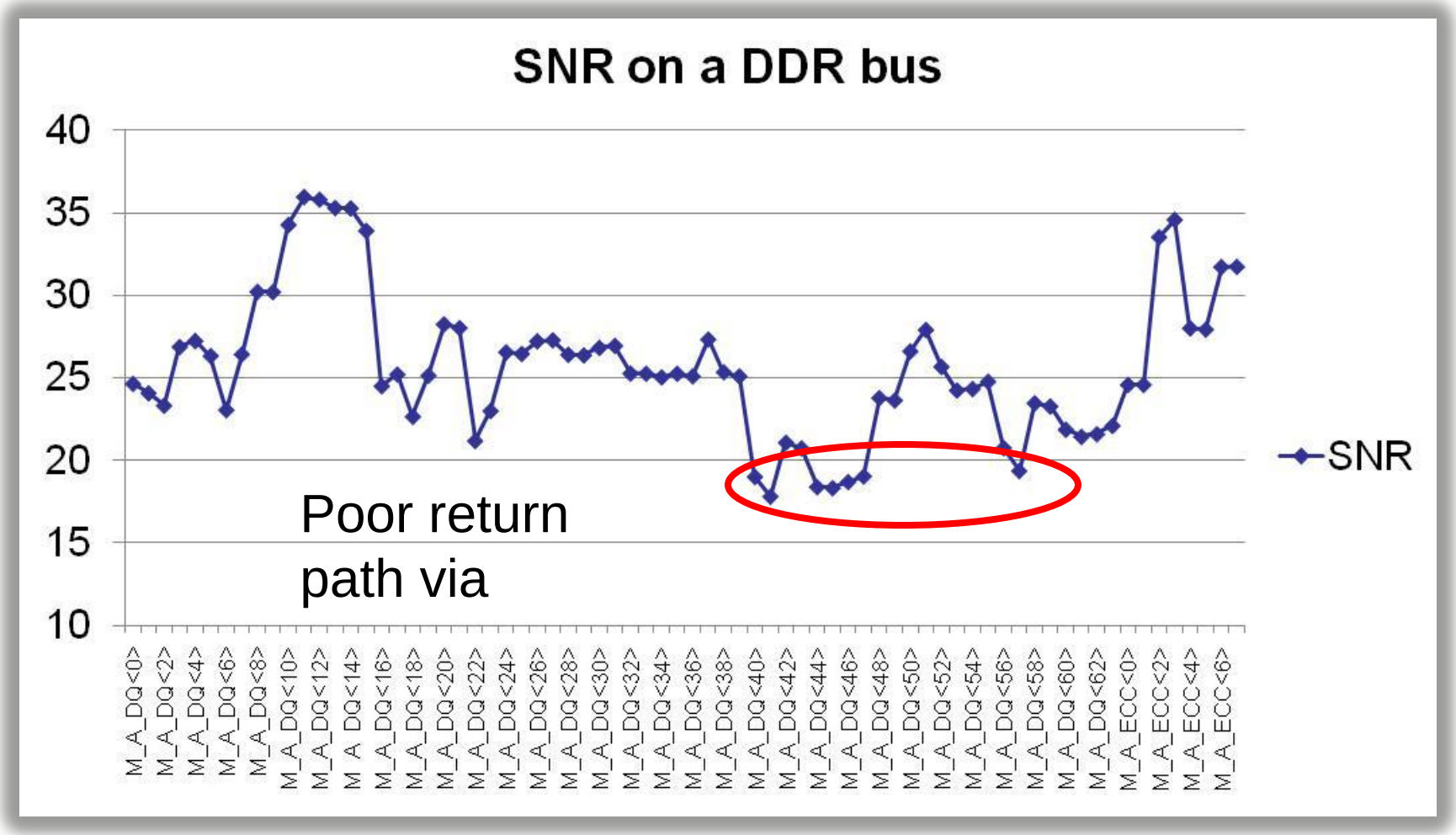
1 **Field Solver**

2 **Combine S-parameters**

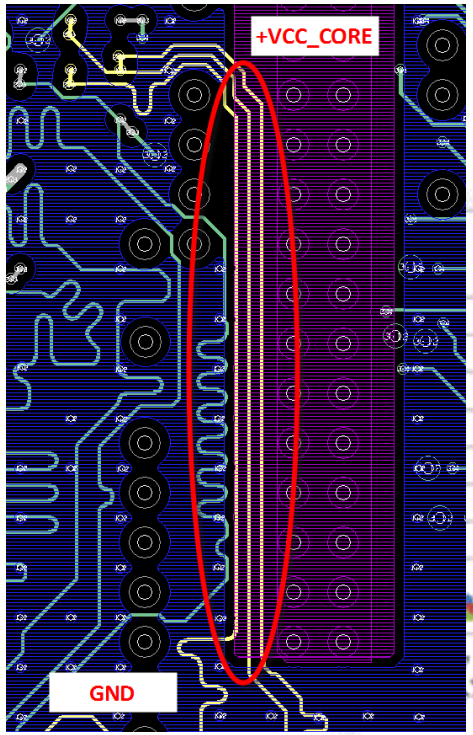
3 **Process & Create Metrics**

4 **Grade Nets**

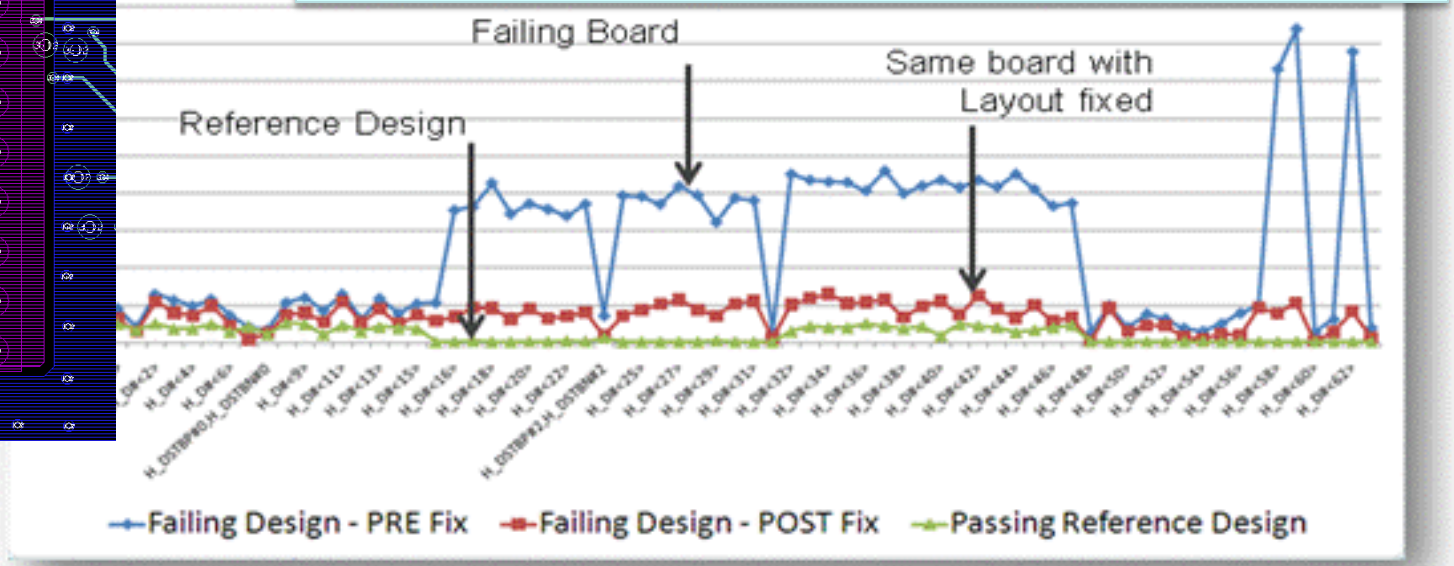
DDR Channel Quality using FDA



DDR Channel Design using FDA

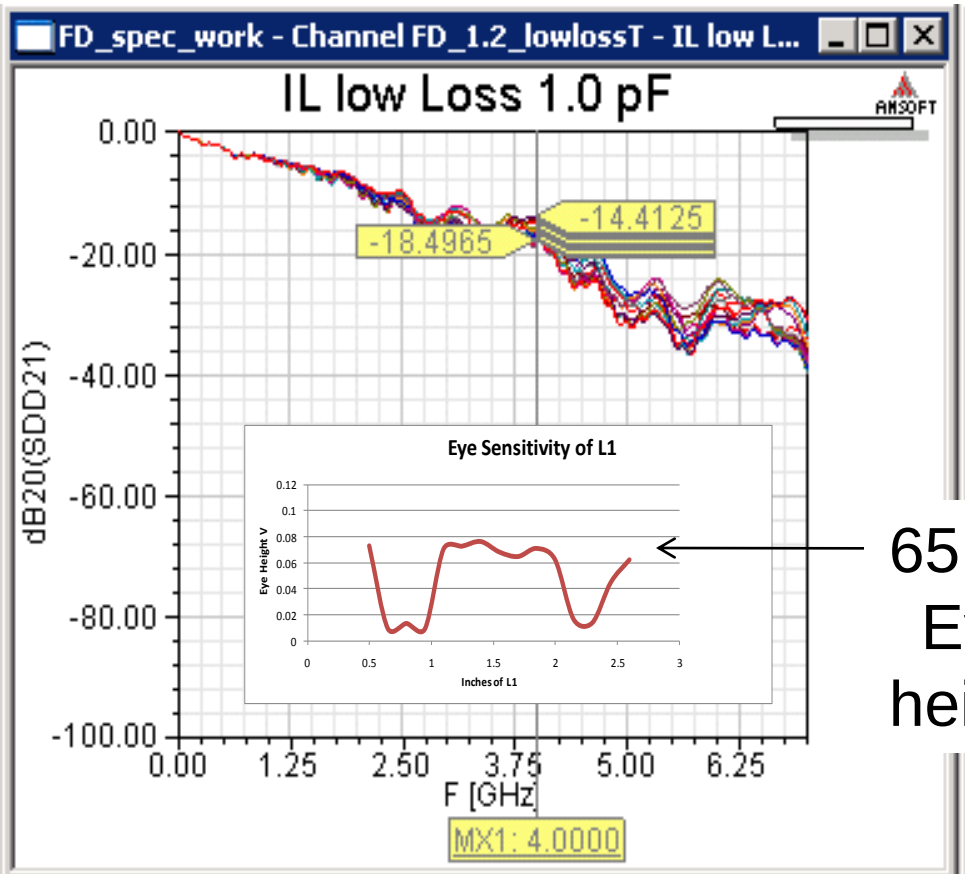


- Outliers Identified
- Signal reference changed and fixed
- Failures disappears after fix
- Only a few hours per iteration

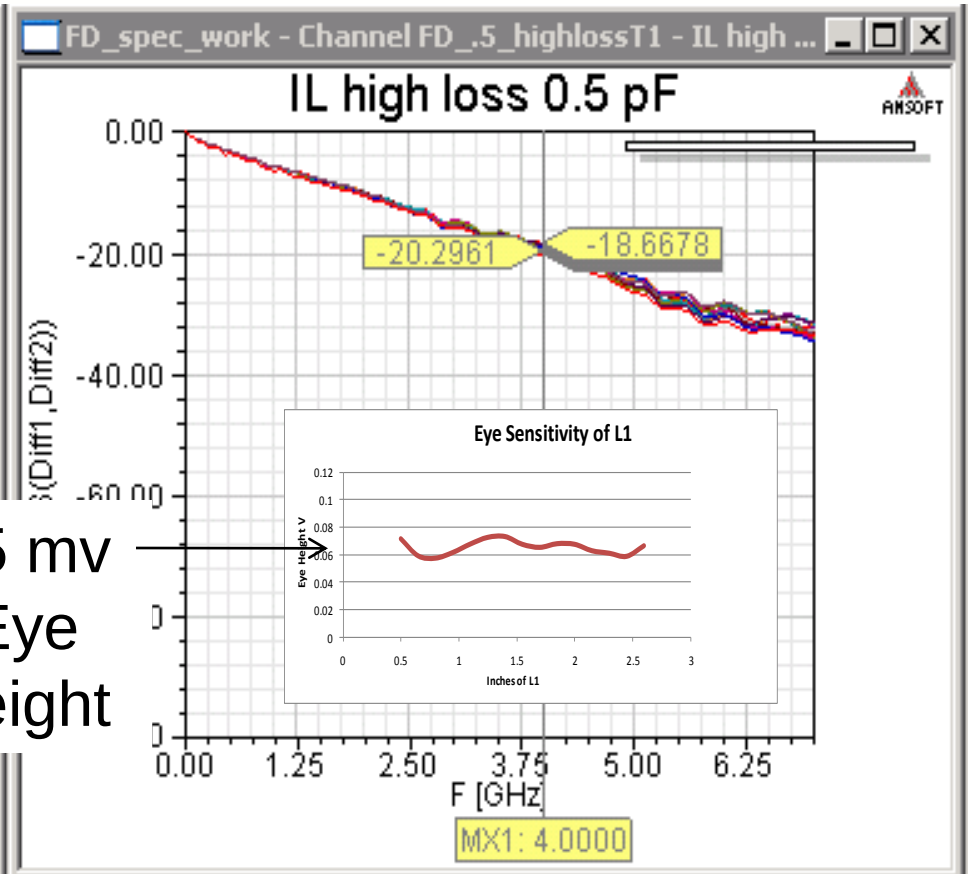


Channel Comparison Using FDA

FDA take the place of complete TD sweeps required to evaluate these 2 different designs

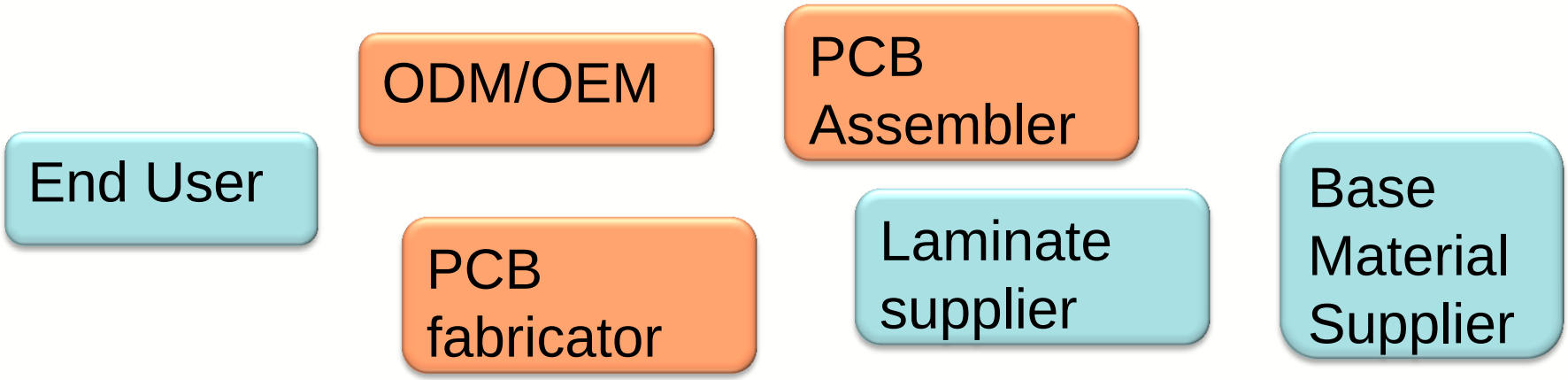


65 mv Eye height



PC Board Ecosystem

- Each player in the board ecosystem has their own perspective
- There are implied and explicit service level agreements between players
- All are required to meet end user expectations
- High speed signaling stresses OEM/ODM, PCB fabricator, PCB fabricator expectations



TD Design Qualifications

Aspects of Electrical Requirements	End User	OEM/ODM	PCB Assembler	PCB fabricator	Laminate supplier	Base Material Supplier
Electrical requirement	Meets performance expectations	BER	Signal quality connectivity and mounting	Impedance, trace loss, and connectivity	Finished Material Properties	Base Material Properties
Design	-	Assembled Boards	Assembled Boards	Bare Boards	laminates	Bulk material
Layout	-	Design	Approve			
Stackup and materials	-	May recommend	Design	Approve		
Design verification	-	Define rules and Simulate	Practice rules	Stackup Planning Tools	Rely on materials	Various tools
Physical Test	-	System Test, BER	TDR, Loss. Opens, shorts test, ICT	TDR, Loss. Opens, shorts test	Rely on materials	Various VNA method

FD Design Qualifications

Aspects of Electrical Requirements	End User	OEM/ODM	PCB Assembler	PCB fabricator	Laminate supplier	Base Material Supplier
Electrical requirement	Meets performance expectations	BER	Signal quality connectivity and mounting	Impedance, trace loss, and connectivity	Finished Material Properties	Base Material Properties
Design	-	Assembled Boards	Assembled Boards	Bare Boards	laminates	Bulk material
Layout	-	Design	Approve			
Stackup and materials	-	May recommend	Design	Approve		
Design verification	-	**FD metric**	**FD metric**	Stackup Planning Tools	Rely on materials	Various tools
Physical Test	-	**FD metric**	**FD metric**	TDR, Loss. Opens, shorts test	Rely on materials	Various VNA method

Summary

- Rigorous development of FD metrics have roots in communication theory
- FD metrics are simple to get for a design
- FD analysis efficiently predict design goodness, without extensive simulation
- FD Metrics Improve Efficiency and Reduce Costs in the PCB Ecosystem