High Density Packaging User Group – Pb-free Materials 2 Project Materials Testing of PWB Substrates to Establish Variability of Construction, Estimate Thickness and Determine Survivability through Lead Free Assembly.

Bill Birch, PWB Interconnect Solutions Inc.
Jason Furlong, PWB Interconnect Solutions Inc.

Abstract
An important element of the High Density Packaging Users Group (HDPUG) Consortium investigation into the reliability of printed wiring board (PWB) constructed with 20 different Pb-free materials was to understand whether the materials were negatively impacted by the six reflow cycles to 260°C. A new electrical test methodology and associated automated test equipment have been developed to non-destructively measure and compare specific attributes of the PWB's material construction that identify whether material degradation (delamination) was present. Additional features of the methodology create product construction baselines which confirm that each individual test vehicle was constructed with the same material properties, thickness and glass/resin ratio, all related to changes in dielectric material properties. The data enables the user to estimate the variability of thickness for each dielectric layer within the product construction. The study contained a total of 27 different constructions; built by three high-end Asia based PWB manufacturers. The Interconnect Stress Test (IST) test vehicles were designed to combine attributes to quantify both via reliability and materials analysis testing. Via reliability results and the statistical correlation between IST and air to air oven testing is reported in a separate paper [5]. Using two specifically designed IST coupons with via-to-via spacing of both 0.040" (1mm) and 0.032" (0.8mm), all products were constructed with 20 layers, laminated to an average of 0.115" (2.92mm), drilled with a 0.010" (0.254mm) vias, producing an aspect ratio of 12 to 1. Seven of the 20 materials were manufactured with two different glass styles and resin contents. The materials were tested on the two coupons types, both as built (non-stressed) and after 6X Pb-free (260°C) reflow (stressed). Twenty different material types were tested, which included eight high Tg, filled FR4 materials, six high Tg halogen-free FR4 materials, and six high speed materials. Correlations between the electrical testing and traditional micro sections for the presence of material damage and confirmation of dielectric thickness are detailed.

Introduction
A previous HDPUG consortium study identified significant challenges in complex multilayer applications with printed wiring board material's ability to survive multiple exposures through Pb-free assembly reflow [1-3], specifically related to the detrimental impact of the higher temperatures on plated through hole (via) reliability and the onset of material delamination. One of the key influences previously noted was the effect of via to via spacing on the materials ability to survive through Pb-free assembly [1].

Additionally, in an earlier study, difficulties were experienced in correlating IST to air-to-air thermal cycle testing [1], the original belief was associated to fundamental difference in test vehicle design, there is now an increasing understanding that material degradation can confound the cycles to failure due to either the initiation of damage to the plated copper barrel, or creating stress relieving effects to the vias during thermal cycling, both conditions can impact the ability to correlate between different accelerated tests methods.

The industry has recently released improved materials that better address Pb-free assembly applications; there was much interest in the consortium to evaluate these materials. Alcatel-Lucent designed the material reliability test vehicle used in this study; "MRT-3" has introduced multiple upgrades to previous revisions. Changes to the test vehicle included 1) Adding a specific area for Dynamic Mechanical Analysis (DMA) testing; 2) Implementing an innovative IST coupon that utilizes capacitance measurements to determine product construction, estimate dielectric spacing, and determine if material damage was caused during assembly (the subject of this paper); 3) Consistency in the geometries and layout between the IST and air-to-air thermal cycle test vehicles. 4) Expanding the focus of the IST and air-to-air thermal cycle designs to address via to via spacing in more detail; 5) Adding a custom designed IBM style WIC-20 coupons for material analysis investigations and moisture sensitivity testing [4].

The goals for this testing were to;

- Characterize the performance of a number of recently released Pb-free compatible materials using the MRT-3 test vehicle
    - Focusing on 20 layer constructions only, with some materials produced with both 58% and 69% resin content configurations
    - Identify materials that are robust through Pb-free assembly reflow designed with 1mm and 0.8mm via to via spacing
    - Include new High Tg halogen free materials
    - Include mid-level electrical performance FR4 and very high speed materials
- For the FR4 and halogen free materials, focus on those that are expected to be more thermally robust and have better electrical performance characteristics while remaining cost effective materials.
- Evaluate the IST coupon design to determine if the methodology provides an effective non-destructive capability for understanding how to use capacitance measurements to confirm consistency of product construction, dielectric thickness and identify the presence of material damage after Pb–free assembly.
- Determine the effectiveness of the improved IST coupon heating element's distribution used throughout the construction (not just on the traditional outer layers).
    - With the anticipation that this would enhance the ability to achieve a statistical correlation between the IST and the air-to-air thermal cycling methods.
- Understand, using the WIC-20 coupons, the effect of moisture on material survivability through Pb-free assembly.

This paper reports the results of electrically quantifying the consistency of each material from a perspective of variability of supplied materials used in each product construction, the ability to non-destructively estimate the dielectric thickness and determining the presence of material damage through Pb-free assembly reflow. Reported separately are moisture sensitivity testing [4], the Plated Through Hole Reliability with High Temperature Lead Free Soldering [5], Conductive Anodic Filament (CAF) tests [6].

MRT-3 Printed Circuit Board Design

The MRT-3 printed circuit board design used for this study is shown in figures 1, 2 and 3. The two IST coupons are specifically designed to combine via reliability and material analysis. Both coupons contain a 0.254mm (0.010") drilled hole size, one coupon located on a 1mm via-to-via spacing and the other coupon has a 0.8mm via to via spacing. The via chains on 1mm and 0.8mm grid in the IST designs are designed identically such that both using the same hole size, including the use of non-functional pads on signal layers only, etc. Complete design details are reported separately [7].

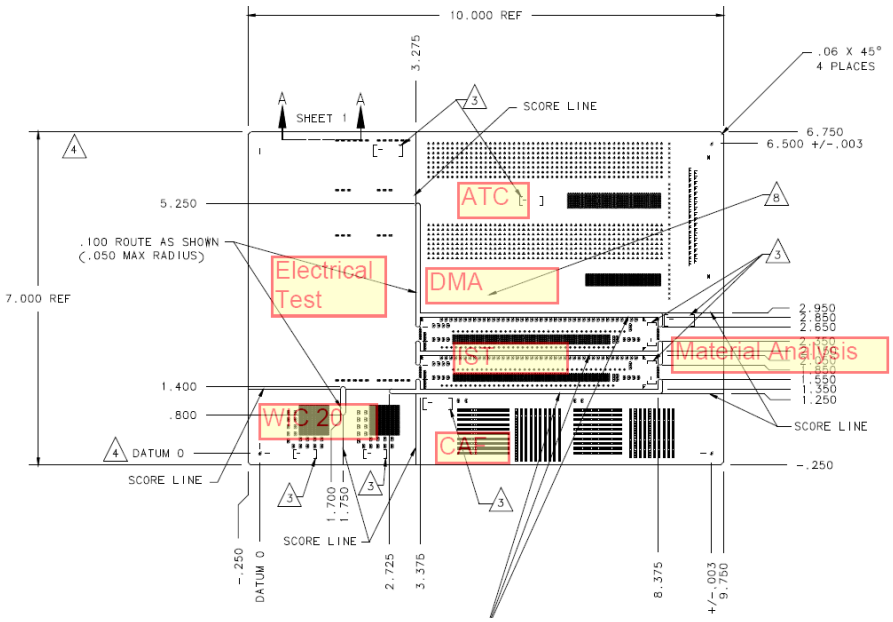


Figure 1

The MRT-3 test board was stepped and repeated 4 times (2 by 2) onto a 24” (610mm) x 18” (457mm) production panel, see figure 2 for production panel lay-out. For this study a minimum quantity of 6 production panels were produced, resulting in a minimum of 24 coupons of each type. Subsequent testing was carried out on both non-stressed (as received) and stressed (6x 260°C Reflow), this effectively results in a maximum of 12 coupons of each type for each test condition. For the purposes of increased statistical confidence a higher number (18+) is recommended, the lower quantity was determined by considering a compromise between statistical validity and containing the escalating costs associated to all types and levels of material testing.

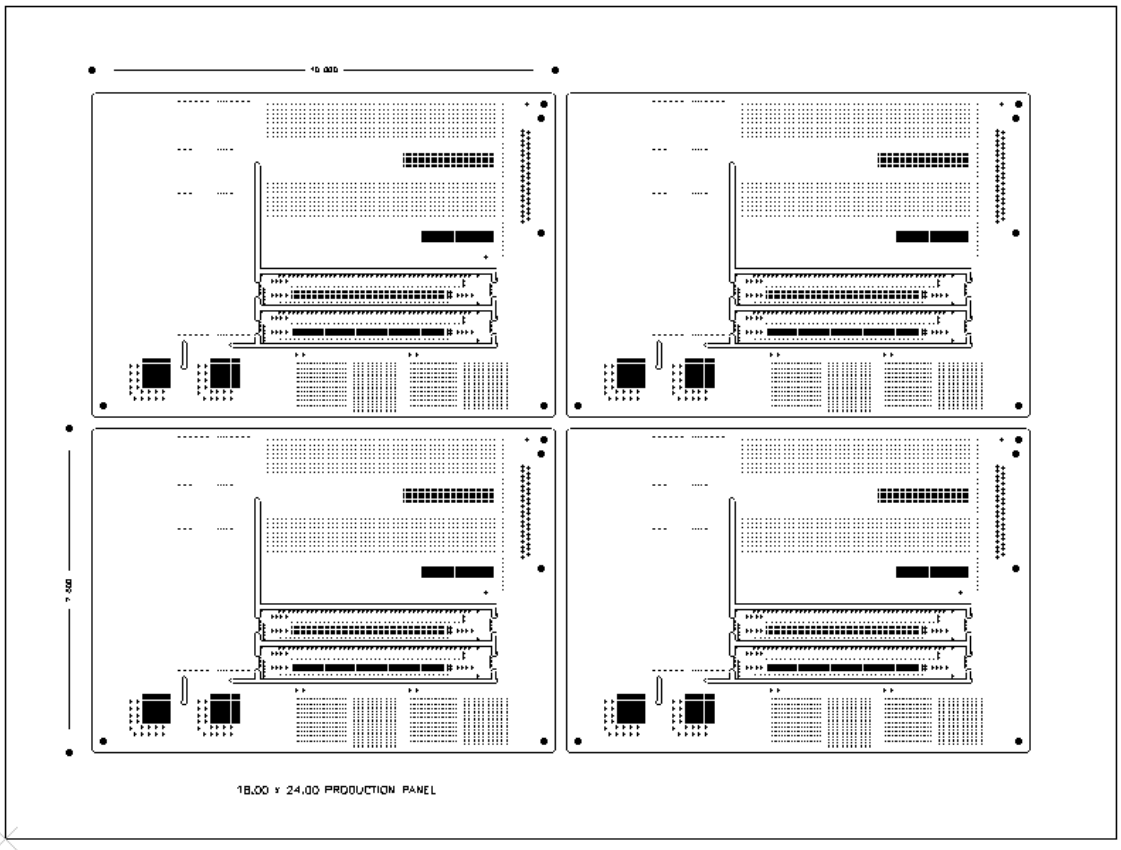


Figure 2

Following the production of the 27 different material types the production panels were pre-routed to enable easier removal (singulation) of certain coupon types and then profile routed into individual (10”/254mm x 7”/178mm) test boards. Figure 3 shows a pre-routed individual test board.

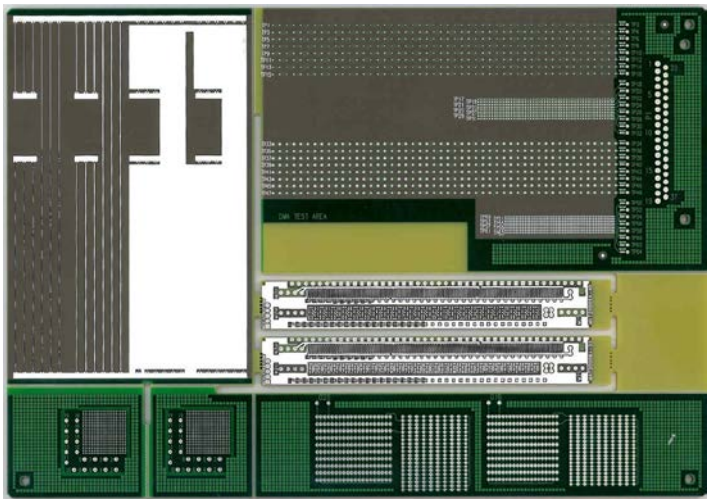


Figure 3

Small labels with material codes were included near each dash number box for each coupon on the panel. This was done to ensure traceability back to the original panel once all the coupons were broken out of the panel following assembly.

Two IST coupons are in each board design as shown in Figure 4. The IST coupons are specifically designed with part numbers MAT20006A-32 at 0.8mm (0.032") and MAT20005A-40 at 1mm (0.040") grid respectively. Note the design is generic and can be designed for any number of layers, copper weights and internal constructions.

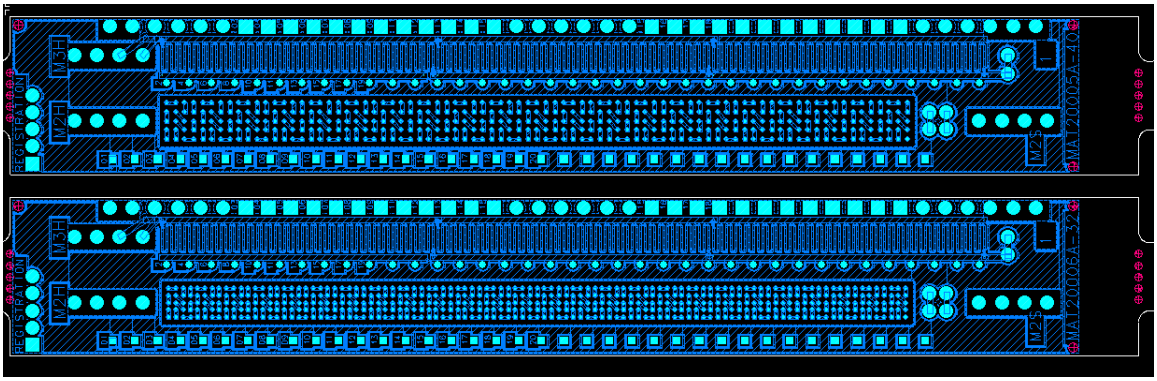


Figure 4: The two IST coupons used in the MRT-3 design.

Four different sets (2 groups of 6 coupons with 1mm and 0.8mm grid) were tested as follows:

- As built (non-stressed), to establish a baseline/reference
- After 6X 260°C reflow assembly (stressed), to be compared to the baseline.

All capacitance measurement were completed on an automated fixture, specifically designed for MRT-3 IST coupons, see figure 5. The test system incorporates a high precision capacitance measurement system, utilizing an auto-ranging frequency capability, which is interfaced to user friendly application software. The measurements, data collection and analysis are both displayed and stored to enable the understanding of information related to product construction, processing variability and relative changes to an established reference, used to determine if material damage is present. The principles used by this tool have proven to be an effective methodology for establishing a reference for determining whether the PWB manufacturing/processing conditions are consistent panel to panel/lot to lot (under control) and that the specified materials used in printed wiring boards are capable of withstanding the cyclic exposure to temperatures that possibly exceed the materials inherent robustness.

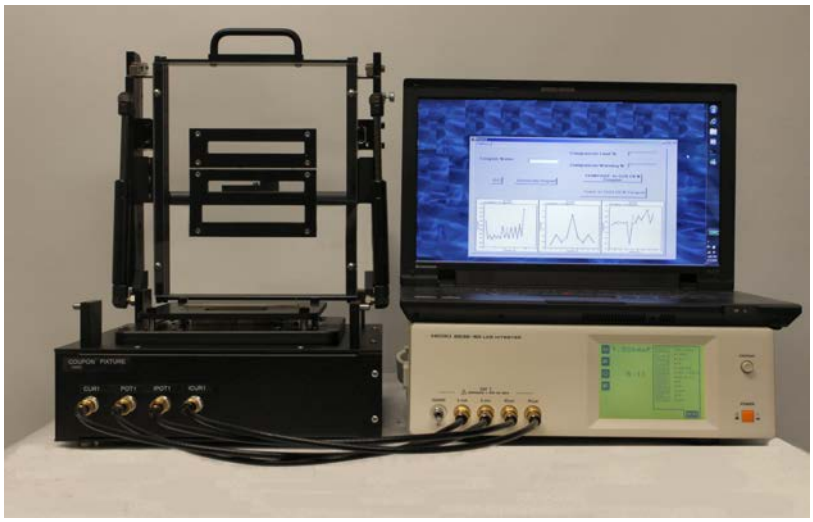


Figure 5: Automated Test Measurement System and Fixture

It was accepted by the consortium that if capacitance testing on the IST coupons identified material delamination or degradation after 6X reflow, suspect coupons would be cross-sectioned to confirm the presence of the material damage. Following a review of the combined results (electrical and microsections) a decision was made for specific materials whether or not to go forward into the via reliability testing phase. Note the 0.8mm pitch coupons are typically more susceptible to

internal delamination, more so than the 1mm pitch coupons. If only the 0.8mm pitch coupons demonstrated delamination, the 1mm pitch coupons could still be deemed acceptable for the via reliability testing.

This paper divides the different testing functions and associated data analysis into four primary categories: A) Confirmation of construction, B) Consistency of Product Construction, C) DELAM protocol: Materials Survivability through 6X 260°C Assembly, D) Dielectric thickness estimation/measurement. Each category is supplemented with an appendix (A, B, C and D) which contains the results for all tested coupon, **the appendices are only available to members of the HDPUG consortium**.

Confirmation of Construction

The product construction section (commonly known as "M1") is designed utilizing a common copper filled area of the materials analysis test (MAT) coupon. The identical copper plates (planes) are created on all internal/external layers. Figure 6 identifies an individual filled area, which represents a single plate.

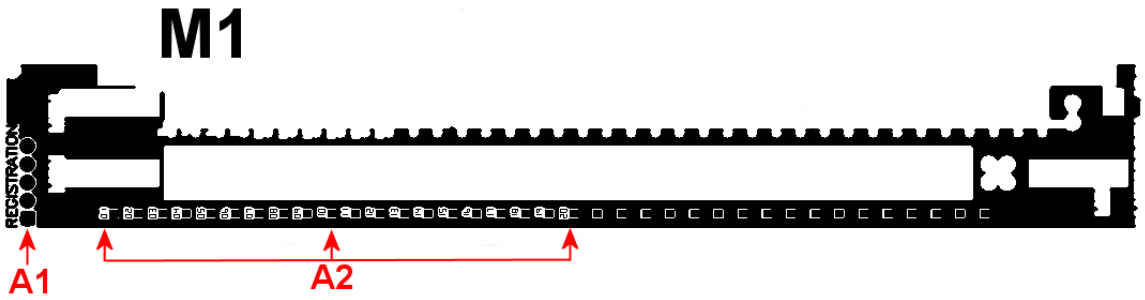


Figure 6

Connections to each plate within the coupon are achieved using a drilled and plated through hole (located in area A2). The holes (based on number of layers used in the construction) are located on a specific via to via spacing (grid) to enable a capacitance measurement using either an automated test fixture, or a manual probing technique. The measured capacitance values are used to determine specific information related to each dielectric pair (B or C stage). One of the surface layers (usually layer 1) should contain a numbering scheme (located adjacent to the hole in area "A2") that confirms which holes are connected to each of the external and internal layers. In addition to the capacitance section there are the conventional registration vias ("A1"), used to measure the drilled hole to internal layer registration. Figure 7 illustrates the appearance of the plate on layer 1 of the MAT coupon.

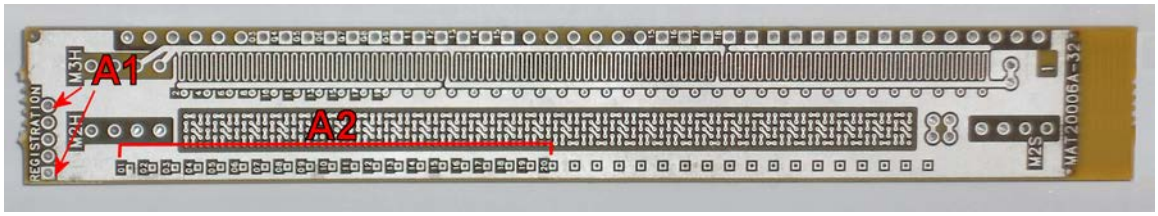


Figure 7

Each internal and external plate is individually designed to be identical in size/area. The plate area will vary slightly by design, in this study the M1 plate for the 0.8mm/0.032" grid coupon was 544.8mm^2/0.8445in^2; the 1mm/0.040" grid coupon was 525.5mm^2/0.8146in^2. For reference the thickness of copper foils and/or any additional inner/outer layer plating are not factors that affect the plate area. By measuring the bulk capacitance for each hole pairing in section A2 (L1 to L2, L2 to L3, Etc.) you are effectively establishing a relative bulk value associated to the plate area, dielectric thickness and the materials inherent electrical properties (dielectric constant - Dk). In this study the auto-ranging frequency function established 800 KHz as the most efficient frequency level for ensuring accuracy, repeatability and reproducibility.

The capacitance can be calculated if the geometry of the plate and the dielectric properties of the material between the plates are known. For example, the capacitance of a parallel-plate capacitor constructed of two common plates both of area *A* separated by a distance *d* is approximately equal to the following:

$C = \varepsilon_r \, \varepsilon_0 \, (A/D)$

Where:

C is the capacitance;
A is the area of overlap of the two plates;
ε_r is the relative static permittivity (sometimes called the dielectric constant) of the material between the plates (for a vacuum, $\varepsilon_r = 1$);
ε_0 is the electric constant ($\varepsilon_0 \approx 8.854{\times}10{-}12$ F m^{-1}); and
d is the separation between the plates.

Capacitance is proportional to the area of the common plates and inversely proportional to the separation between conducting plates. The closer the plates are to each other, the greater the capacitance. Anticipating that both the B and C stage dielectric materials "should" have a consistent Dk, the most dominant factor affecting any changes in capacitance value will be related to the dielectric thickness between the two plates. Based on this principle we are able to correlate the relationship between the measured capacitance and the expected dielectric thickness.

The 58% stack-up combined both a C stage using a 1 ply 2116 (53% resin) and a B stage using 2 plies 1080 (62% resin), this should have achieved a pressed thickness of 0.127mm/.005" and 0.137mm/.0054" respectively. See figure 8 for full 58% resin construction details.

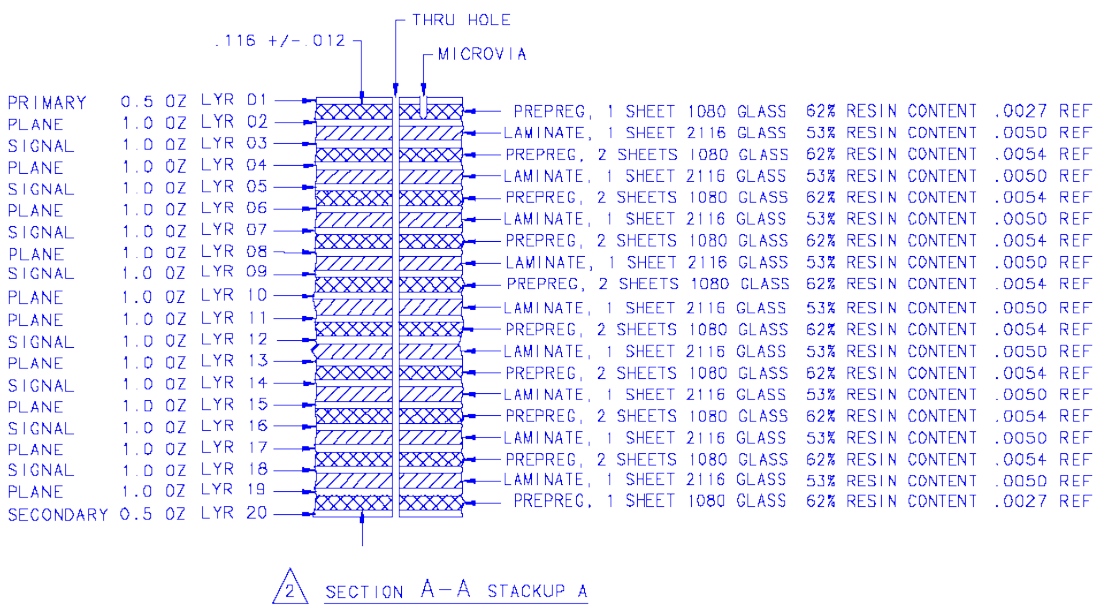


Figure 8

Note: Microvias were ablated into both surface layers (L1 to L2 and L20 to L19), this was required for interconnections used in the S-parameter impedance test board design.

Figure 9 shows an example of the capacitance measurements for seven coupons constructed with the 58% resin stack-up, built on the 0.8mm/0.032" grid, measured as received, built using FR4 material "A". An initial microsection of the test vehicle is recommended to confirm the relationship between the bulk capacitance value and the mechanical measurements. After the M1 section measurements are collected the data can be plotted and statistically compared to determine the full product construction.

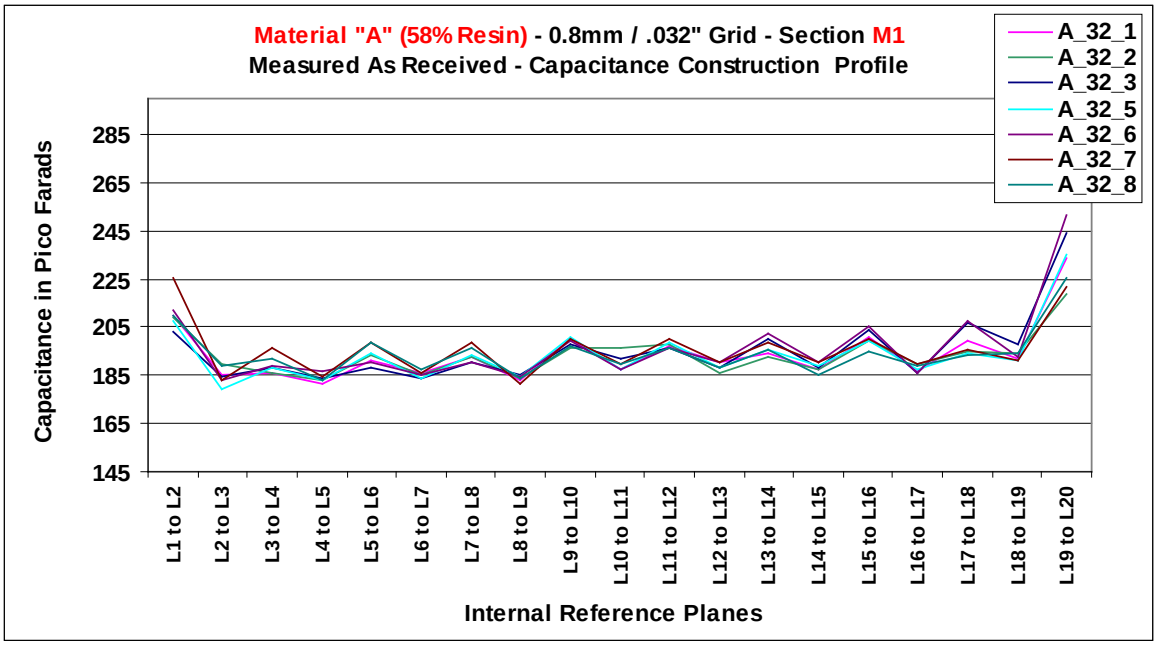


Figure 9

The data confirms that all coupons appear to use the same symmetrical construction. The small difference in bulk capacitance confirms the minor variation in dielectric thickness of the B and C stage materials, showing the C stage with slightly higher capacitance values due to slightly lower dielectric thickness. The data also indicates certain variability that needs further analysis to better understand whether they are related to differences at the PWB supplier (internal process control) or material vendor (material supplier control). The data in figure 9 confirms the outer dielectric pairs measured the highest levels of variability; this is primarily associated to controlling the thinner B stage spacing containing the inherently higher resin content.

The 69% stack-up combined C stage using 2 plies 106 (71% resin) and B stage using 2 plies 1080 (67% resin), this should have achieved a pressed thickness of 0.107mm/.0042" and 0.152mm/.006" respectively. See figure 10 for full 69% resin construction details.

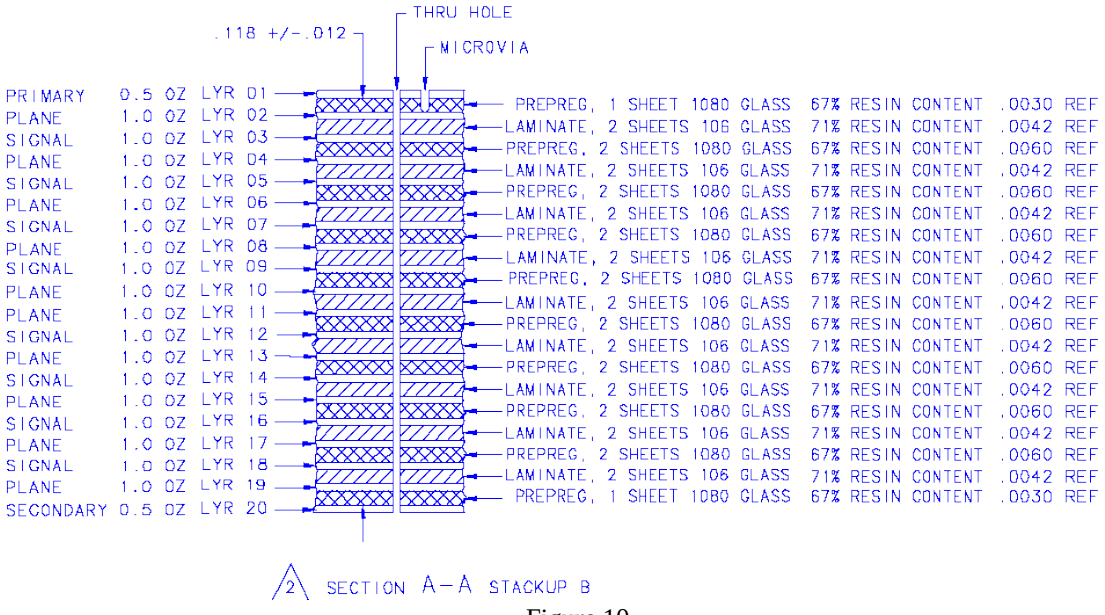


Figure 10

Figure 11 shows an example of eight coupons built on the 0.8mm/0.032" grid, measured as received. Material "B" was built with the same base resin as material "A", but was constructed with the 69% resin stack-up. The data again confirms that

all coupons appeared to use a similar construction, but the 69% construction profile is now clearly different compared to the 58% construction. The difference in bulk capacitance confirms the dielectric thickness of the B and C stage materials are dissimilar, showing the C stage higher due to the decrease in dielectric thickness. The data again indicates variability in both the B and C stage material values.

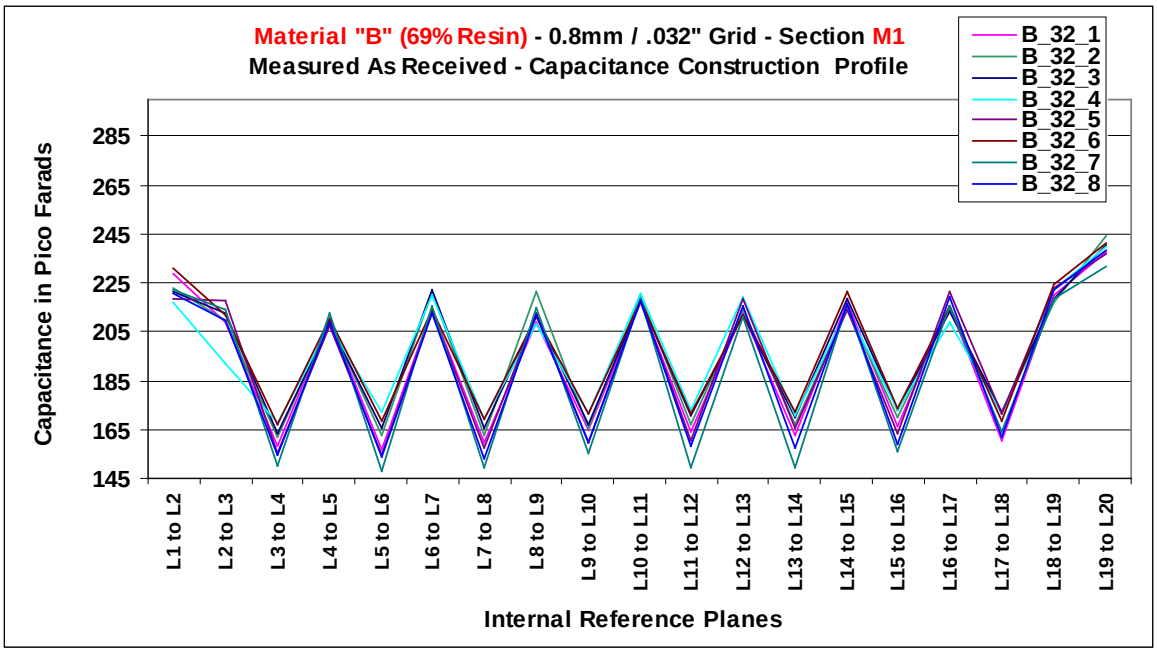


Figure 11

Appendix A (only available to consortium members) includes all measured M1 data collected from every tested coupon, including both via-to-via spacing designs (0.040”-1mm and 0.032”-0.8mm), each of three material types (FR4, Halogen Free and High Speed) and both resin content stack-up configuration (58% and 69%). An analysis of the data from all measured coupons confirmed the following:

- Each material/resin content construction measured different (unique) profiles, and each demonstrating different degrees of consistency between the C and B stage dielectrics
- The majority of materials demonstrated consistent results between all measured coupons. This should not be too surprising considering all coupons were processed within a single production/material lot. It is not known whether different production/material lots would replicate the same results.
- One Halogen Free material (“P”) was intended to use 58% resin content, the construction profile illustrated a different configuration; subsequent analysis confirmed the material contained 62% resin content.
- The dielectrics between the outermost layers measured both the highest readings and the highest variability of all layers. In both stack-ups a single ply of 1080 glass was used to accommodate the ablation of microvias. The increased variation could create challenges for PWB fabricators, due to the potential difference in dielectric spacing.
- Random variations were found between coupons built with the same material type
- Changes within a coupons dielectric layer were easily identified; the non-destructive techniques demonstrated an effective capability to discern small changes within the dielectric.
- The results of the 0.040”-1mm and 0.032”-0.8mm coupons were virtually identical

The mean measurements of all test coupons were calculated based on the 0.032”-0.8mm coupons, the results are shown in figures 12 through 17.

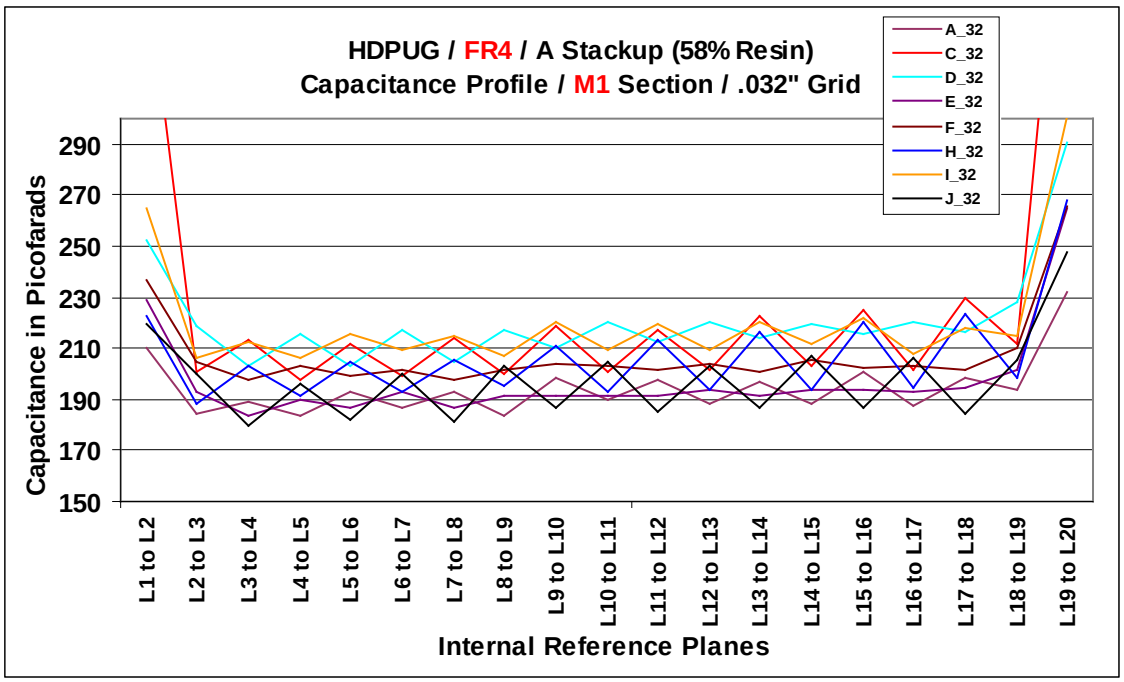


Figure 12 FR4 Material – 58% Stack-up

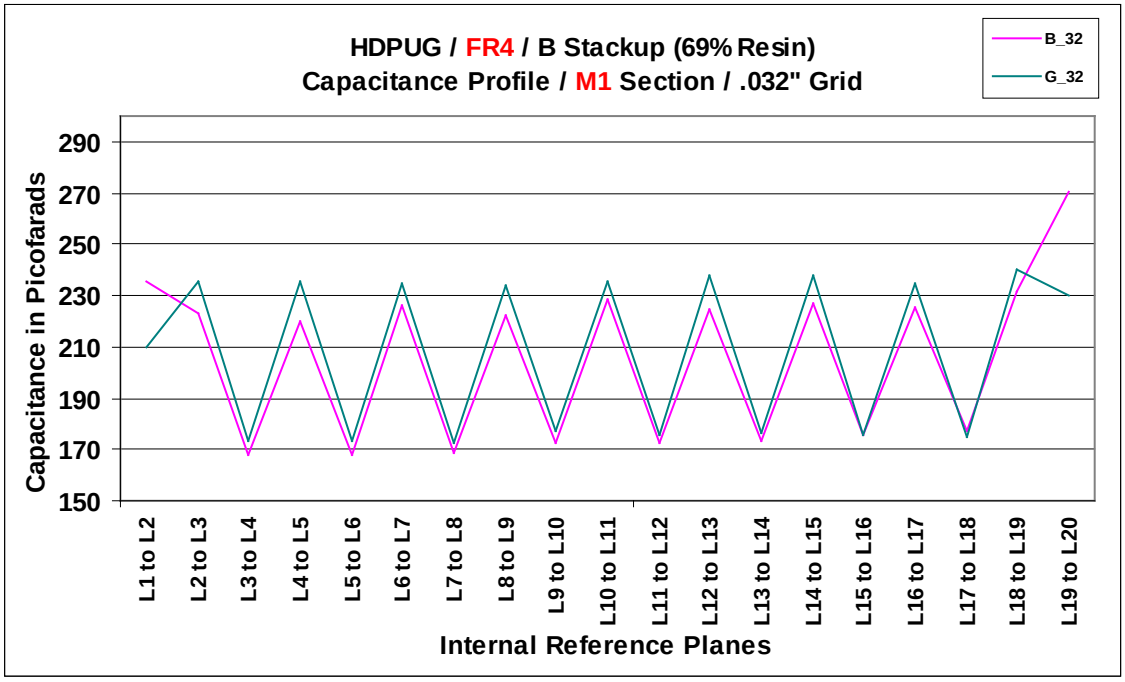


Figure 13 FR4 Material – 69% Stack-up

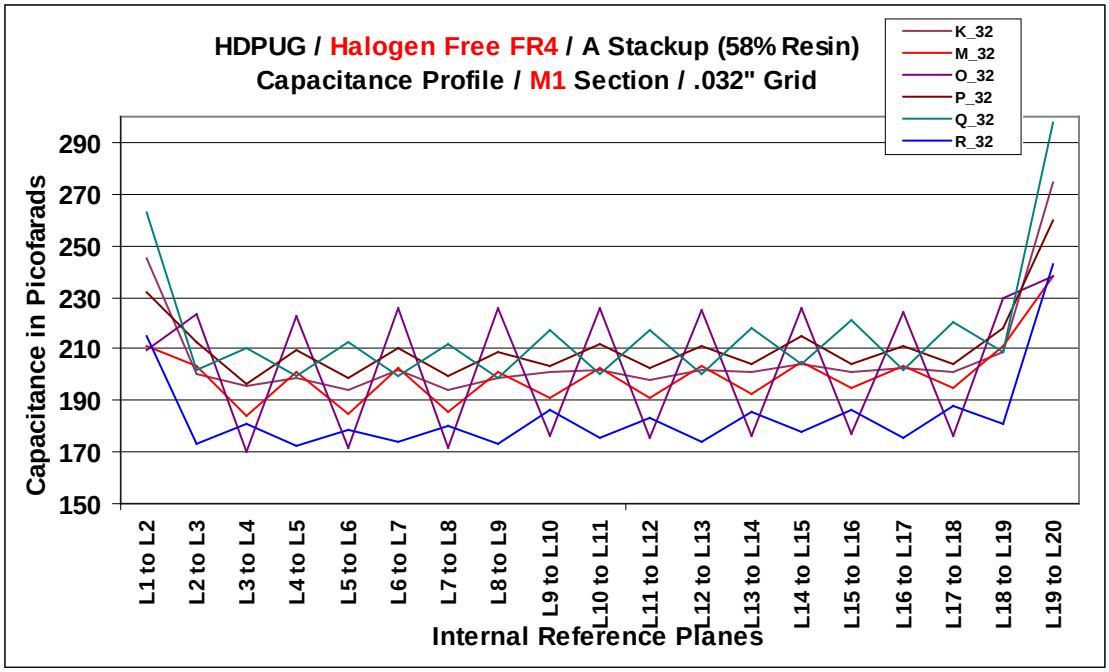


Figure 14 Halogen Free Material – 58% Stack-up

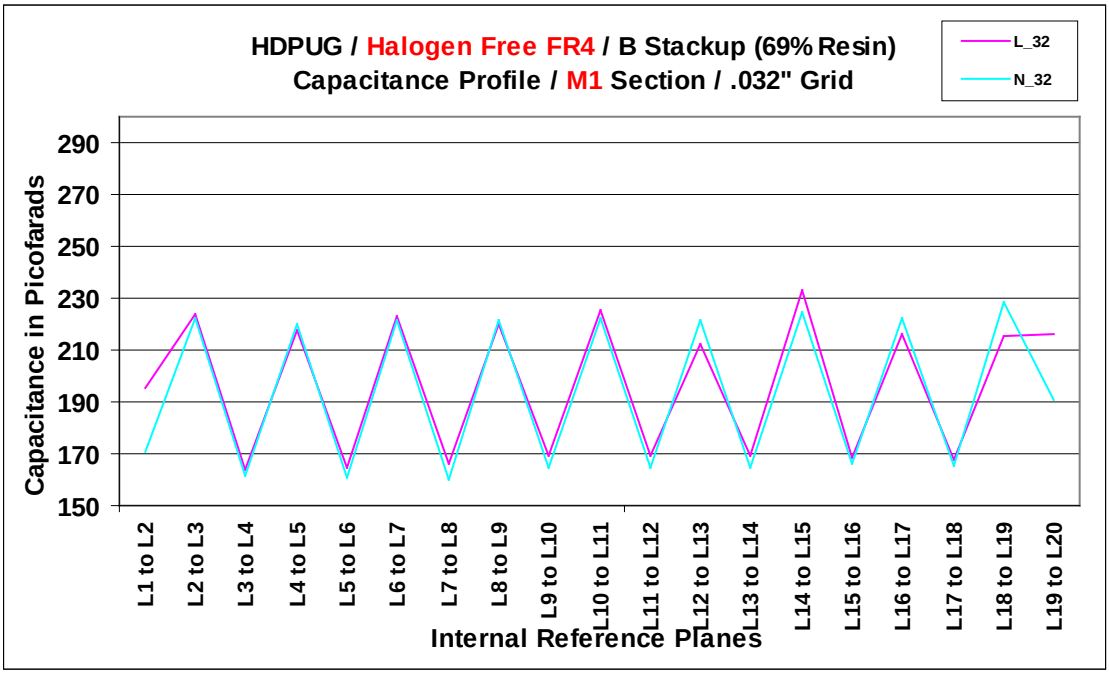


Figure 15 Halogen Free Material – 69% Stack-up

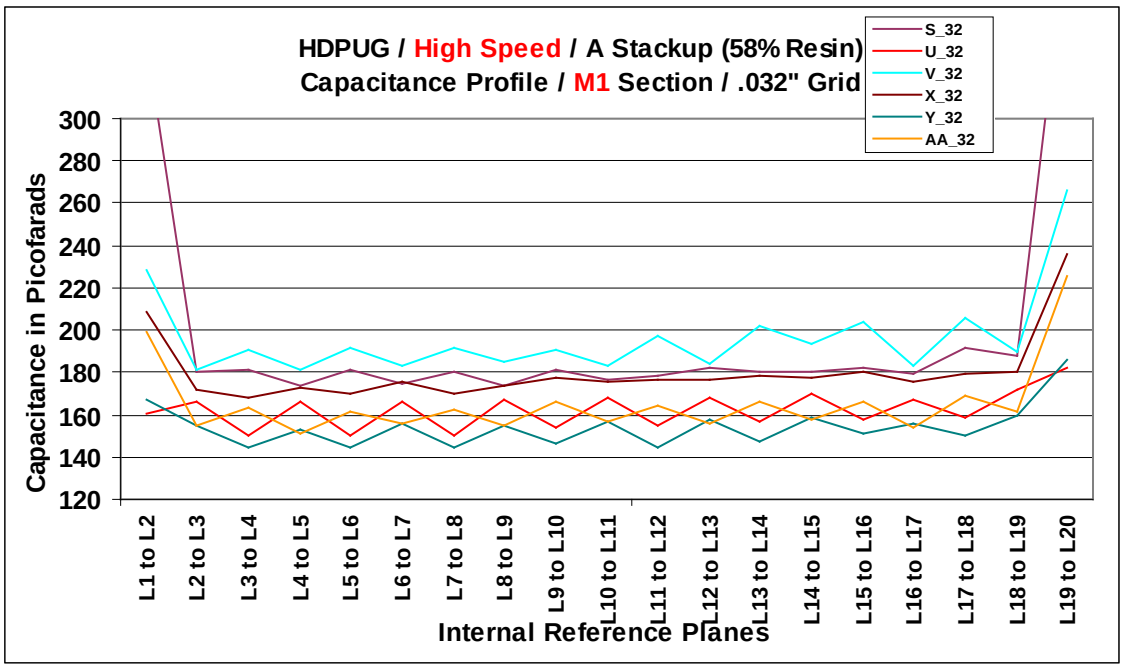


Figure 16 High Speed Material – 58% Stack-up

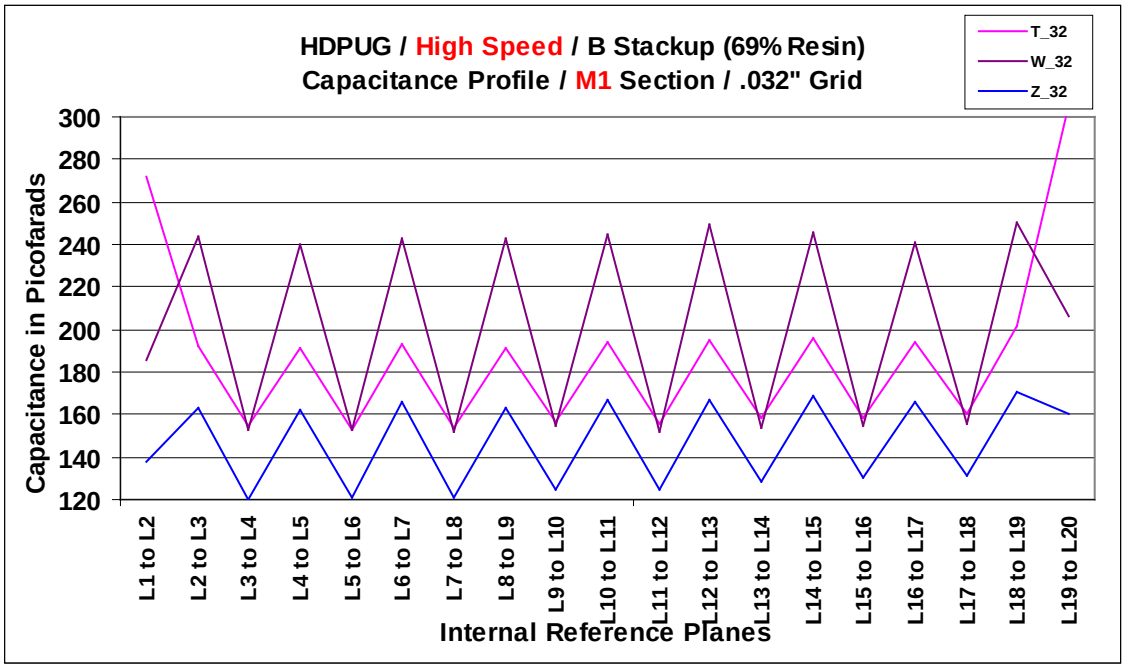


Figure 17 High Speed Material – 69% Stack-up

The measurement of the construction/capacitance profiles establishes a reference for subsequent testing after 6X 260°C assembly. Additionally the data creates a baseline for any follow-on testing of additional panels, from future production lots. Any measured changes found that are relative to this reference profile are potential differences in dielectric spacing, glass/resin content or material Dk properties, any changes found could impact the ability to control the specified impedance value.

This methodology creates a very useful tool for the PWB manufacturer, contract manufacturers and OEM's because it gives an effective non-destructive capability to confirm that all coupons, panels and production lots are built with the same material construction. It is also very useful for electrical designers to determine and better understand material and process variations that improve the ability to establish tolerances related to the influences of both material and manufacturing process for controlled impedance products.

Consistency of Product Construction

The second phase of data analysis was required to better understand the causes of variations found between the coupons from the same material type/configuration and then determine whether the differences were related to either levels of control within PWB manufacturing, or are inherently within the B and C stage materials received from the vendors. The testing completed permitted a sampling of each material type and stack-up configuration. The data from the two designs (.040"–1mm and 0.032"-0.8mm) were compared and proved statistically consistent (virtually identical) increasing the confidence that both coupon designs effectively measured the same levels/degrees of variability.

For this section of analysis of the consistency can only be construed as relative, because there are inherent differences between material properties (Dk) that do not permit an absolute comparison. The normalization of the data will be considered in the dielectric thickness estimation/measurement section of this paper.

The variability of measured capacitance was influenced by the combination of both the material vendor and the PWB manufacturer. The C-stage (cured) laminate is commonly produced with high levels of process control; the materials are required to meet exacting tolerances, based on thickness and electrical specifications. The thickness tolerances can be controlled by purchasing to one of three IPC standard classifications (A, B or C), in this study the material vendors were requested to build to their "standard" tolerance, which is anticipated to be "B" class. The PWB manufacturers influence on C-stage variability is negligible; their process variability is primarily related to the B-stage (pre-preg/bonding) laminate, created by the processing through their pressing equipment and applied controls used during the lamination and curing procedures. Differences in pressed thickness and resin flow characteristics are related to glass/resin ratio which can vary dependent on the methods of heating in the press (electrical/steam/oil), heating ramp-rates, applied pressure and platen planarity. The design of the product can also affect the ability of the resin to flow effectively, in this study the test vehicle design was consistent, and so the results are considered relative.

The bulk capacitance data collected from the M1 section for each of the 27 material types consisted of the following: Average of eight coupons from both coupon designs (0.8mm/.032" and 1mm/.040" grid), nineteen dielectric layers (B and C stage), measured both as received and after 6X @260°C reflow. For this section only the data from the as received coupons is compared.

For each material type and grid size a low, median, high box diagram was created, illustrating the consistency of each dielectric layer within the coupons construction. Figure 18 illustrates an example of a "predictable" material (Type "U" - High speed – 58% Resin) that demonstrated good overall consistency for all B and C-stage dielectric layers. The first and last data-points (distribution layer for the microvias) identify good outer layer control, the internal B and C stage dielectrics confirm low variability and very similar capacitance values, indicating the thickness of each layer would be virtually the same.

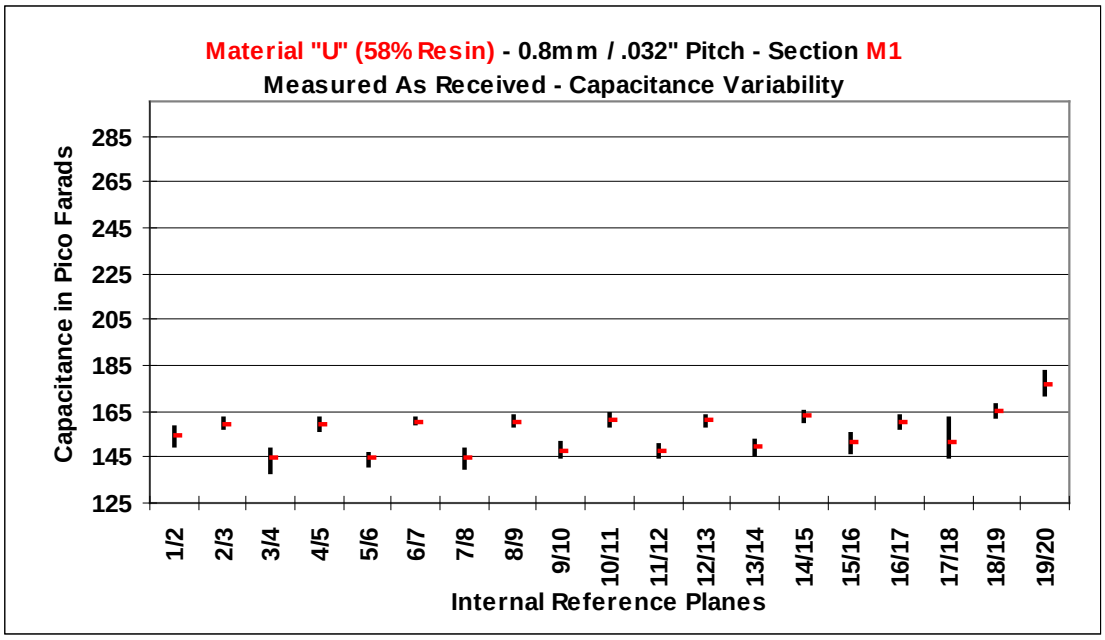


Figure 18

Figure 19 shows a FR4 material (Type “E” - FR4 – 58% Resin) with increasing variability, primarily in the B-stage material. The B-stage in the outer layers is effectively measuring double the amount of variance compared to the internal B-stage layers. Increased variability of the outer layers will primarily influence the control of thickness (volumes of resin) remaining between the surface and first internal copper foils, this critical geometry will impact the ability to effectively ablate the microvia cavity down to the target pad. The capacitance variability of all coupons equates to 11% (L1 to L2) and 15.5% (L20 to L19), the measured difference found in microsectioning was 0.01mm / .0004” to 0.015mm / .0006”. The C-stage demonstrated good control and appears very consistent.

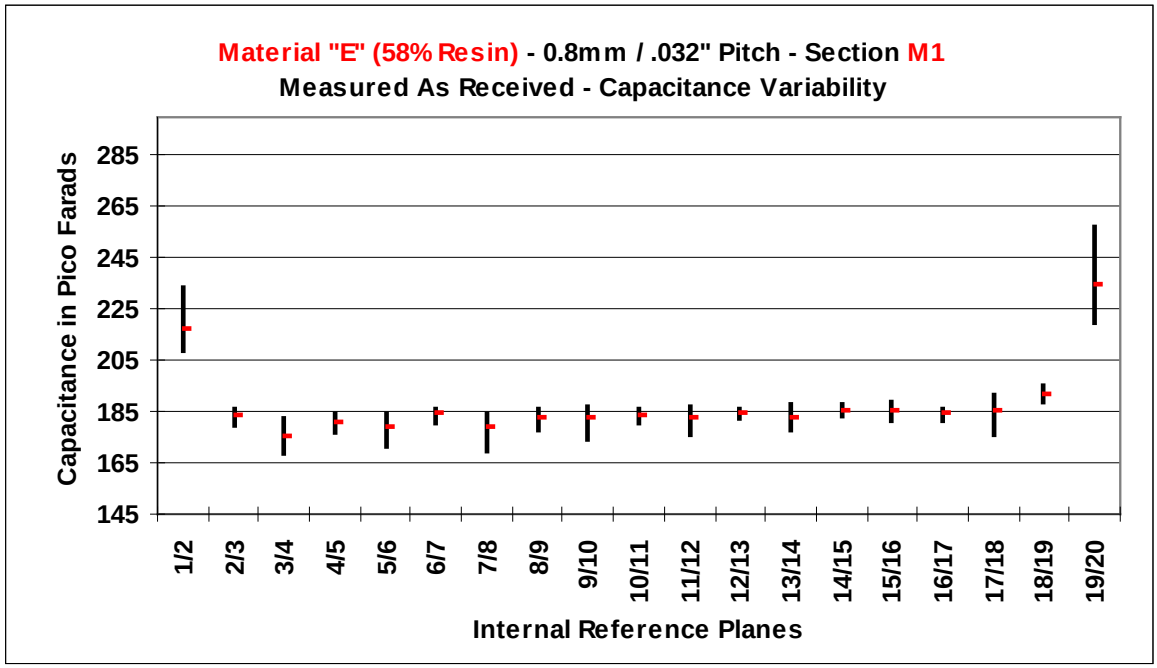


Figure 19

Figure 20 illustrates a halogen-free material (Type “Q”) that exhibits high variability only on the B-stage layers, but good controls within all C-stage layers. The increased levels of variability in the B-stage do not necessarily result in a reliability concern, but the 15% to 20% difference in capacitance values (anticipated differences in thickness) will have a 1% to 2% effect on line impedance. Although this is not a large factor it will absorb 10% to 20% of the available impedance tolerance.

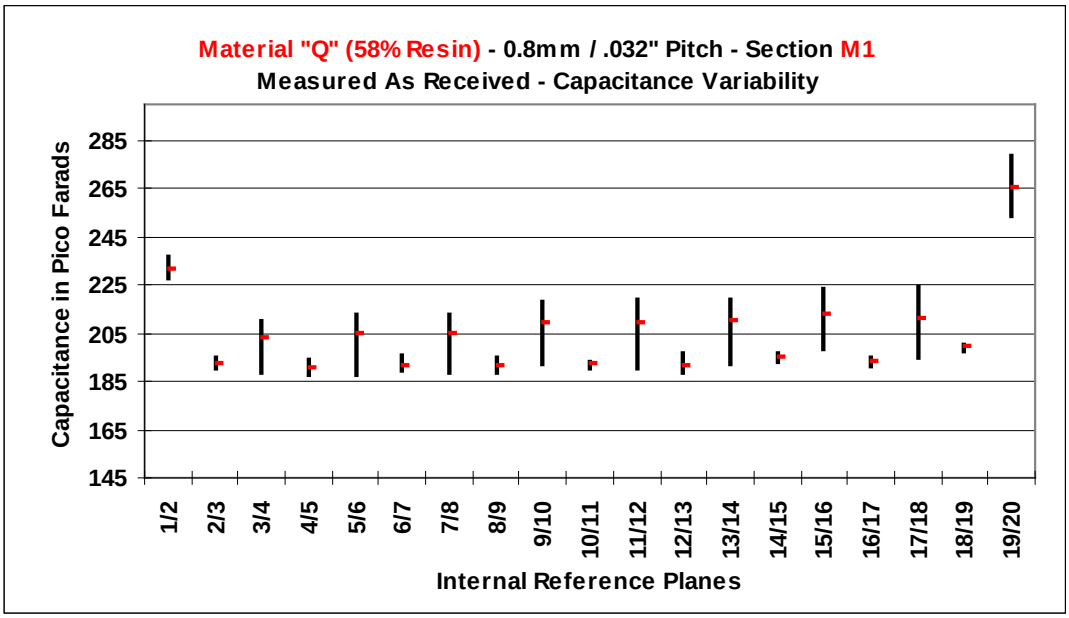


Figure 20

Figure 21 shows a high speed material (Type "V") that demonstrated unpredictable changes in capacitance values, this is indicative of material damage, due to changes in the material properties (Dk). Subsequent microsections confirmed the presence of material damage. Delamination was also found following 6X 260°C reflow, this material was subsequently withdrawn from the via reliability testing.

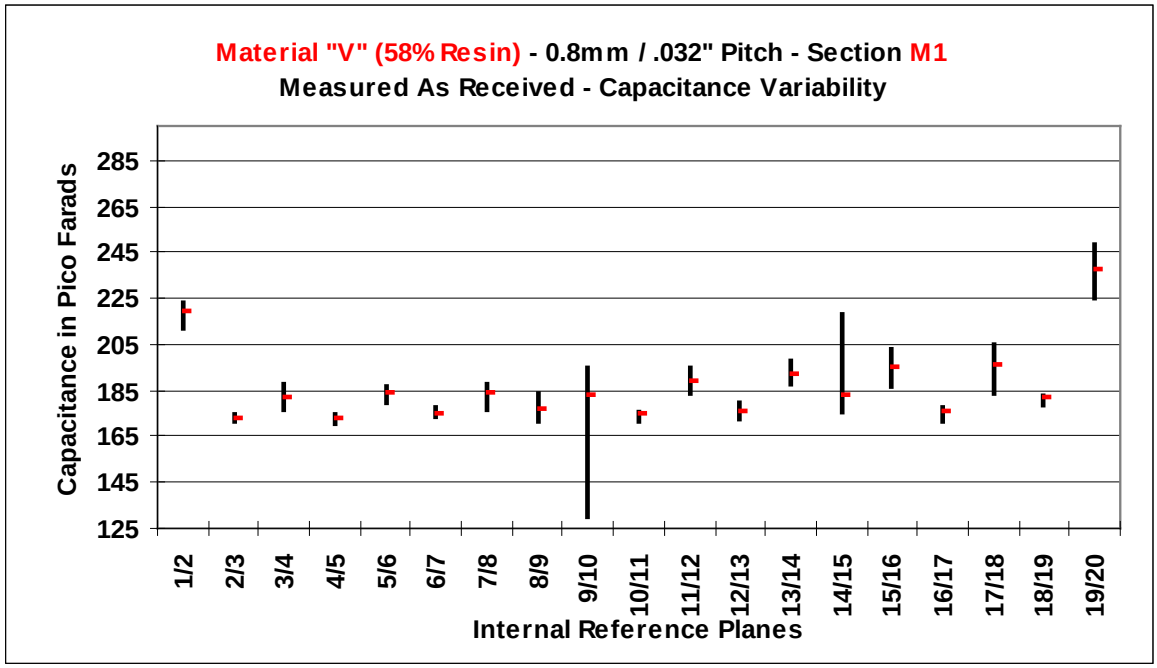


Figure 21

Following an initial review of all data, certain trends became evident:

a) When comparing the results for all materials, the overall consistency demonstrated a wide variety of controls for both the base materials and PWB manufacturing process. The data ranged from virtually identical results for all coupon (both grids), to a maximum of 15% difference between the 8 coupons from each grid size.

b) Each B-stage dielectrics (in the majority of cases) measured between 2x and 4x variability compared to the C stage dielectrics (for the same material).

c) The two outer most layers (L1 to L2 and L20 to L19) demonstrated the highest levels of variability of all B-stage dielectrics. This should not be too surprising considering the use of a single ply of 1080 B-stage (62% and 67% resin content) used in A and B stack-ups. The resin flow characteristics required for both insulation and encapsulation for the outer layers demonstrated a variance by either coupon location, and/or panel to panel consistency.

d) Based on the small sample size and understanding that each material was being compared based on a single production lot, increased variability should be anticipated if a either a larger sample size or multiple production lots were factored into the equation.

The data was further analyzed to determine whether the results were being influenced by one or more of the multiple variables involved in this study. The minimum and maximum range (Pico-farad delta) of capacitance values were calculated for each material and grid size, and then sub-divided into three categories: a) The B-stage dielectric for the outer layers only, b) All remaining B-stage dielectrics, c) The C-stage dielectrics. Figure 21 summarizes the results for all material types

Type	32 Outer	40 Outer	32 B-Stage	40 B-Stage	32 C-Stage	40 C-Stage
A	28	17	9	7	7	6
B	13	13	19	14	10	8
C	19	15	9	7	5	4
D	21	17	15	10	6	5
E	31	25	12	12	6	6
F	17	15	14	13	7	6
G	17	15	14	13	8	8
H	27	22	21	18	9	10
I	14	13	27	21	4	3
J	17	13	11	7	4	4
K	7	4	12	8	19	19
L	11	12	13	10	3	4
M	6	4	10	9	6	6
N	7	9	9	11	6	6
O	16	9	10	9	7	6
P	17	17	26	25	5	5
Q	13	13	8	7	3	3
R	35	32	26	19	14	12
S	19	16	7	7	7	7
T	8	20	8	6	4	4
U	17	10	19	15	10	10
V	15	21	12	9	13	10
W	18	19	20	10	4	4
X	8	7	15	8	3	2
Y	18	18	14	11	4	4
Z	23	18	15	14	6	6
AA	14	13	15	16	6	5

Note: A to J – FR4 / K to R – Halogen Free / S to AA – High Speed

Figure 21

Figure 22 compares the mean variability of the outer layer B-stage dielectrics to the base resin type (FR4, Halogen Free and High Speed), the only trend is that the Halogen Free demonstrated the lowest overall level of variability.

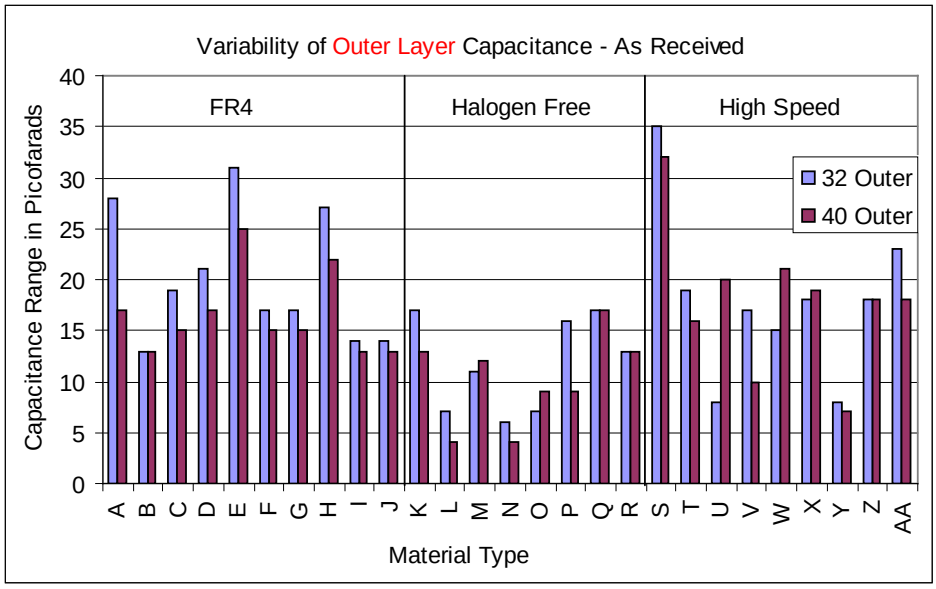


Figure 22

Figure 23 compares the mean variability of the all other B-stage dielectrics to the base resin type (FR4, Halogen Free and High Speed), there are no clear trends.

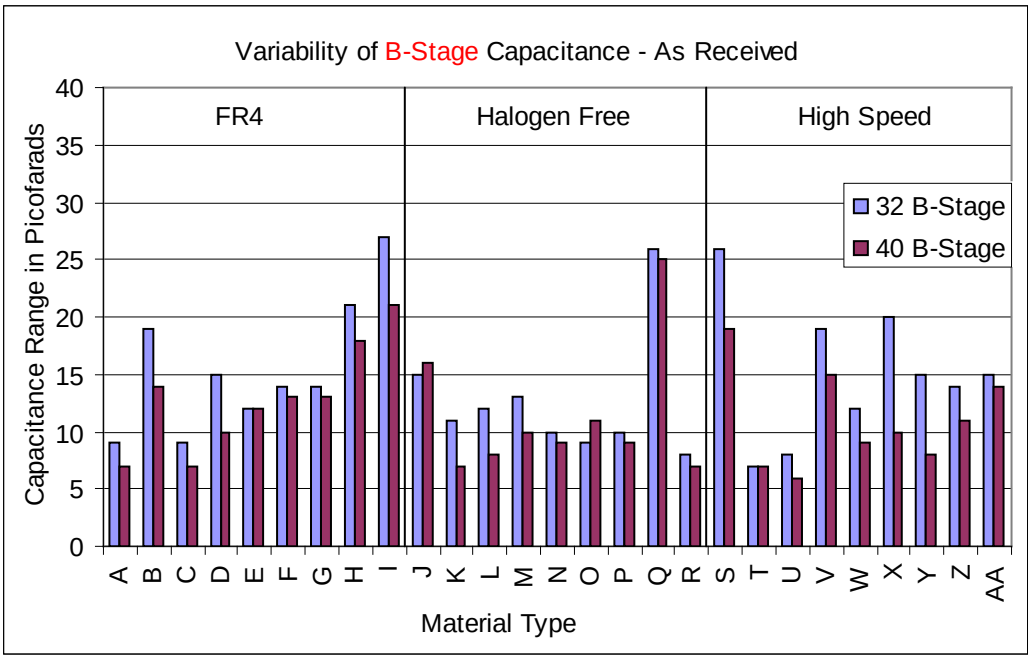


Figure 23

Figure 24 compares the mean variability of the C-stage dielectrics to the base resin type (FR4, Halogen Free and High Speed); the only trend is that the FR4 demonstrated the lowest levels of variability, although the Halogen Free is similar with one exception.

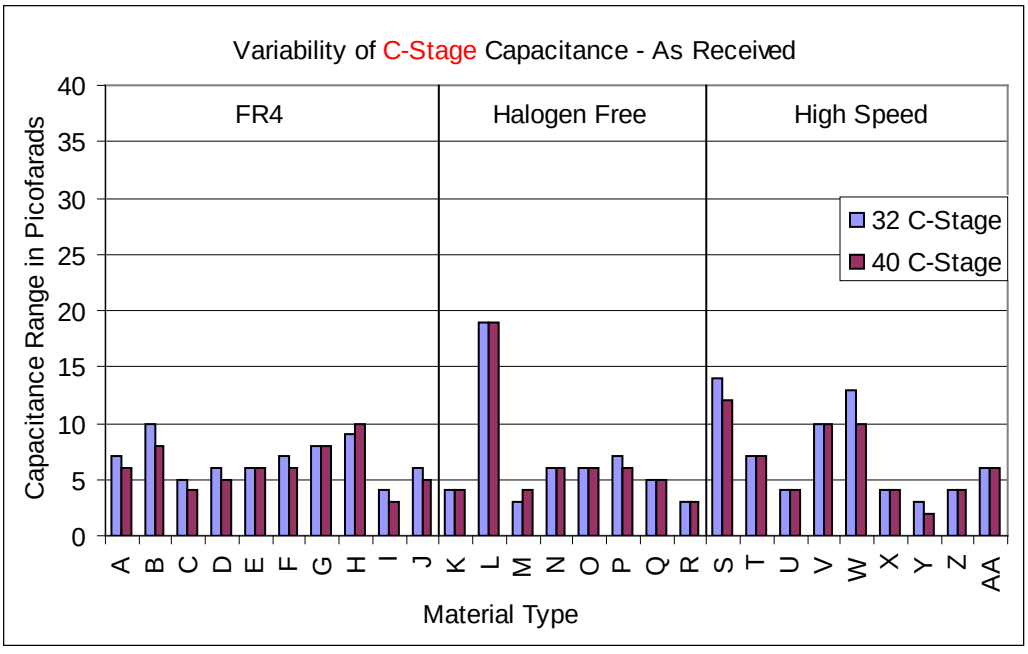


Figure 24

Figure 25 compares the mean variability of the B-stage dielectrics to the stack-up configuration (58% to 69% resin content) the only trend is that the 69% resin content demonstrated a slightly lower overall level of variability.

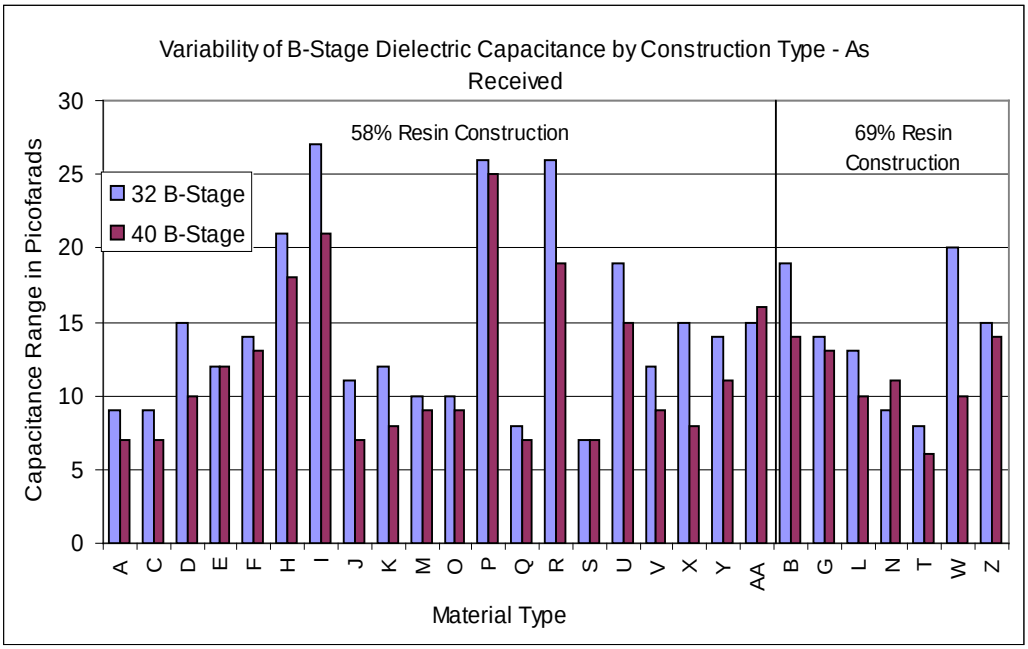


Figure 25

Figure 26 compares the mean variability of the B-stage dielectrics to the PWB manufacturing site; the small trend is that the PWB Site #2 demonstrated the lowest overall level of variability.

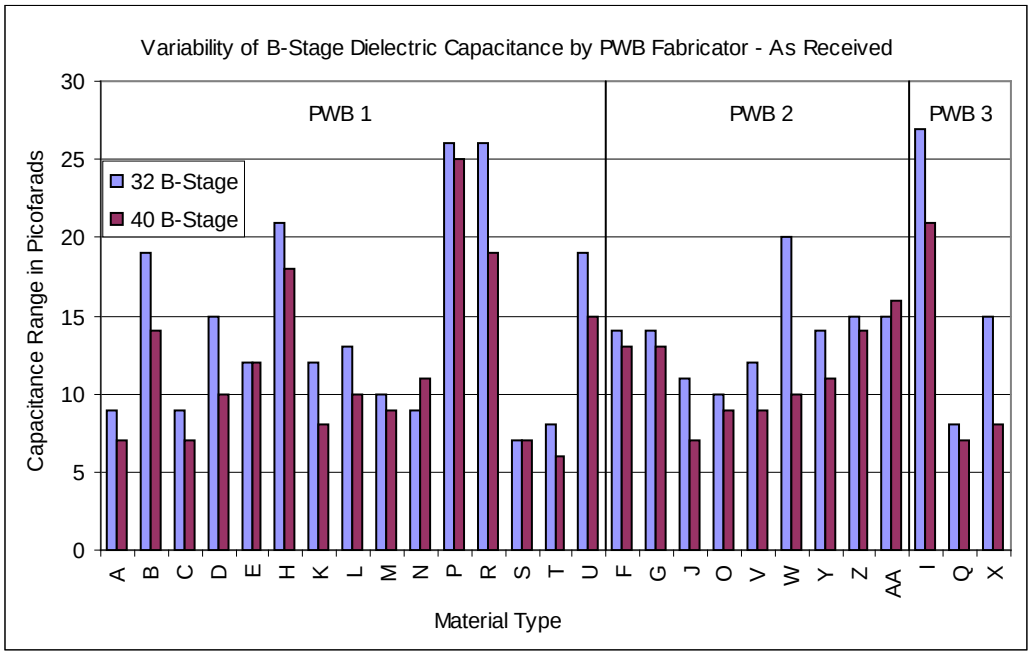


Figure 26

Figure 27 compares the mean variability of the B-stage dielectrics produced by the material suppliers, vendors 1, 3, 5 and 6 produced materials with the highest variability.

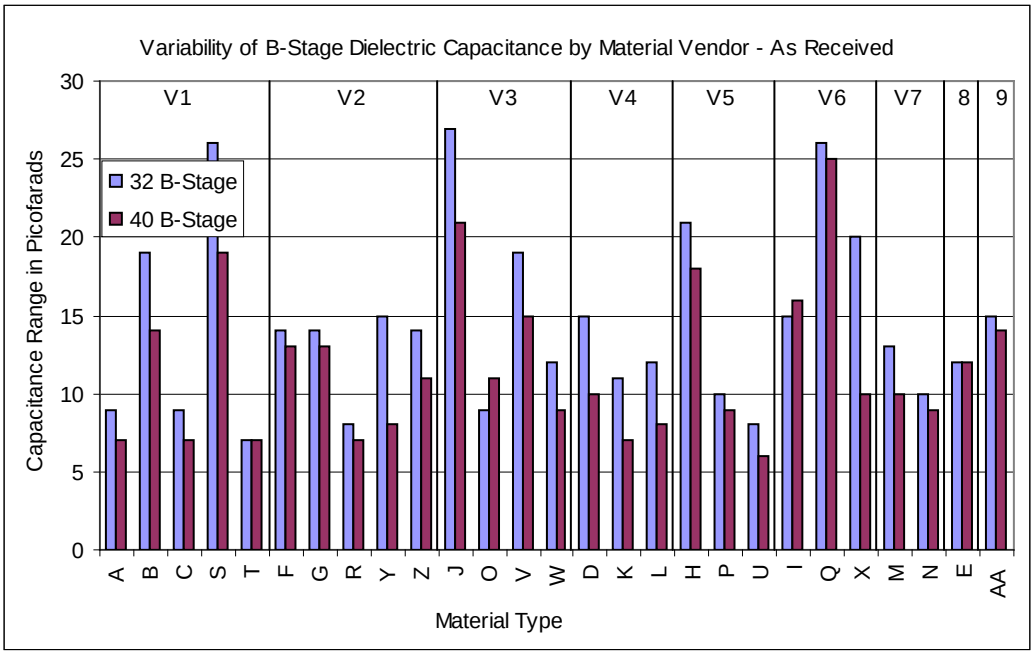


Figure 27

Appendix B (only available to consortium members) includes box-plot graphs for each material type, comparing the low, median and high measured values from the M1 data, collected from all tested coupons.

DELAM protocol: Materials Survivability through 6X 260°C Assembly

The Laminate Analysis Methodology (LAM) activity associated to the DELAM test protocol utilizes a different section of the MRT-3 coupon; it is commonly referred to as the M2 section. The test circuit area has two primary responsibilities: a) Reliability testing of the via structures, b) Robustness testing of the materials, following assembly. The via reliability protocol involves the electrically (ohmic) heating of the coupon on the IST test system, in order to thermally cycle between ambient and 150°C in 3 minute cycles to measure via reliability. Figure 28 illustrates the M2 section, it is designed with a "super-heat" circuit (four-pin connector shown as "B1"), located at four internal levels (layers 3, 7, 14 and 18) of the product construction. The traditional via reliability test (sensing) circuit (four-pin connector shown as "B2") measures the plated through vias from the top to the bottom layers. Area "B3" defines the hole to hole spacing (grid/pitch), this study used two separate designs (0.8mm/.032" and 1mm/.040" grid).

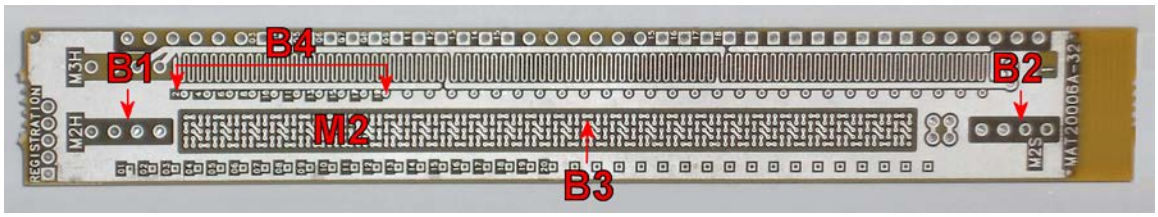


Figure 28

The material testing includes PTH with the via-to-via spacing, which should be consistent with the smallest grid/pitch device designed into the product. The capacitance holes ("B4") are connected to each of the internal copper planes; these connections are identical to product construction. The layer to layer configuration selected by the consortium used a strip-line (sig/plane/sig/etc.) concept; each internal copper plane was connected using a drilled plated through hole which resulted in 10 internal planes (9 capacitance measurements). The reduction from 19 individual dielectric measurements in M1 to 9 combined B and C stage measurements in M2 has two implications to effectively determining the presence of material damage; a) the sensitivity to measure Dk change between two dielectrics is reduced because the area of damage that changes the Dk becomes a smaller proportion of the bulk capacitance, b) the measured changes in capacitance are lower because the small (localized) increases in dielectric thickness, caused by the presence of a material separation are relatively lower in proportion to the increased dielectric thickness. Accepting this reality confirms that small areas of material damage may not be easily detected until the total area is sufficiently large enough to effectively measure with statistical confidence.

The M2 section has two unique features compared to the M1 and M3 sections: a) the inclusion of 0.25mm/0.010" drilled and plated through vias (commonly filled in most designs) located on a 0.8mm/0.032" and 1mm/0.040" grid sizes. These grid sizes are consistent to the majority of SMT device (PGA, BGA, FPGA, CCGA, etc.) to be used in today's product, although 0.6mm/0.024" grid is starting to become increasingly common. Previous studies by the HDPUG consortium have confirmed that the via-to-via spacing can have a critical effect on the propensity for internal material damage, which was again confirmed in this study. b) The configuration/polarity of the inner layers represents a standard construction used in the electronic industry, basically a signal line located between two internal planes. The combination of these features and the associated distance between the vias and planes creates an environment where vapour pressure has limited ability to dissipate, increasing the shear stress on the glass/resin materials. The vapour pressure is only partially related to the presence of available moisture (absorbed/inherent water content); if the moisture content is very low vapour pressure would still occur (although to a lesser degree) and will continue to increase relative to the rising temperature [4]. The resulting superheated steam would follow the equation P = RT/V, the higher the temperature the higher the pressure for a constant volume of moisture. The reality is that the increased temperatures now being used in lead free assembly has effectively double the level of vapour pressure inside the PWB substrate

Significant bulk capacitance change (greater than 4% reduction) after reflow is typically an indication that internal delamination is present. A change in capacitance of 4% considers some allowance for moisture leaving the coupon during assembly. If this level of change should occur, it is recommended to discontinue any further testing of the material and perform immediate failure analysis. The results of the microsection analysis will confirm or refute the presence of material damage. In this study certain materials were eliminated all together while others were restricted to testing only the 1mm/.040" grid coupons. This process proves effective at removing damaged materials or coupon types before committing to the cost, time and expense of the reliability testing.

The primary responsibility of the material analysis (robustness) testing philosophy is to determine whether the B and C stage materials can "survive" assembly without structural damage (delamination). If the materials are confirmed to be robust it establishes the ability of the product to go forward into the via reliability testing phase.

Material damage has proven to be a confounding factor because it effectively changes the stress loading due to the stress relieving (dissipating) affect around the via structures. There is a high probability of false positive results when measuring via reliability in products that have material damage present.

The MRT-3 coupons are designed to be measured (ideally) before and after the 6X 260°C assembly cycles on the identical coupon. In this study all PWB manufacturing and assembly activities were completed in Asia, the logistical constraints prevented the ability to measure the coupons before the 6x 260°C reflow cycles.

Each of the materials non-stressed coupons were measured and compared, the mean profiles were calculated and established as the baseline/reference for subsequent comparison to all assembled cycles (stressed) coupons. Each material contained various levels of variability between the B and C stage materials, as shown in the consistency of product construction section. Comparing the impact of assembly with different sets of coupons will complicate the situation, but if the coupons follow the same construction in both cases the difficulties can be overcome. Equal quantities of coupons were received with both non-stressed and stressed (assembled) conditions.

Appendix C (only available to consortium members) includes graphs for each material type, comparing capacitance profiles from both grid sizes for the M1, M2 and M3 sections, the data was collected from all coupons exposed to 6X 260°C and compared to the mean profile of all non-stressed coupons. The focus for material damage is based on capacitance changes measured within the M2 section

Evaluating the capacitance data was completed by entering all measured profiles from the stressed coupons into a spreadsheet and calculating the relative change to the reference profile, as a percentage. Figure 29 is a plot of the capacitance changes measured on the M2 section containing a 0.8mm/.032" grid built with material "A". The results illustrate minimal changes were measured, confirming a robust material. The small variations between each coupon are relative to the inherent differences of the dielectric properties (thickness and Dk). The "shape" of the data is related to the comparison with the reference profile, which is based the fact that the mean of non-stressed coupons had to be used in this study.

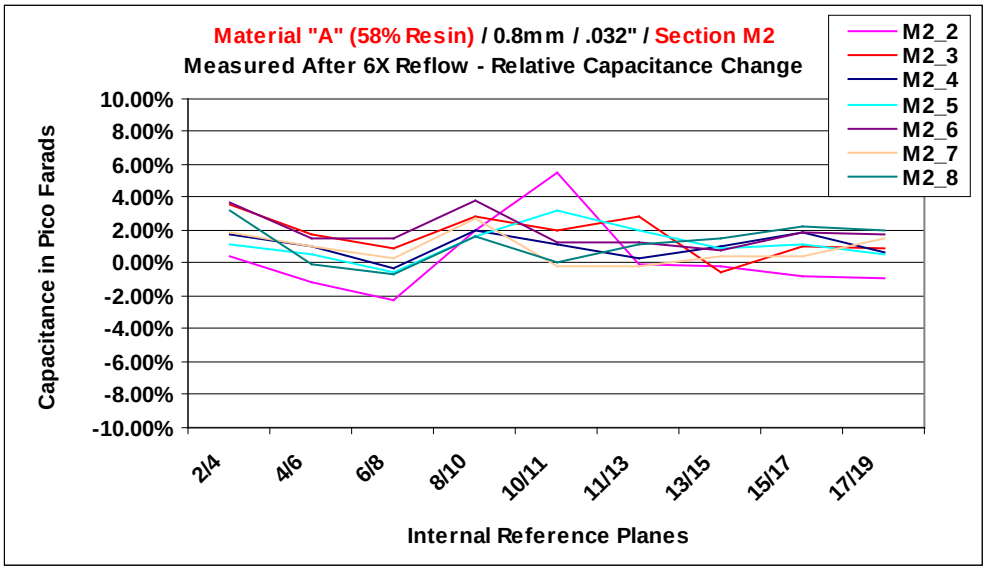


Figure 29

Figure 30 shows the capacitance changes in the M2 section containing a 0.8mm/.032" grid built with material "O". The dramatic change to the capacitance profiles for virtually all stressed coupons clearly demonstrates material degradation (delamination). The data identifies that two levels within the construction were damaged (L8 to L10 and L11 to L13), both dielectric areas are a combination of B and C stage materials, either side of the L10 to L11 central C stage laminate. If delamination occurs within the construction, the material failures are typically near the center of the board (layers 8-13 in the 20 layer construction) where the vapour pressure and shear stress are at their highest levels. The reality that most delamination occurs within the central zone of the construction is significant because most manufacturers of PWB's and assemblers of PCB's are oblivious to their presence; it is only if delamination is visible on the surface layers that a concern is raised. Internal delamination (a physical separation between and within the B and C stage materials) and damage (a breakdown in the bond between the resin and glass fibres) are both conditions where conductive anodic filament (CAF) can propagate [6]. Electrochemical migration is highly accelerated when a physical "path" is available, in combination with the presence of moisture and an electrical bias.

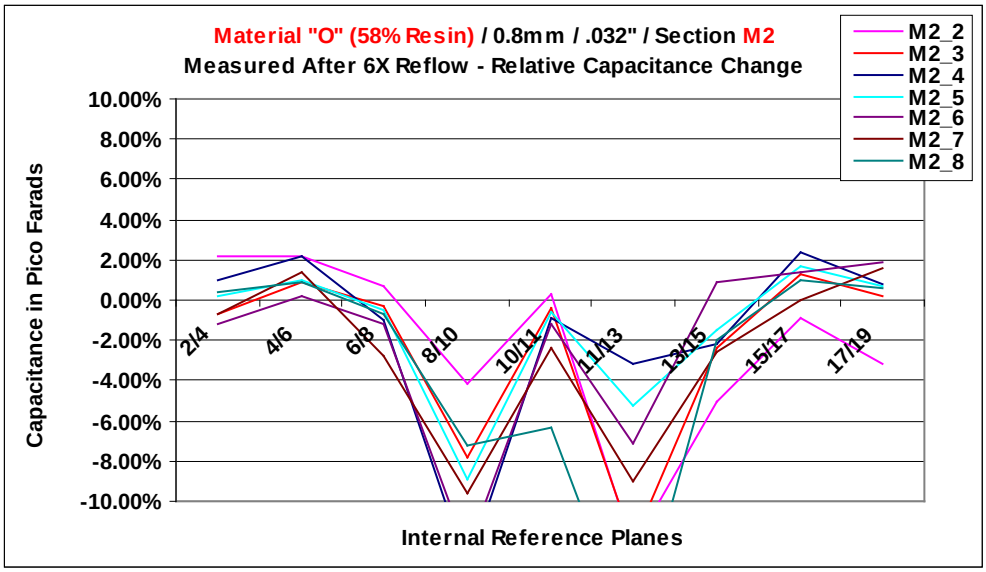


Figure 30

In order to understand the major influence that via-to-via spacing can have on the propensity to material damage, figure 31 shows the results from the 1mm/.040" coupons, built on the identical product (material "O"). Only two of the stressed coupons (#3 and #7) measured sufficient change to justify a reason to complete failure analysis. The relative change (6% to 8%) signifies that "lower-levels" of delamination should be anticipated between L8 to L10 and L11 to L13, which may not necessarily be widespread and present in all cases when multiple microsections are prepared.

Microsections were completed on all 25 material types to determine the correlation between the electrical results and the presence of material damage. Images 1, 2a and 2b show both low and high magnification photographs of the material "O" damage. Delamination is clearly evident within the central zone, image 2a and 2b also show smaller crack initiation below the large delaminated area.

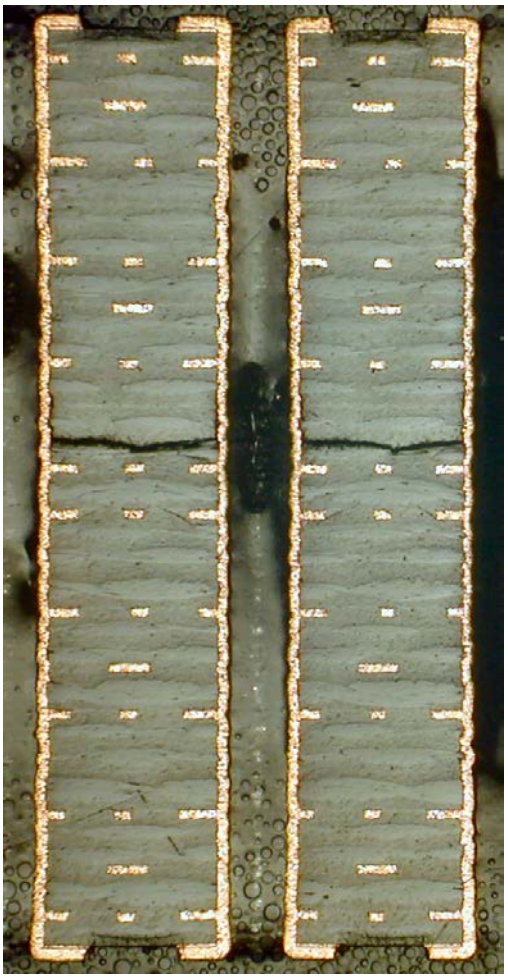


Image 1 - Material "O" - 0.8mm/.032 Grid

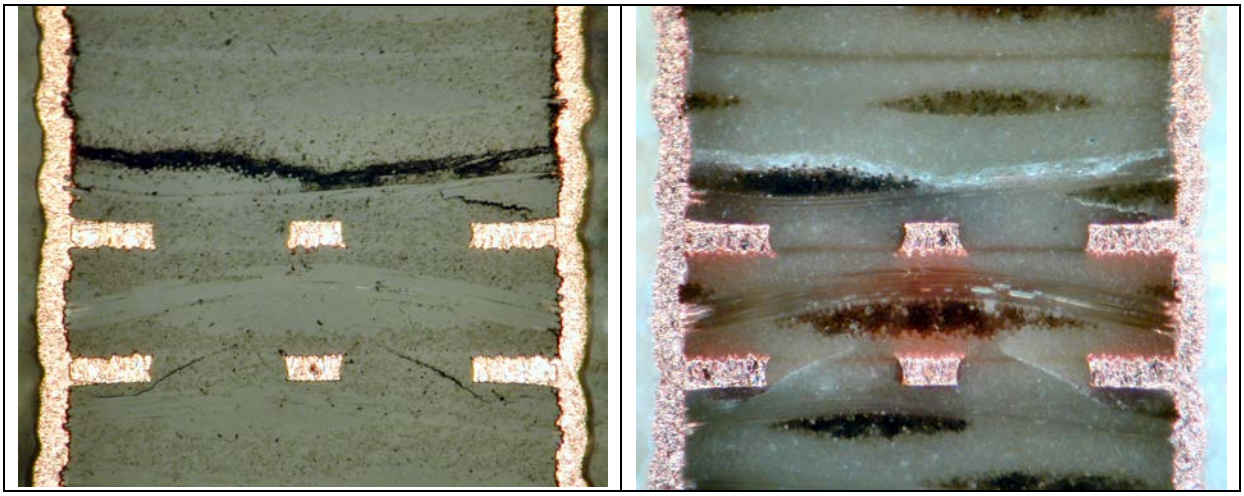


Image 2a **Image 2**

Normal field view **Dark field view**

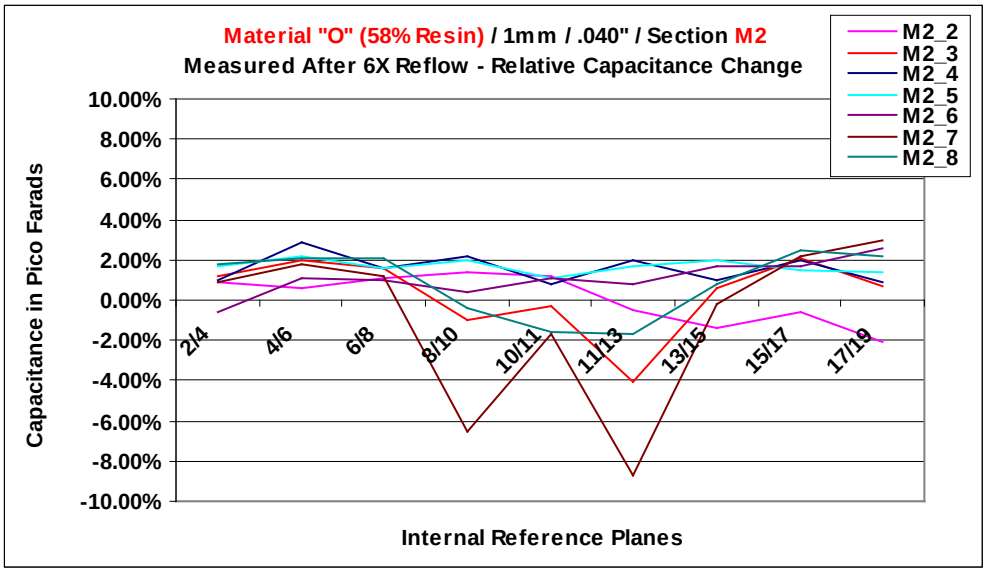


Figure 31

The capacitance data and microsections results for all 25 materials were collated; the two materials that were received with obvious delamination ("U" and "V") were not factored into this analysis. The data confirmed 10 materials failed on the 0.8mm/.032" grid coupons, only two coupons from materials "O" and "N" were found to contain material damage in the 1mm/.040" grid coupons. There was a 90%+ correlation related to confirming the presence of material damage between the electrical and microsection results.

The results of the testing after 6 passes through the SMT reflow oven demonstrated a lower level of damage compared to the microsection work completed after traditional 6x solder floats for ten seconds at 260°C and 288°C (IPC-TM-650 Method 2.6.8 Condition A). The results of this thermal stress methodology again demonstrated that the results from the visual examination of the samples were very dependent on which specific test coupon was being used. Figure 32 shows the results from a large volume of microsections that were produced from the multiple test vehicles designed into the MRT-3 test board. The capacitance and microsection results completed on the IST MAT coupons after 6 SMT reflow cycles compares well (but not perfectly) with the microsections exposed to 6 solder floats at 260°C. The coupons exposed to 6 solder floats at 288°C demonstrated increased damage that was not found in coupons processed through the reflow oven.

				Cross-sections after Thermal stressing											
				Internal Material Damage after 6X 260C reflow						Internal Material Damage after 6X 288C thermal shock					
Coding	Stackup	Resin Content (%)	Visual Delam after 6X Reflow	1mm ATC	0.8mm ATC	1mm IST	0.8mm IST	CAF - 16 mil HW-HW	CAF - 20 mil HW-HW	1mm ATC	0.8mm ATC	1mm IST	0.8mm IST	CAF - 16 mil HW-HW	CAF - 20 mil HW-HW
	FR4:														
A	A	58	No	No	No	No	No	HWS	HWS	No	MAJ	No	No	No	No
B	B	69	No	No	No	No	No	HWS	HWS	No	MAJ	No	No	No	No
C	A	58	No	No	No	No	No	MAJ	No	No	No	No	No	No	No
D	A	58	No	No	No	No	No	HWS	EB	No	No	No	No	No	No
E	A	58	No	No	No	No	No	No	HWS	No	MAJ	No	No	No	No
F	A	58	No	No	No	No	MED	EB	No	No	MAJ	No	No	MAJ	MAJ
G	B	69	No	No	No	No	MAJ	No	No	No	MAJ	No	No	No	No
H	A	58	No	No	No	No	No	No	HWS	No	MAJ	No	No	No	No
I	A	58	No	No	MAJ	No	MED	No	HWS	No	MAJ	No	No	No	No
J	A	58	No	No	MAJ	No	MAJ	MED	No	MAJ	MAJ	MAJ	MAJ	No	No
	Halogen Free FR4:														
K	A	58	No	No	No	No	MED	HWS	HWS	No	MAJ	No	No	HWS	No
L	B	69	No	No	No	No	No	HWS	HWS	No	MAJ	No	No	HWS	No
M	A	58	No	MED	MAJ	MAJ	MAJ	MAJ	MAJ	MED	MAJ	MAJ	MAJ	MAJ	MAJ
N	B	69	No	MED	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ
O	A	58	No	No	MAJ	No	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ
P	A	58	No	No	No	No	No	No	No	No	No	No	No	No	No
Q	A	58	No	No	MAJ	No	MAJ	HWS	HWS	No	MAJ	No	MAJ	HWS	No
R	A	58	No	No	No	No	No	HWS	No	No	No	No	MAJ	No	No
	High Speed Materials:														
S	A	58	No	No	No	No	No	No	No	No	MAJ	No	MAJ	No	No
T	B	69	No	No	No	No	No	No	No	No	No	No	No	No	No
U	A	58	No	EB	MAJ	MAJ	MAJ	EB	EB	MAJ	MAJ	EB	MAJ	EB	EB
V	A	58	Yes	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ
W	B	69	Yes	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	No	MAJ	MAJ	MAJ	MAJ	MAJ
X	A	58	No	EB	MAJ	No	MED	EB	No	No	MAJ	No	No	HWS	No
Y	A	58	No	EB	EB	EB	MAJ	EB	No	EB	EB	EB	MAJ	EB	EB
Z	B	69	No	No	EB	EB	MAJ	No	No	No	EB	No	MAJ	EB	No
AA	A	58	No	No	No	No	No	No	No	No	No	No	No	MAJ	No

HWS Hole Wall Separation > 20% is only defect found (note - <20% not listed)
Damage in Zone A only not listed
MAJ Major - Delamination, Cigar voids beyond zone A or Snake Delam
MED Medium damage - May or may not be rejectable (example - medium cigar void)
EB Eyebrow cracks beyond Zone A

Figure 32

Figure 32 confirms that material delamination was found in a total of 21 different materials following exposure to 6x 288°C, when using the 0.8mm/.032" grid ATC coupon design.

This result contradicts the microsection analysis results when using both the IST and CAF coupons, the ATC coupon failed an additional 11 materials. A design review was completed to understand if any coupon lay-out differences existed that may explain the situation. The ATC coupon contains no internal planes, unlike the IST and CAF coupons which are designed with a strip-line configuration. The absence of internal copper would reduce the thermal transfer, creating a larger temperature delta between the surface and the central layers. The resulting CTE mis-match would create an increased level of shear stress, which would be focused at the centre of the construction.

The 10 Materials which demonstrated damage were identified and changes were made to the coupon selection protocol for via reliability testing. In most cases the 0.8mm/.032" coupons were withdrawn from air to air testing (but not IST testing due to the small sample size available), the rejected coupons were replaced with 1mm/.040" coupons. When the statistical analysis for the correlation between the IST method and Air to Air thermal cycling method were being completed consideration was given with the knowledge that certain coupons were known to contain material delamination and that difference with the coupon grid sizes were being compared.

Figure 33 identifies the overall results from capacitance testing and microsections taken from the same coupons. A failure analysis report (only available to consortium members) was drafted with multiple images from the microsections produced from all materials types.

Material #	0.8mm / .032" Grid		1mm / .040" Grid	
	Delam Y/N	Type	Delam Y/N	Type
FR4				
A	N	N/A	N	N/A
B	N	N/A	N	N/A
C	N	N/A	N	N/A
D	N	N/A	N	N/A
E	N	*Vertical	N	N/A
F	Y	Barrel to Barrel	N	*Vertical
G	Y	Barrel to Barrel (2 of 8)	N	N/A
H	N	N/A	N	N/A
I	N	N/A	N	N/A
J	Y	Barrel to Barrel (2 of 8)	N	N/A
Halogen Free FR4				
K	N	N/A	N	N/A
L	N	N/A	N	N/A
M	Y	Barrel to Barrel	N	N/A
N	Y	Barrel to Barrel	Y (2 of 8)	Barrel to Barrel
O	Y	Barrel to Barrel	Y (2 of 8)	Barrel to Barrel
P	N	N/A	N	N/A
Q	Y	Barrel to Barrel	N	N/A
R	N	N/A	N	N/A
High Speed Material				
S	Y	Micro Crack	N	N/A
T	N	N/A	N	N/A
U	Y	Barrel to Barrel	N	N/A
V	Y	Catastrophic	Y	Catastrophic
W	Y	Catastrophic	Y	Catastrophic
X	Y	Barrel to Barrel	N	N/A
Y	N	N/A	N	N/A
Z	N	N/A	N	N/A
AA	N	N/A	N	N/A

Figure 33

Following a review of all data, certain trends became evident:

a) The dominant level of damage was found (electrical data and microsections) in the 0.8mm/.032" grid coupons. Only sporadic material damage was found in two materials with the 1mm/.040" coupon design.

b) All material damage was found within the central zone between layers L8 and L13, and was not visible from the surface layers.

c) Careful consideration must be given for coupon design when testing small grid arrays using the 6x at 288°C solder float test methodology, false negatives can result.

d) The non-destructive DELAM test protocol proved both effective and correlated to traditional solder float methodology for identifying the presence of material damage.

e) Using the minimum of 4% decrease in bulk capacitance as an electrical specification demonstrated the ability to identify material damage; additional work is required to confirm this specification with an increased level of products and materials.

Dielectric thickness estimation and measurement

It is standard practice in the PWB industry to complete multiple microsections to confirm the construction of the manufactured products, using an electrical test methodology that confirms that all production panels are built with the same construction would permit a cost saving by reducing the total number of sections required. The measured data also creates an effective statistical reference that can be used every time additional lots of the same part number are produced.

Converting the capacitance data into predicted/estimated dielectric thickness measurements can be easily achieved by completing an initial microsection on one of the electrically measured coupons. Algorithms are established from the statistical relationship between the measured capacitance, measured dielectric and the common area between the two planes (plates), to establish an effective Dk. Plots, graphs and statistical analysis are generated that enable thickness predictions of critical dielectric layers for all remaining coupons.

It should be emphasized that a measured microsection traditionally records a value specifically related to a designated test coupon, this coupon should be representative of the products construction in order to simulate the resin flow characteristics that determine the effective dielectric thickness. The measured value is relative to a number of factors related to copper density, the primary influences are quantity of over-lapping copper layers, copper weights, the ability of the B stage resin to flow and achieve both insulation and encapsulation.

The bulk capacitance measurement technique is different in respect that the measurement and predicted thickness determinations are based on a relatively large surface area; specifically the geometries associated to the size of the copper planes in the test coupon. The bulk capacitance determines the "average" dielectric thickness over the length and width of the plate; it is considered that this approach is more effective at quantifying the representative dielectric environment for use in the critical impedance calculations that are used when modeling and calculating the dielectric thickness for high speed lines.

Previous sections have identified how the capacitance is automatically collected from the MRT-3 test coupon, figure 34 illustrates the capacitance measurement data collected from the M1 section, and this enables the ability to predict the copper to copper dielectric thickness measurements for all layers within the construction. Data collection should be taken from coupons that have not experienced any thermal stressing; this avoids the added complication of possible material damage that can impact the correlation between capacitance and microsection measurements. The combination of data should ideally be taken from the same coupon, but if the capacitance data confirms consistent measurement (construction) any coupon from the lot may be microsectioned.

Layers	Measured Dielectric in Mils	Measured Capacitance in Pf
1-2	0.00298”	210.0
2-3	0.00521”	184.2
3-4	0.00508”	188.9
4-5	0.00523”	183.5
5-6	0.00497”	193.2
6-7	0.00515”	186.4
7-8	0.00497”	193.2
8-9	0.00523”	183.5
9-10	0.00484”	198.6
10-11	0.00506”	189.6
11-12	0.00486”	197.6
12-13	0.00510”	188.4
13-14	0.00488”	196.9
14-15	0.00510”	188.3
15-16	0.00478”	200.9
16-17	0.00512”	187.6
17-18	0.00483”	198.7
18-19	0.00496”	193.5
19-20	0.00299”	231.8

Figure 34

Figure 35 illustrate how the same capacitance values and the dielectric thickness measurements can be graphed to demonstrate their relationship. Microsection measurements confirmed the majority of B and C stage dielectric layers measured between .00475” (0.12mm) and .00525” (0.135mm), with the exception of the outer layer measurements of .003” (0.08mm).

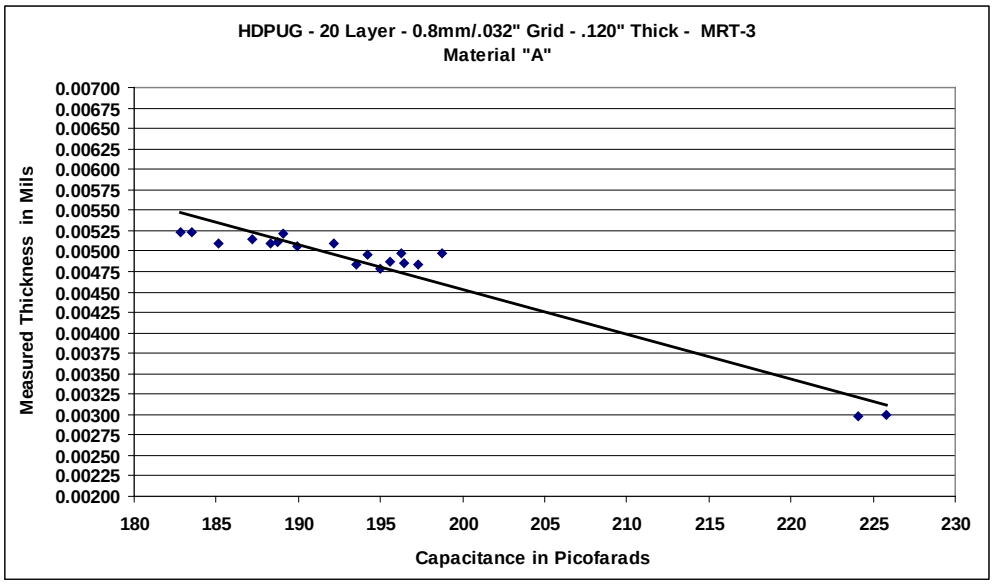


Figure 35

Knowing the capacitance value, the dielectric thickness and the plate area, the only unknown variable is the determination of the materials “effective Dk”. The formula establishes a factor that is used in the algorithm, if the same materials are used throughout the construction the same factor can be applied for each dielectric layer. If different types of materials are used (E.g. Flex-rigid would contain FR4 and polyimide) a separate factor for each material type will need to be determined.

The effective Dk can be calculated with the combination of: the geometry of the plates, the measured capacitance and the known dielectric spacing between the plates.

$\varepsilon_r \varepsilon_0 = C\ (D/A)$

The predicted dielectric thickness can be calculated with the combination of: the geometry of the plates, the measured capacitance and the previously calculated "effective Dk".

$D = A\ (\varepsilon_r\ \varepsilon_0) / C$

Based on the above equations the bulk capacitance values can now be converted into dielectric thickness. Figure 35 shows the constructions of 8 coupons built with the same material ("A"), the data now provides the user with the capability to review each dielectric layer to understand where material construction differences may exist. This information would prove very useful for electrical designers and PWB manufacturers to better understand the inherent variability's of the materials and processing conditions.

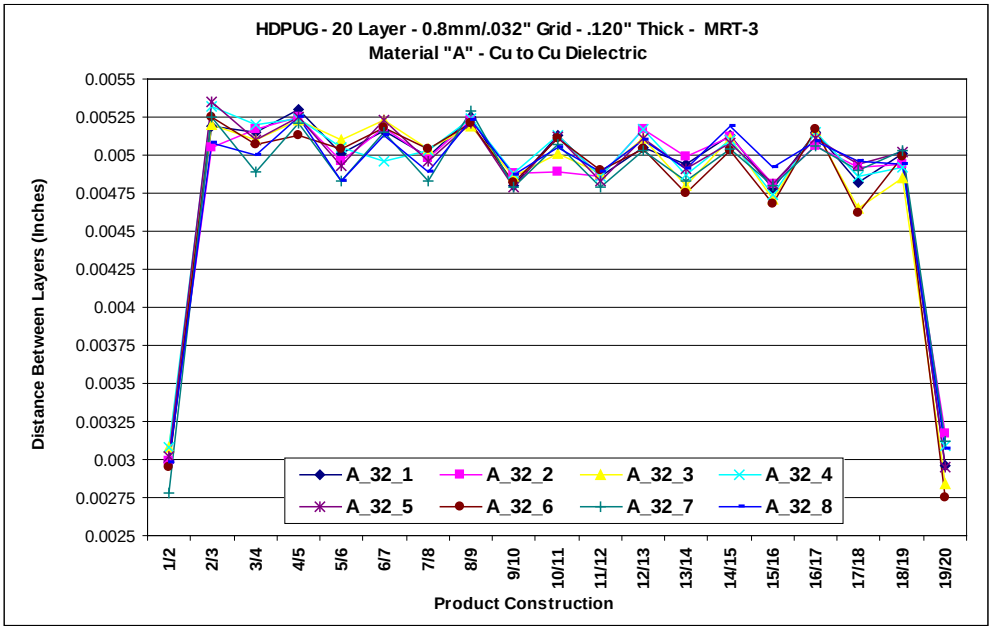


Figure 35

Appendix D (only available to consortium members) includes graphs for each material type, comparing capacitance profiles (0.8mm/.032" grid size), for the M2 sections. The data shows the calculated mean thickness with the actual measured thickness and all coupons predicted thickness' to the one measured coupon.

Figure 36 gives a further example of predicted thickness for coupons built with a material using a 69% resin content construction, where the dielectric thickness ranged between .0045" (0.115mm) and .0065" (0.17mm), with the exception of the outer layer measurements of .0035" (0.09mm). The coupon to coupon variability has increased to approximately .0005" (0.0127mm), which represents an effective 10% variance within the B stage dielectric thickness.

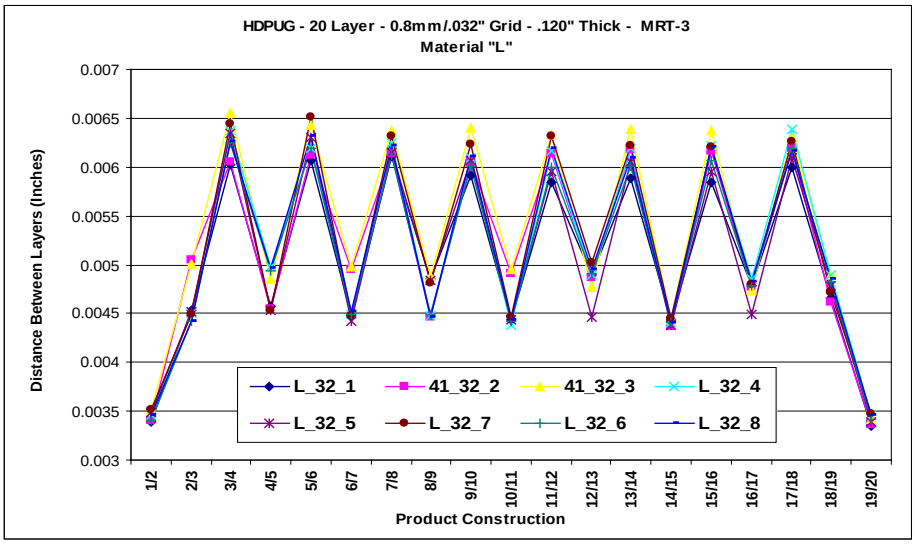


Figure 36

Once the user's confidence has determined the relationship/correlation between the capacitance measurement and microsection thickness measurements it is the PWB manufacturer's decision which technique offers the greatest advantage for decision making on product construction. Important Considerations: The capacitance measurement is non-destructive, the thickness profiles can be established within minutes rather than the several hours and cost associated with excessive microsection analysis. Secondly, using the capacitance profiles creates a baseline reference for subsequent measurements to be taken after exposure to elevated temperatures experienced during the assembly and rework phase. Thirdly, the capacitance data combines the influences of dielectric thickness and material Dk; ultimately it is the electrical environment (not the absolute dielectric thickness) that is crucial for producing controlled impedance products.

Following a review of all data, certain trends became evident:

1) Converting capacitance measurements into correlated thickness measurements is a non-destructive, fast, low cost option over traditional microsectioning.
2) Presently levels of microsectioning and their associated costs could be dramatically reduced, creating important savings in the area of product assurance.
3) Presently the data collected from microsection analysis is rarely collated or compared to understand product or process variability; using capacitance conversion data greatly increase this potential.
4) Creating statistically comparable product thickness profiles enables the end use customer to quantify that each production lot is built with the same construction.
5) The PWB manufacturer can immediately review product construction information to better understand the variances of supplied materials and the influence of processing equipment and conditions.
6) Modeling for controlled impedance products would benefit both electrical designers and PWB manufacturers because of the improved understanding and quantification of material and manufacturing tolerances.

Study Conclusions:

a) The MRT-3 IST test coupon design proved to be a very effective test vehicle for non-destructively understanding multiple aspects of material performance through Pb free assembly, characterizing material variability and predicting dielectric thickness.
b) Material damage through Pb free assembly confirmed the dominant level of damage/delamination was found (using electrical and microsection analysis) in coupons designed on a 0.8mm/.032" grid.
c) Twelve of the 27 materials proved unsuitable for 6X 260°C Pb free assembly, specifically on the 0.8mm/.032" grid size.
d) The result of conventional 6X solder float testing to 288°C can be strongly influenced by the test vehicle/coupon design.
e) Although each material supplier was instructed to build the same glass/resin configuration each construction measured different (unique) profiles, each demonstrating different degrees of consistency between the C and B stage dielectrics.
f) Changes within a coupons dielectric layer were easily identified; the non-destructive techniques demonstrated an effective capability to discern small changes within the dielectric thickness.
g) Each B-stage dielectric (in the majority of cases) measured between 2x and 4x variability compared to the C stage dielectrics (for the same material). The data ranged from virtually identical results for all coupons (both grids), to a maximum of 15% difference between the 8 coupons from each grid size.
h) Based on the small sample size and understanding that each material was being compared based on a single production lot, increased variability should be anticipated if either a larger sample size or multiple production lots were factored into the equation.

References:

[1] Smetana, Joe, Sack, Thilo, Rotschild, Wayne, Birch, Bill, and Morton, Kim, “Bare Board Material Performance after Pb-free Reflow”, IPC/APEX, Las Vegas, NV, 2009.

[2] W Rothschild and J Kuczynski, “Lessons Learned About Laminates during Migration to Lead-free Soldering,” S30-1, Proceedings of IPC Expo 2007. Reproduced (without references) in OnBoard Technology, November 2007

[3] G Tennant, M Kelly, W Rothschild and A Khan, “Lead-free Laminates: Surviving Assembly & Rework Processes to Deliver High Quality and High Reliability Products,” CMAP Lead-free Conference 2005

[4] C. Xu, R. Kopf, J. Smetana, D. Fleming, “Moisture Sensitivity and Its Effect on Delamination”, IPC/APEX, Las Vegas NV, 2011.

[5] Smetana, J., Birch, B., Sack, T., Morton, K., Yu, M., Katzko, C., Helminen, E., Luo, L. “Reliability Testing of PWB Plated Through Holes in Air-to-Air Thermal Cycling and Interconnect Stress Testing after Pb-free Reflow Preconditioning”, IPC/APEX, Las Vegas NV, 2011

[6] Morton, K, Smetana, J., “The Effects of Reflow on Conductive Anodic Filament (CAF) Performance of Materials”, IPC/APEX, Las Vegas NV, 2011

[7] Smetana, J., Birch, B., Rothschild, W., “A Standard Multilayer Printed Wiring Board for Material Reliability Evaluations”, IPC/APEX, Las Vegas NV, 2011.

Electrically Quantifying Product Construction and Material Robustness

Bill Birch

April 2011

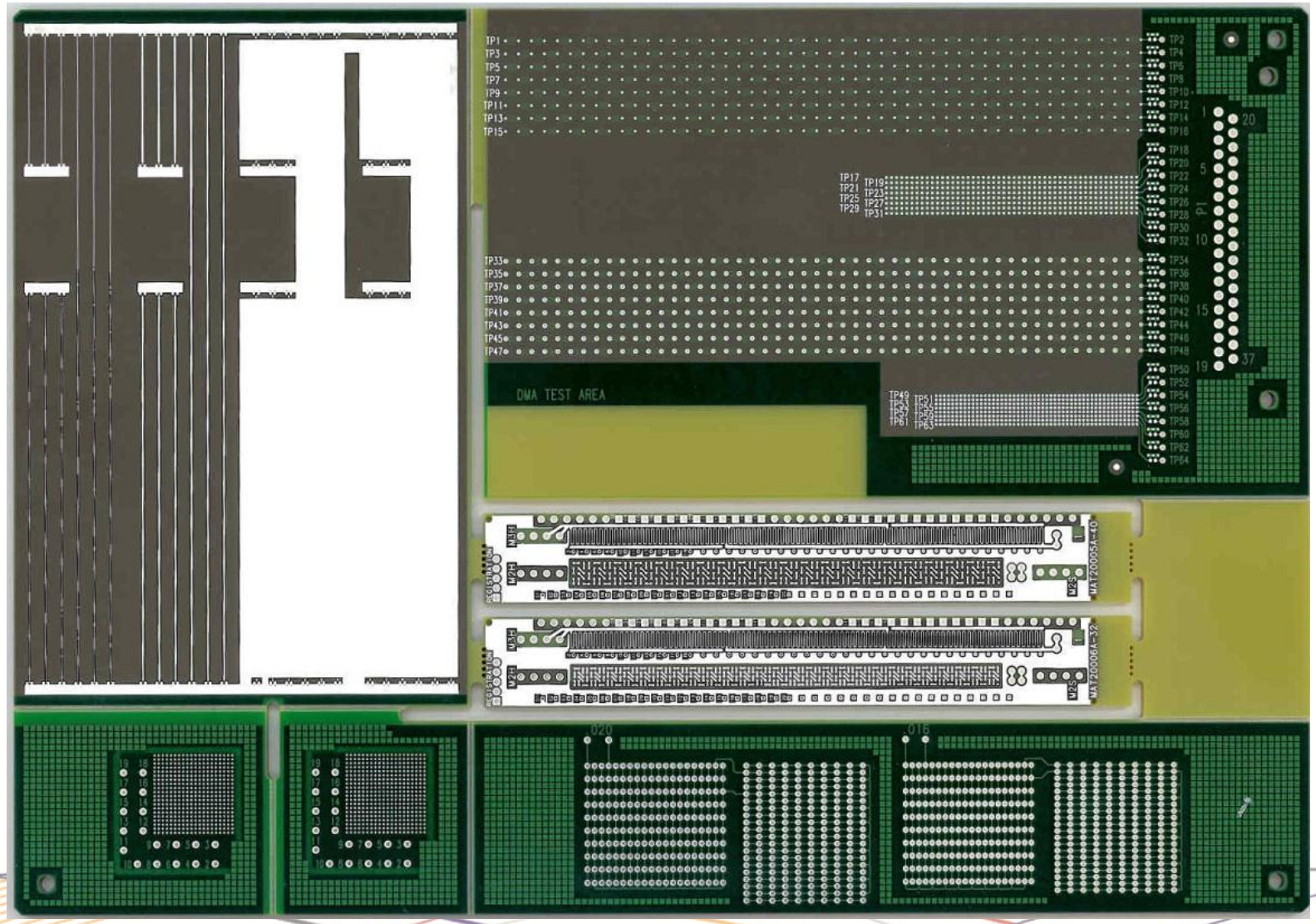
High Density Product User Group (HDPUG) Phase 2 - Lead-Free Study

- Purpose – Measure the ability of 27 lead free compatible materials to Survive 6X 260°C Assembly
- 20 Layers, 2.9mm Thick, 0.25mm drilled PTH, 0.15mm single level microvia, 1mm and 0.8mm grid, IAg Finish, 2 resin constructions, built by 3 Asian PWB
- Celestica performed 6X Reflows to 260°C, through 10 zone SMT convection oven.
- Correlate Via Reliability, Measure Material Damage, CAF, WIC, DMA/TMA

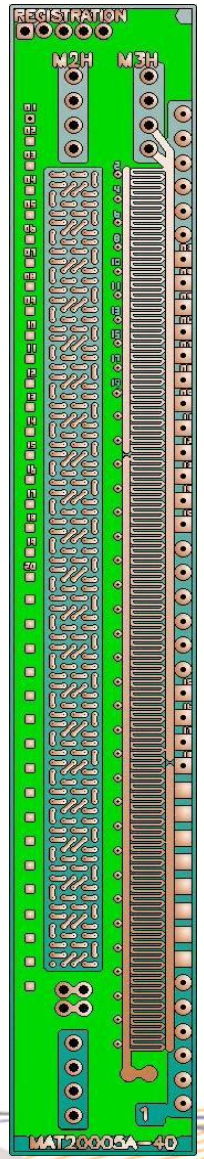
HDPUG Lead-Free Study Responsibilities

- Confirm Each Material was Produced With Similar Glass/Resin Constructed Materials
- Determine Variability Across Each Group of Coupons (1mm and 0.8mm Via Spacing)
- Establish Correlation Between Measured Dielectric Thickness and Capacitance Predictions
- Identify If Material Damage/Delamination was Present Following 6X Reflows to 260°C

MRT-3 Test Vehicle



MRT-3 IST DELAM Test Coupon Design



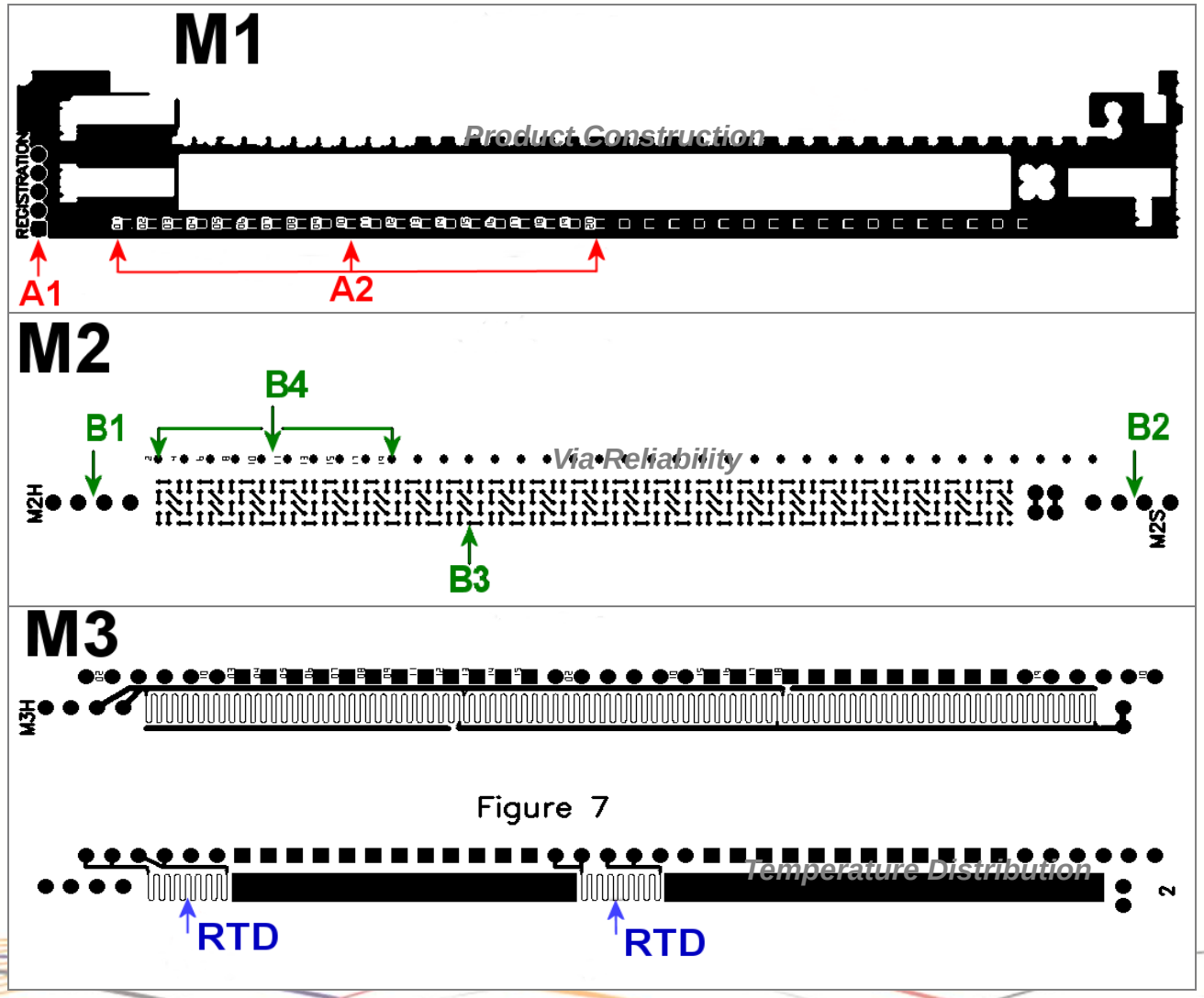


Figure 7

Product Construction

Via Reliability

Temperature Distribution

Automated Measurement and Profiling

Dielectric

Estimation

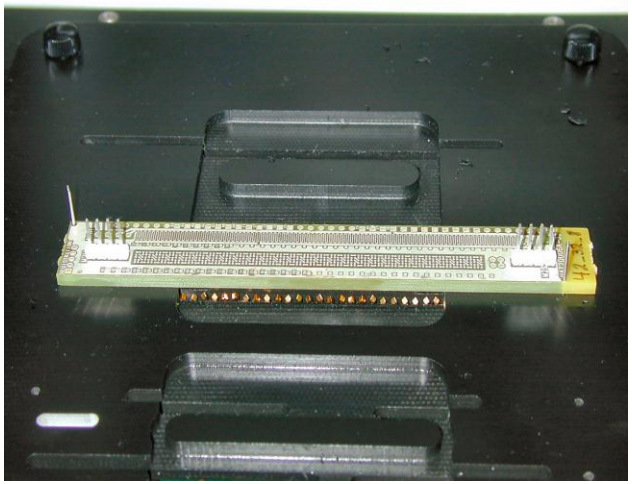
Laminate

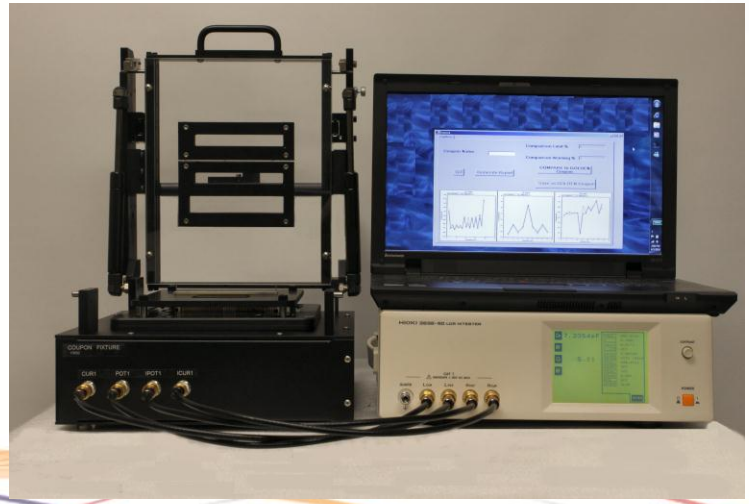
Assessment

Method

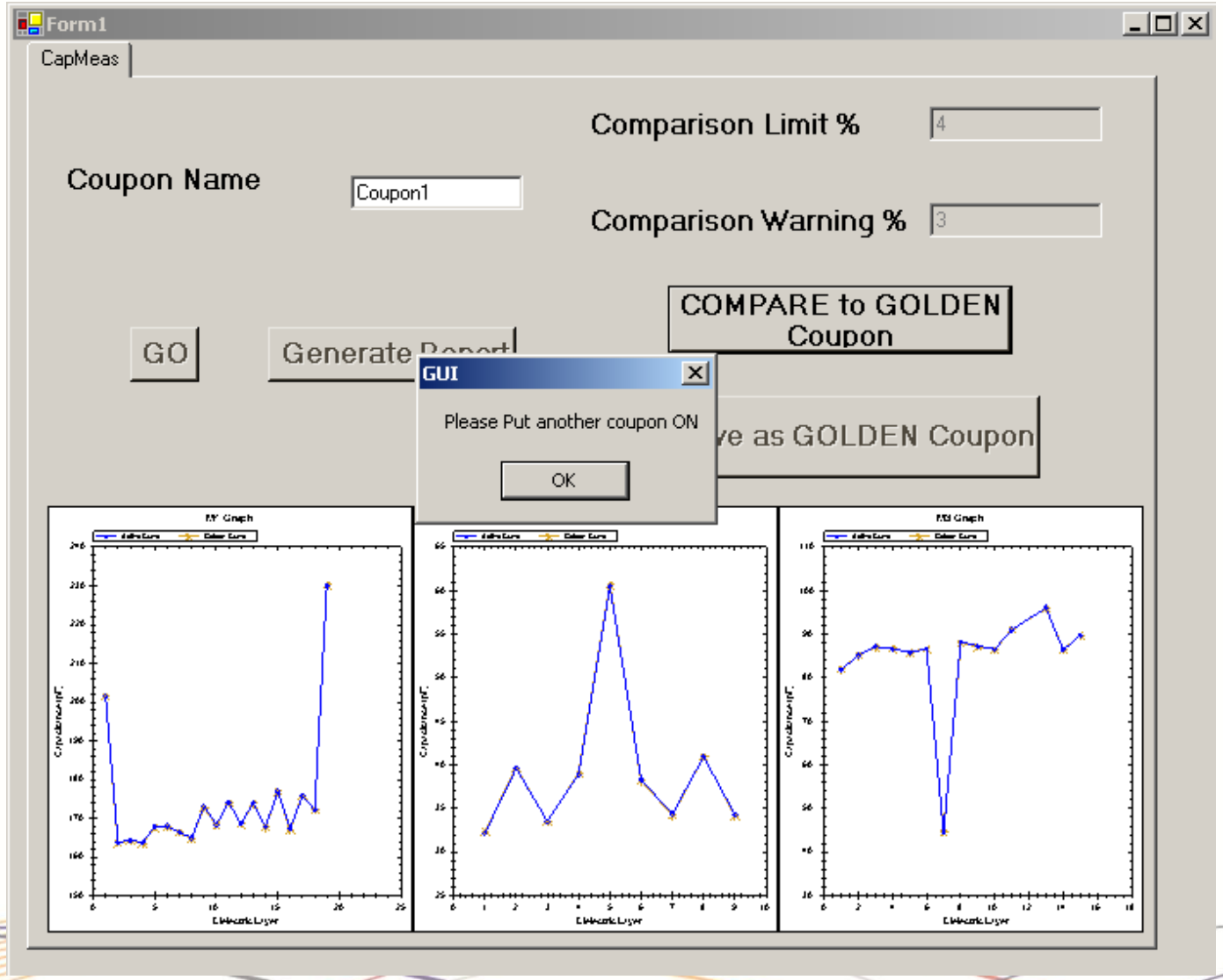
20,000+ Data Point Compared

Custom Designed Test Fixture

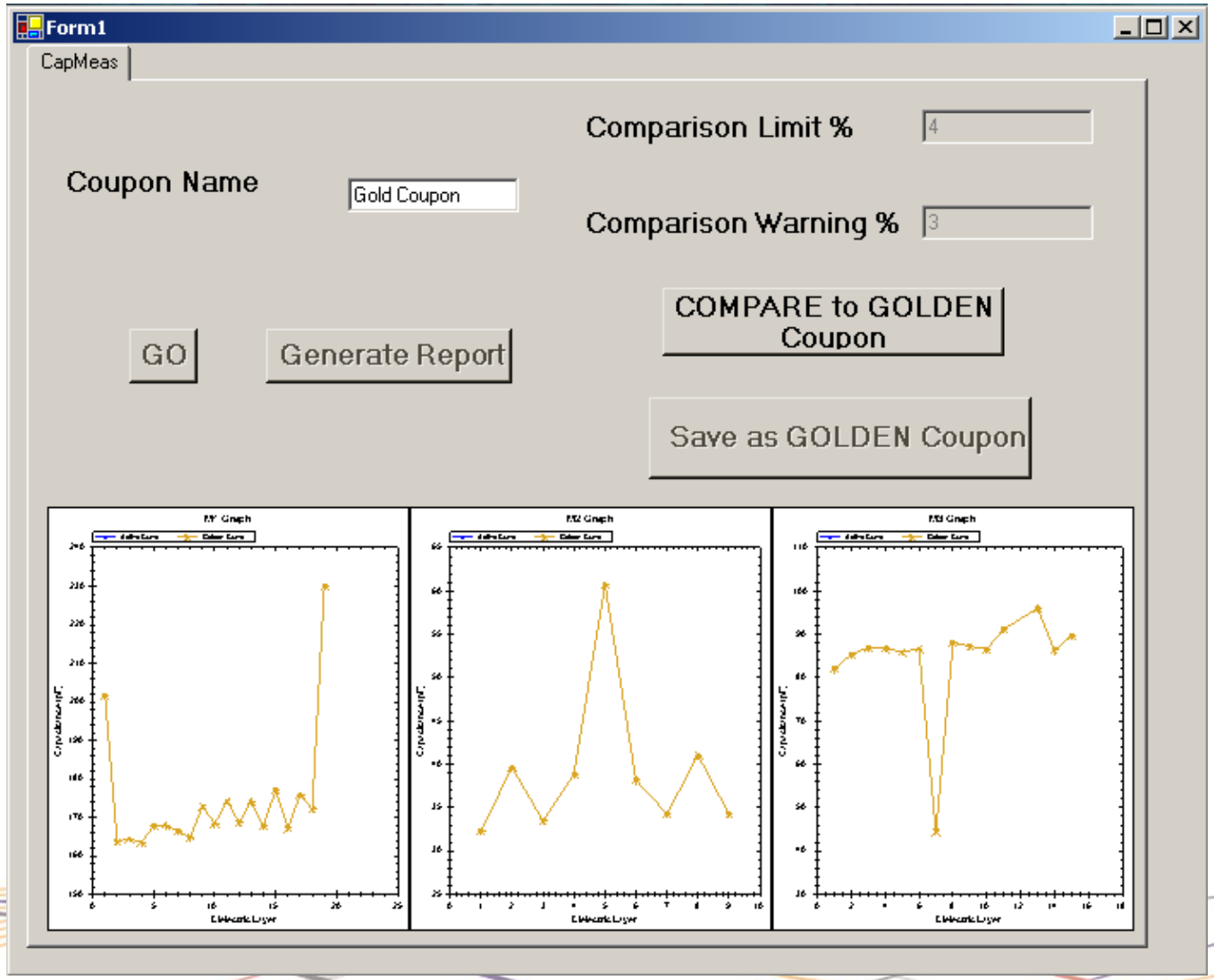




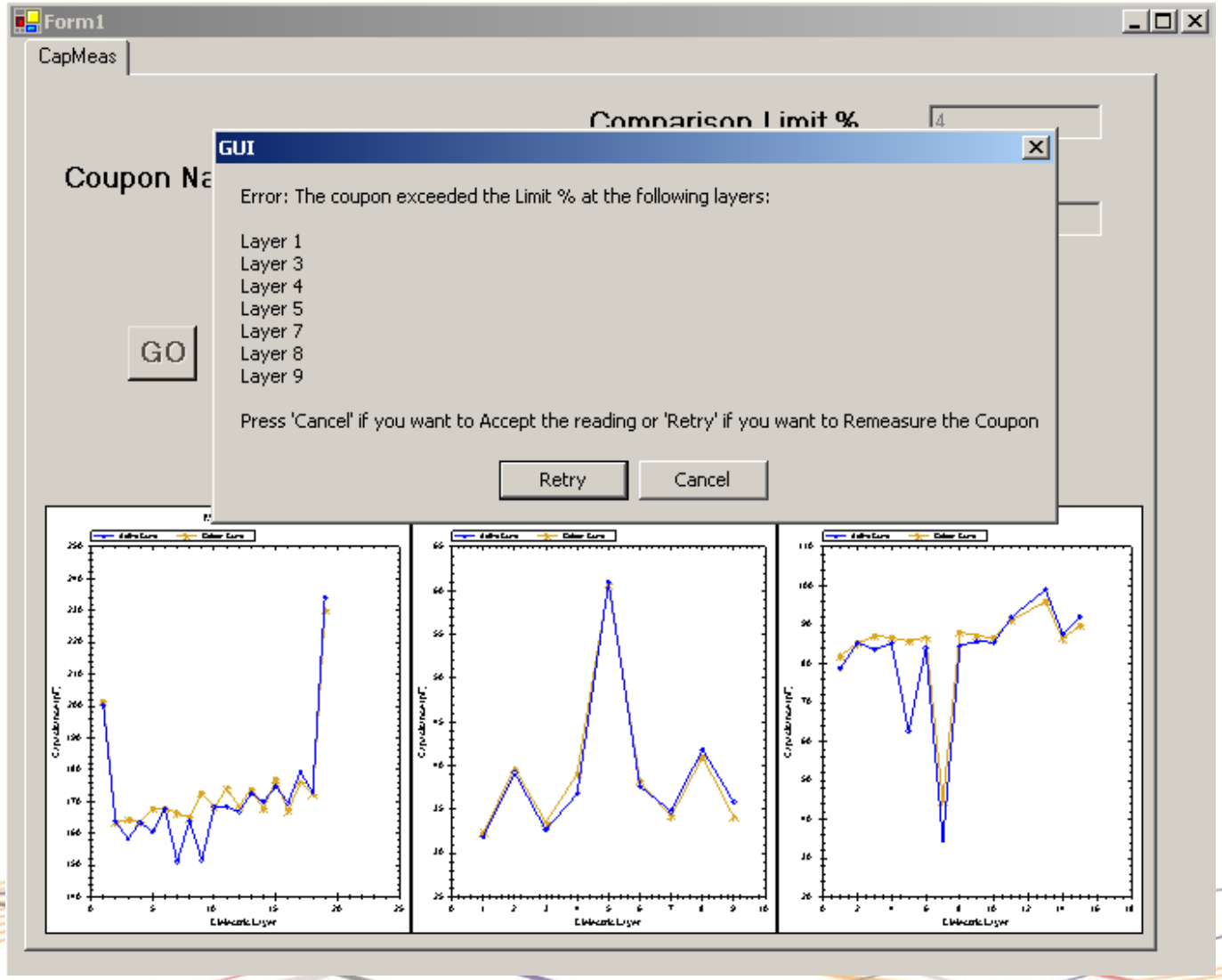
Capacitance Profiling of 3 Different Sections



Establish Product Profile – As Received



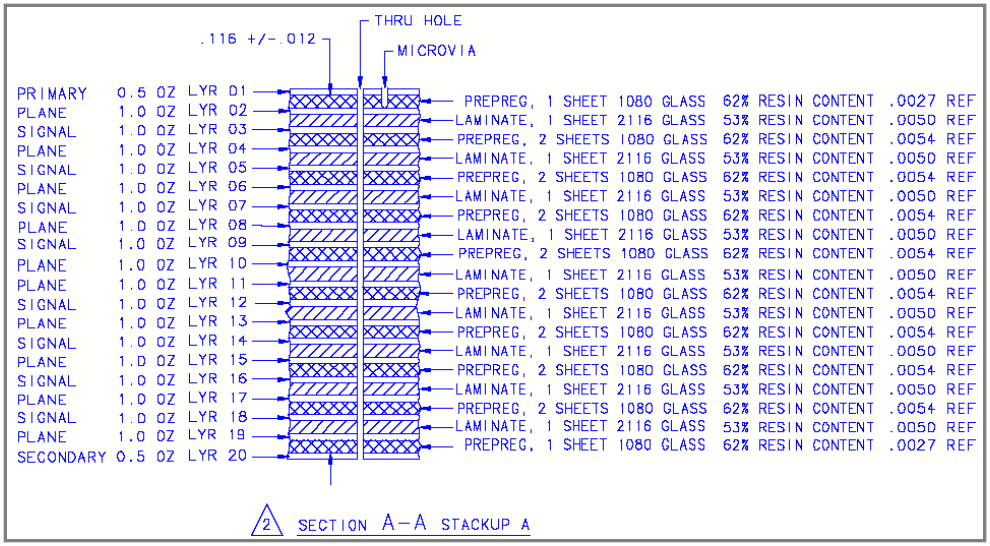
Compare Product Profile – After Assembly



27 Materials Tested in Lead-Free Impact Study

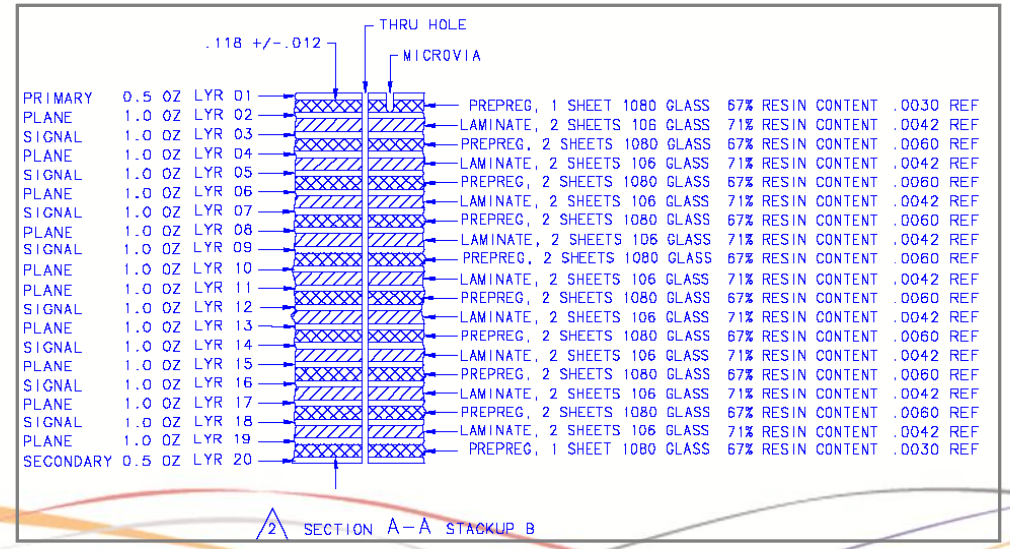
Coding	Stack-up	Resin Content (%)	Description
FR4			
A	A	58%	Filled Phenolic FR4
B	B	69%	
C	A	58%	
D	A	58%	
E	A	58%	
F	A	58%	
G	B	69%	
H	A	58%	
I	A	58%	
J	A	58%	
Halogen Free			
K	A	58%	Filled Halogen Free FR4
L	B	69%	
M	A	58%	
N	B	69%	
O	A	58%	
P	A	58%	
Q	A	58%	
R	A	58%	
High Speed			
S	A	58%	High Speed Material
T	B	69%	
U	A	58%	
V	A	58%	
W	B	69%	
X	A	58%	
Y	A	58%	
Z	B	69%	
AA	A	58%	

20 layer Construction “A” and “B”

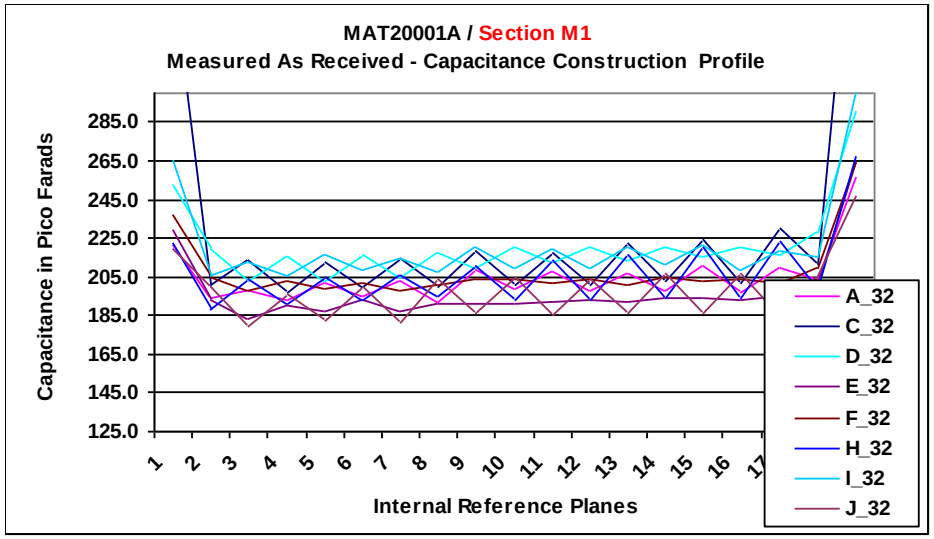


58% Resin Content

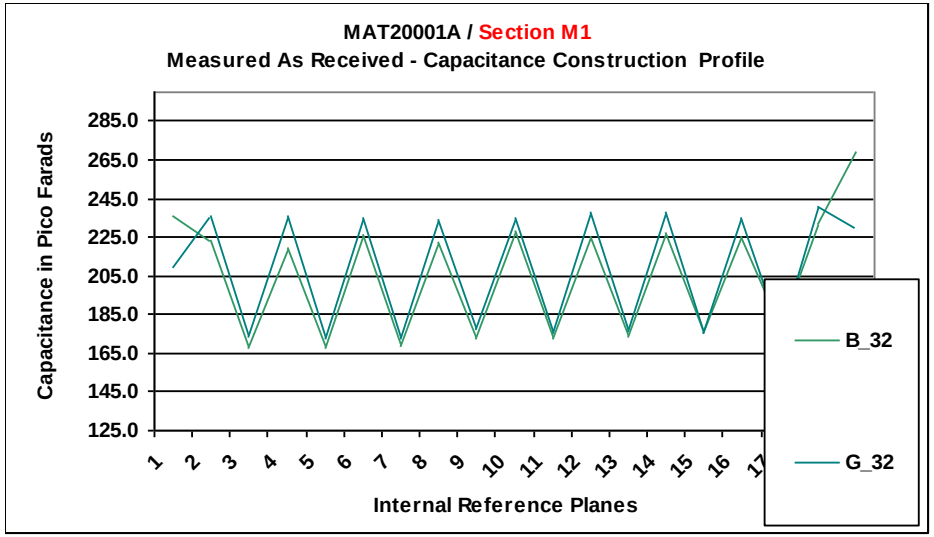
69% Resin Content



Comparison of Constructions For
FR4 Materials

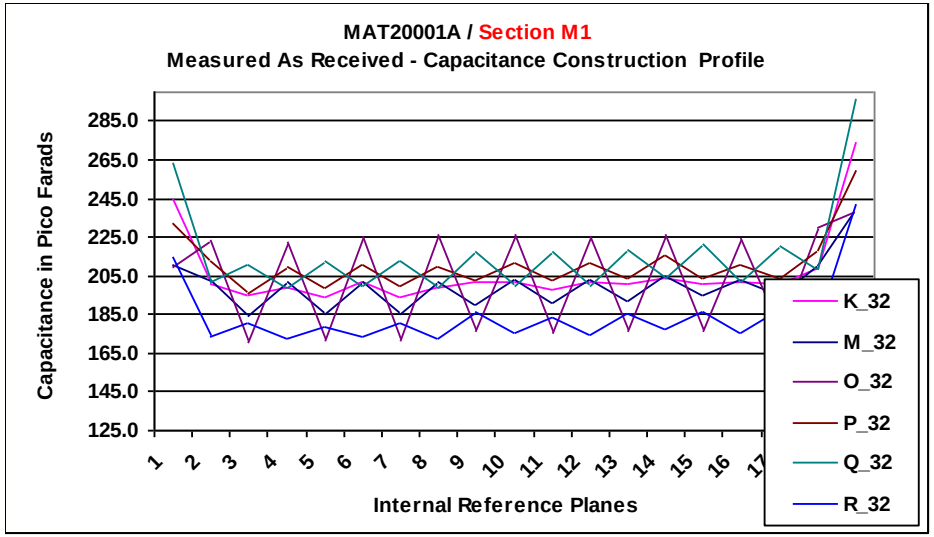


8 Products with "A" Stack-up (58%)

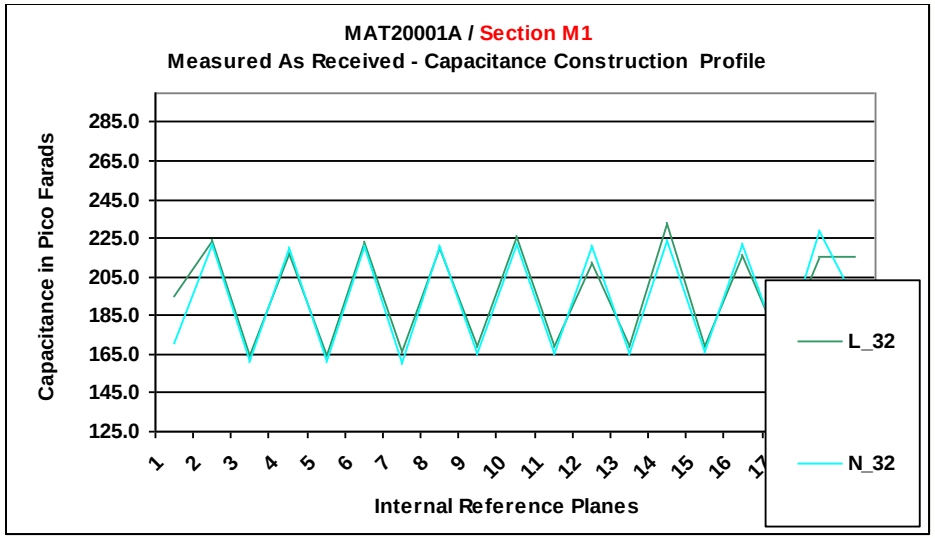


2 Products with "B" Stack-up (69%)

Comparison of Constructions For
Halogen Free Materials

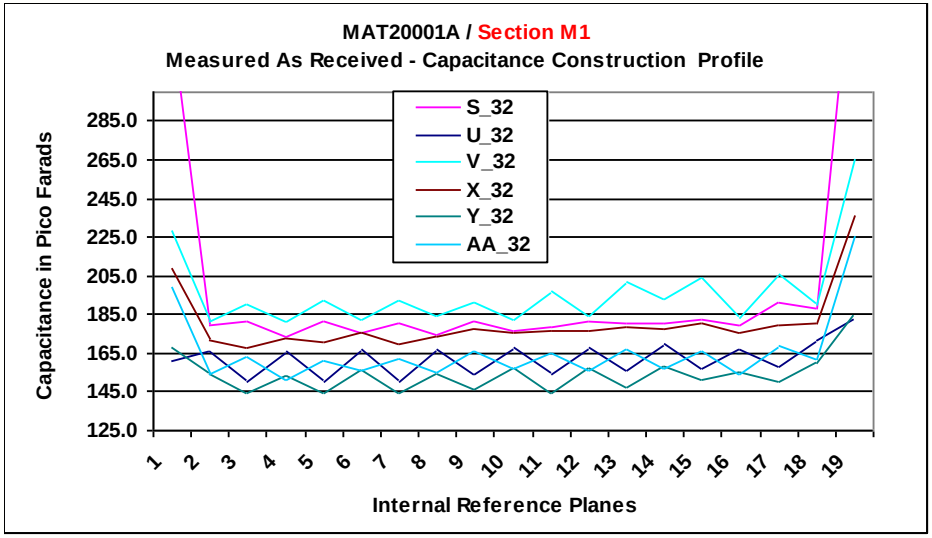


6 Products with "A" Stack-up (58%)

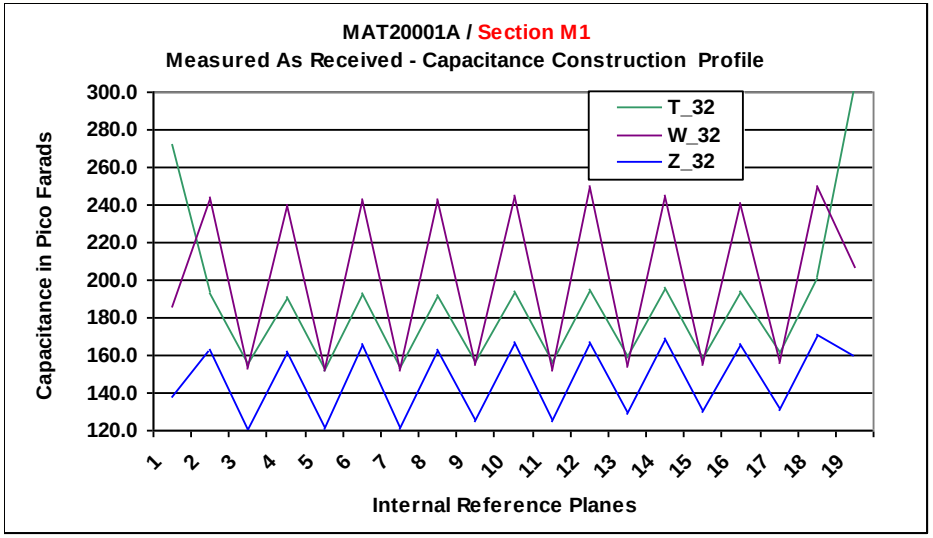


2 Products with "B" Stack-up (69%)

Comparison of Constructions For
High Speed Materials

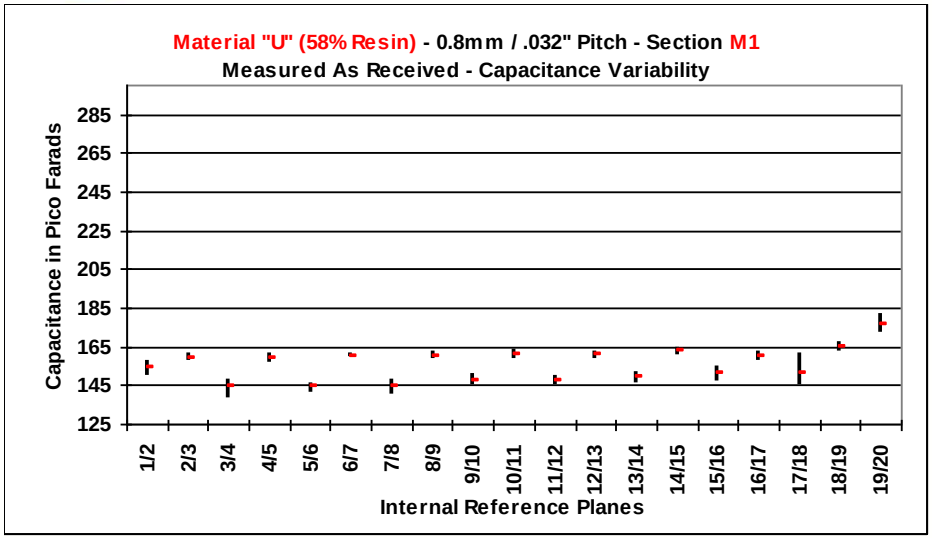


6 Products with "A" Stack-up (58%)

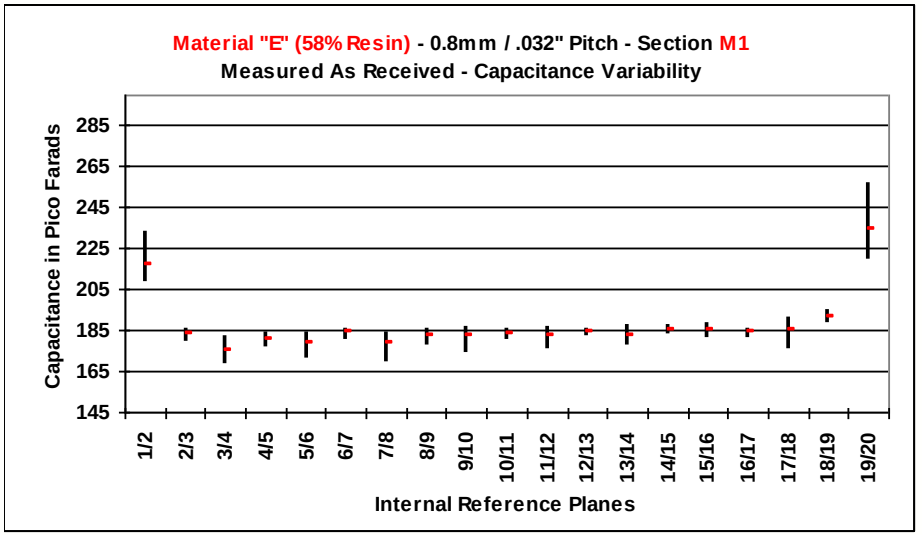


3 Products with "B" Stack-up (69%)

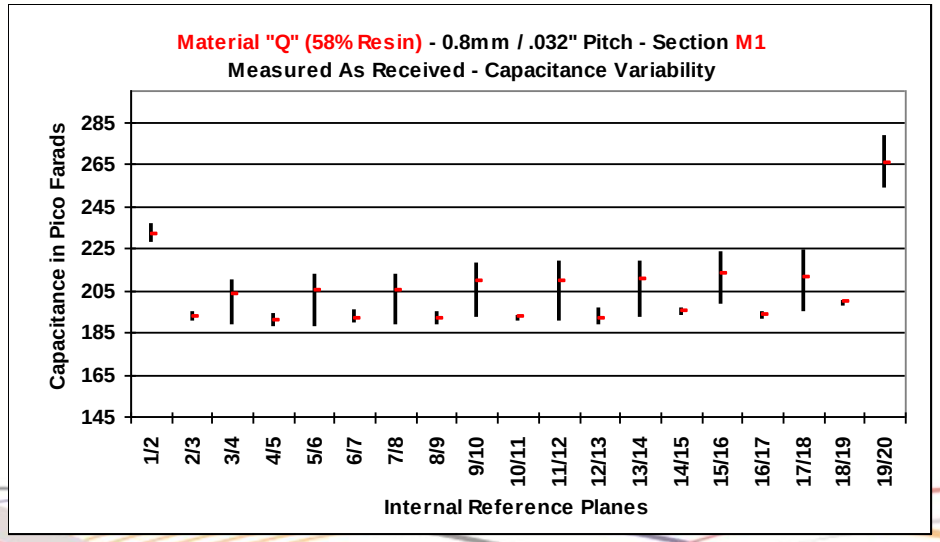
Comparing Variability's Within Each Material



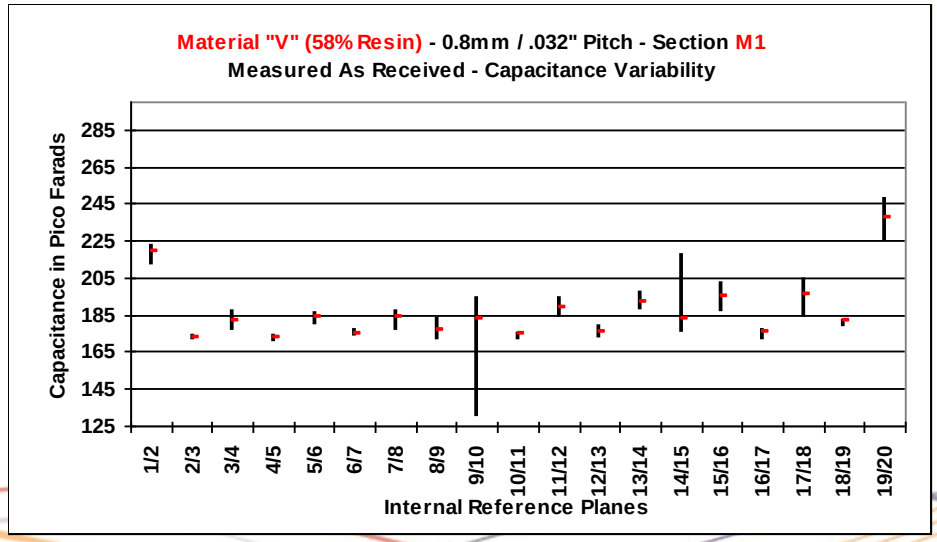
Stable/Predictable Material



Outer Layer Variability

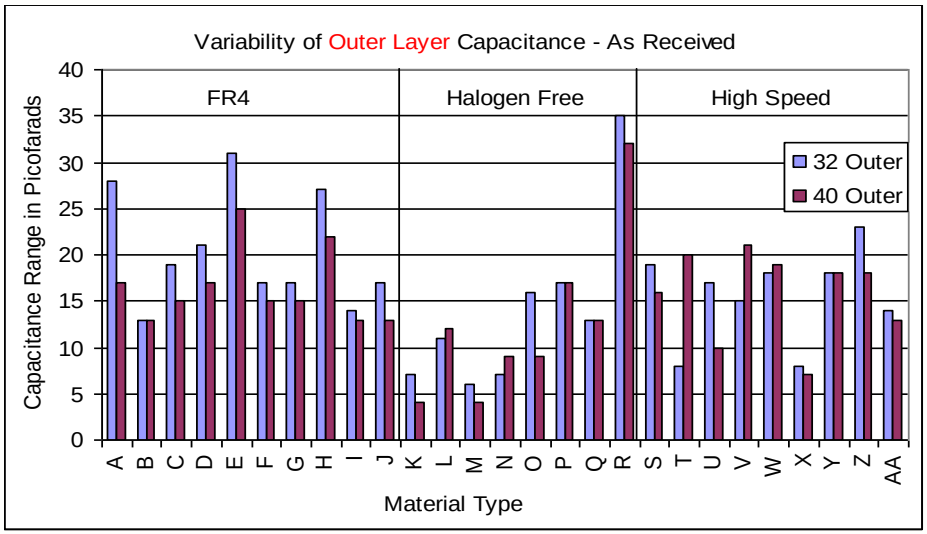


B-Stage Only Variability

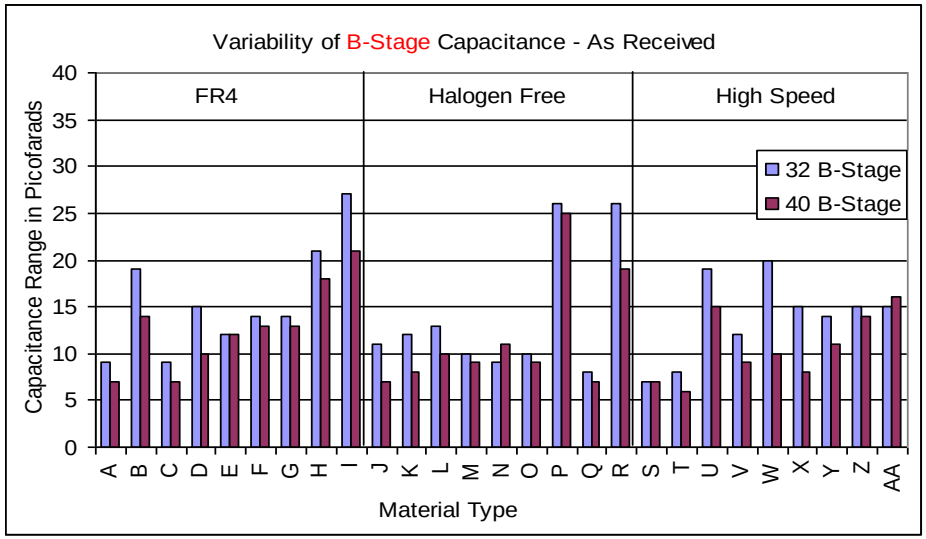


Damaged Material

Comparison of Outers Layers and B-Stage

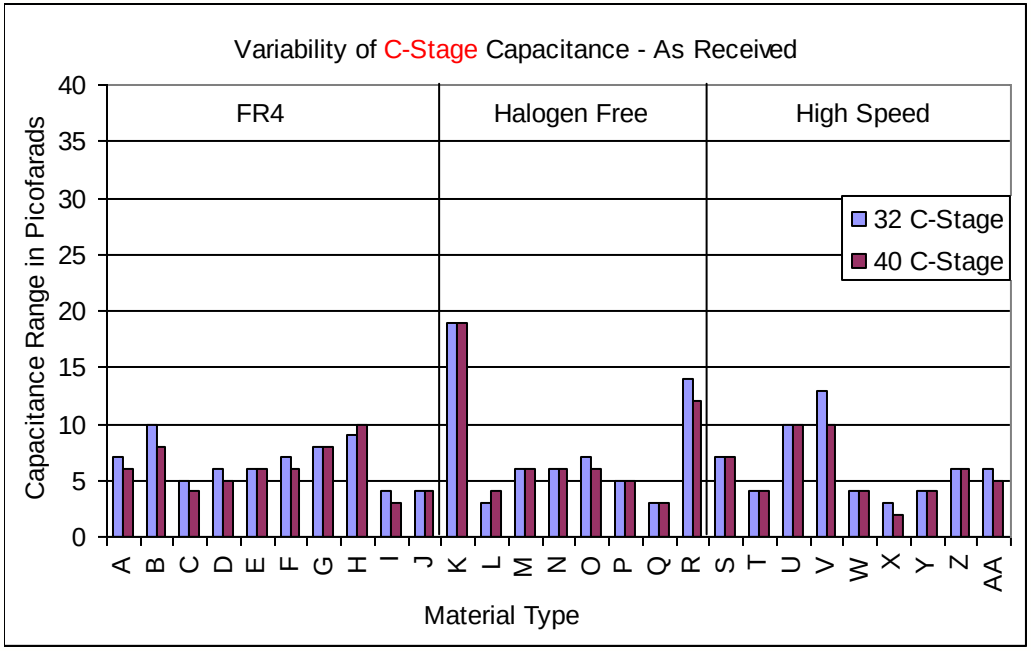


27 Products Outer Layers Variability



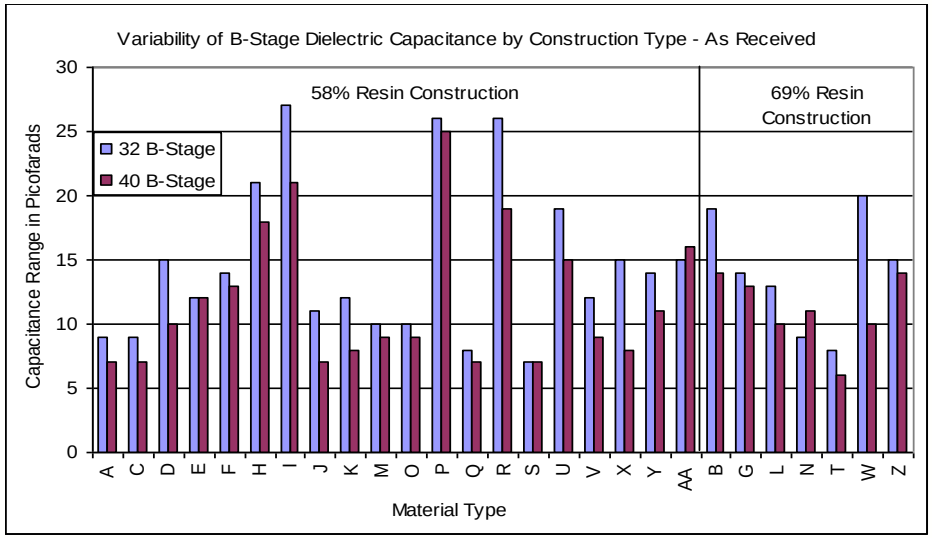
27 Products B-Stage Variability

Comparison of C-Stage

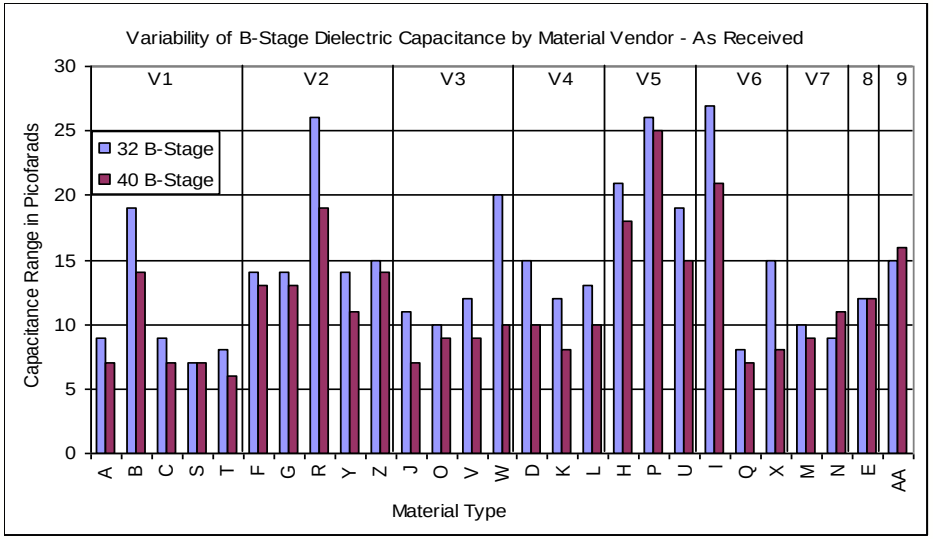


27 Products C-Stage Variability

Comparison by Stack-up or Material Vendor

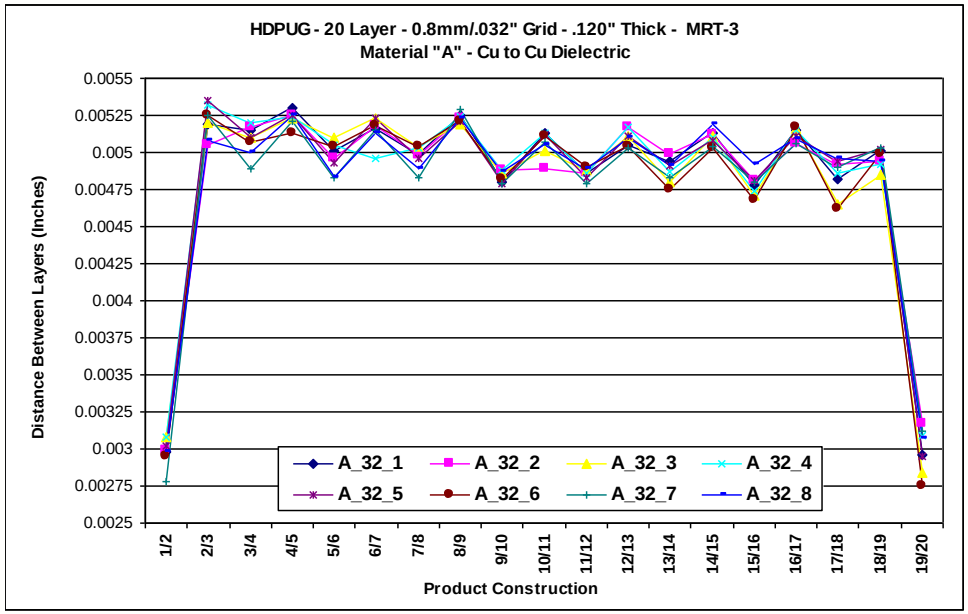


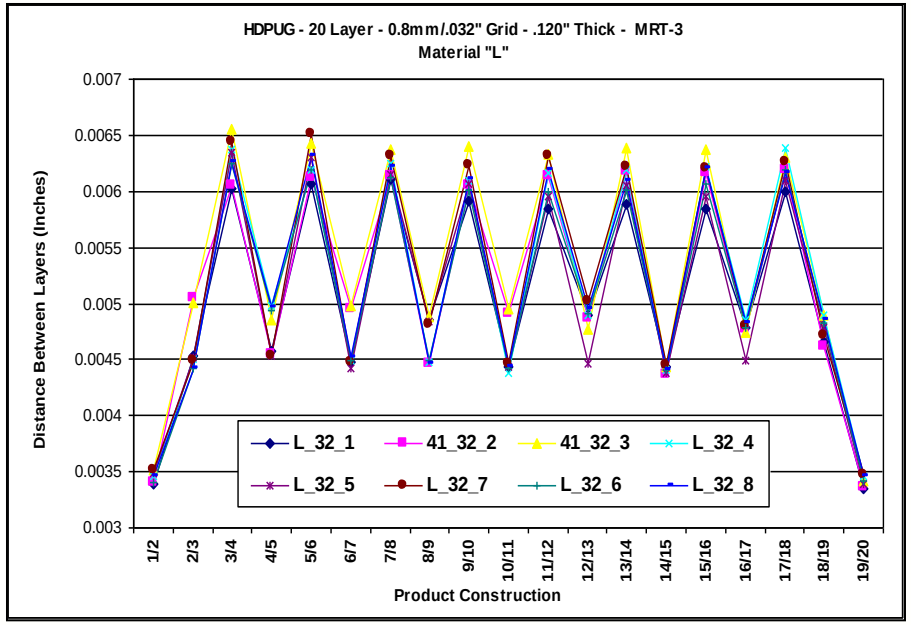
27 Products "A" Vs "B" Stack-up



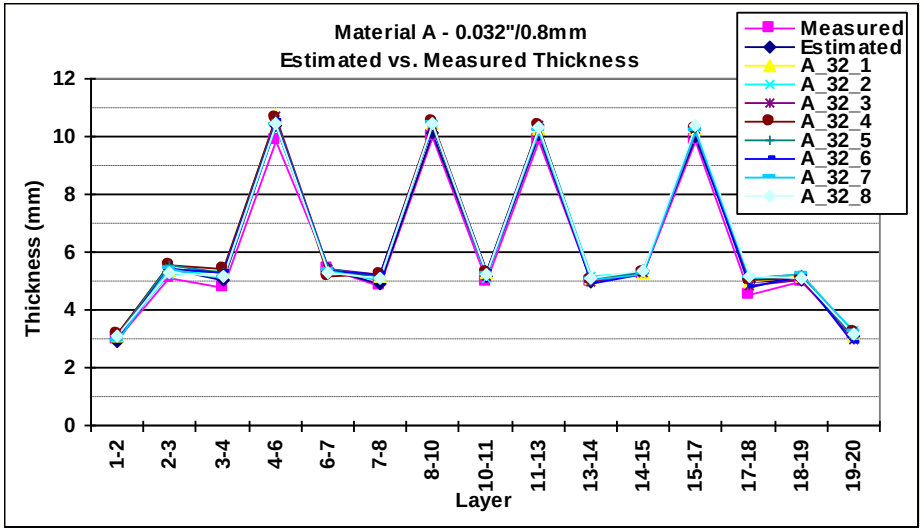
27 Products – 9 Material Vendors

Predicting/Measuring Material Thickness

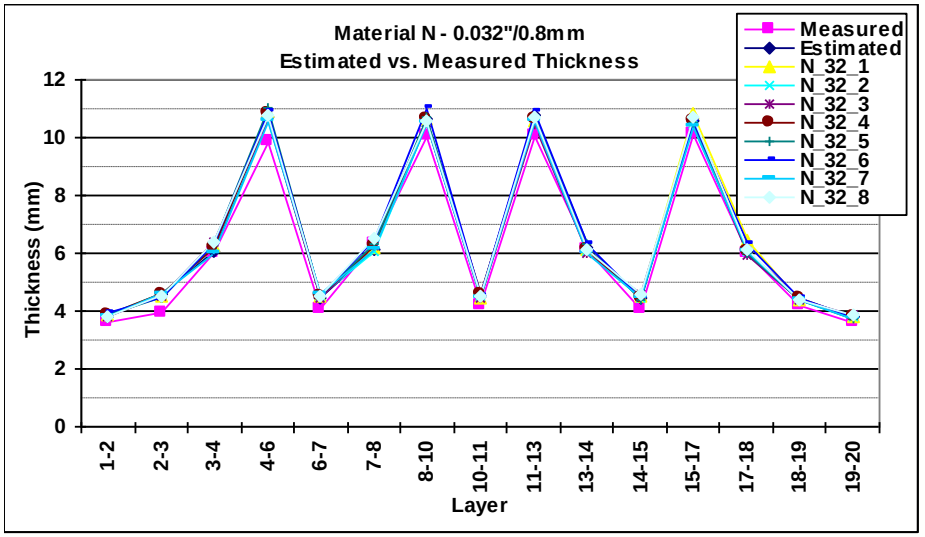




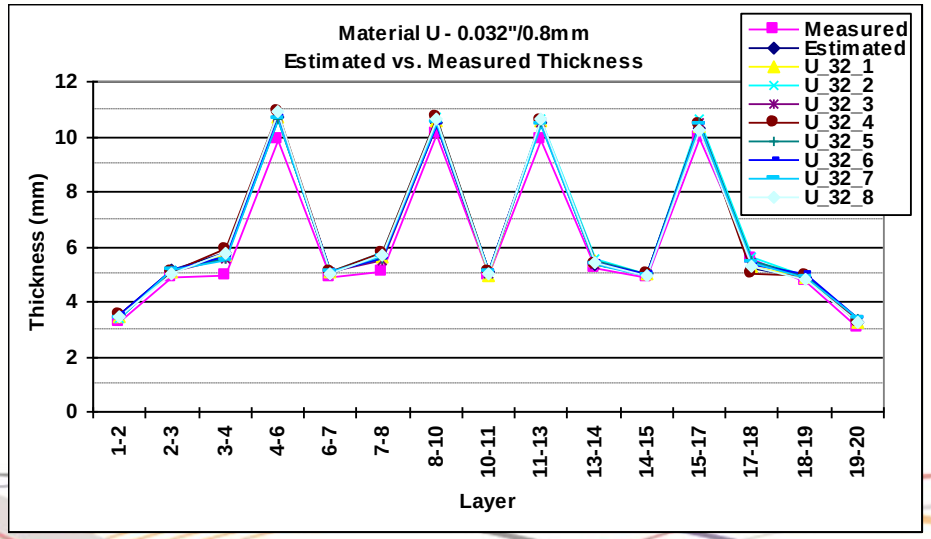
Measuring Dielectric Thickness with Capacitance



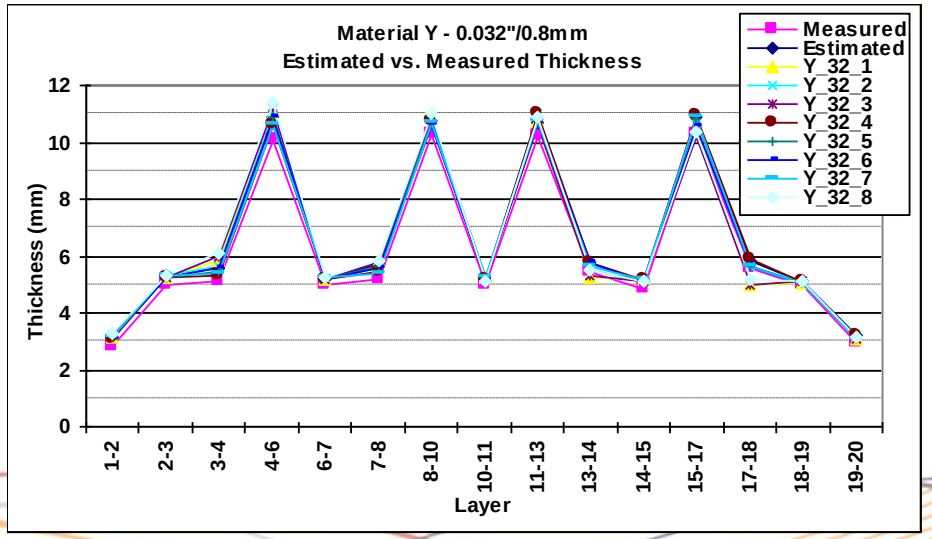
FR4 – Material "A" 58%



Halogen Free – Material "N" 69%

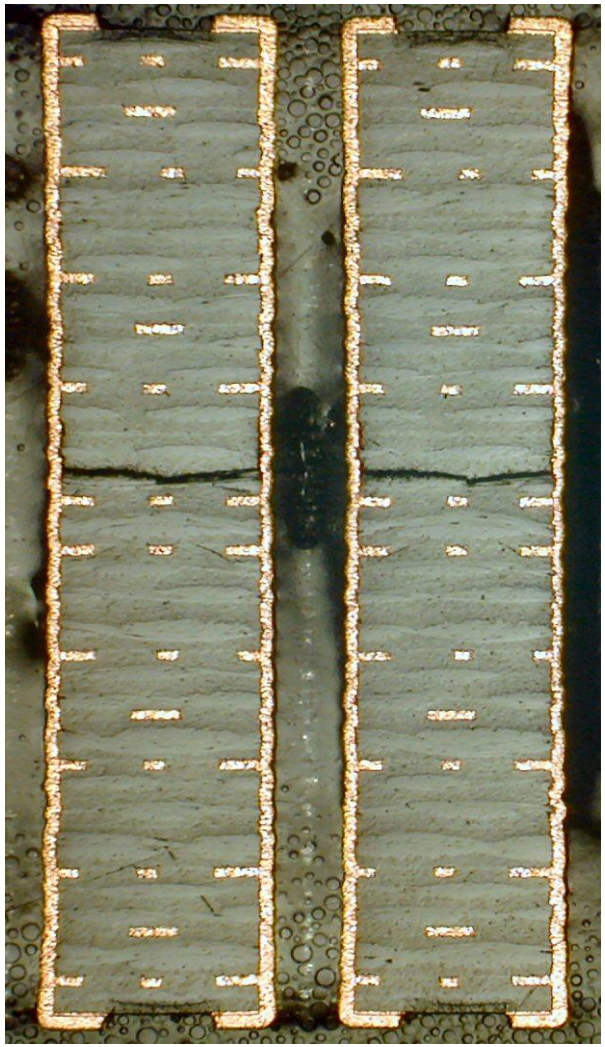


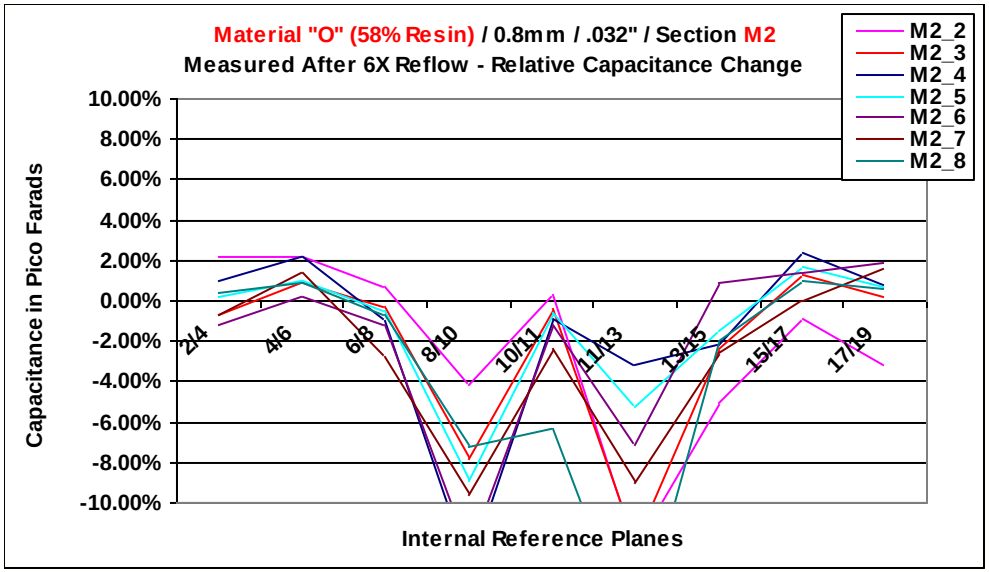
High Speed – Material "U" 58%

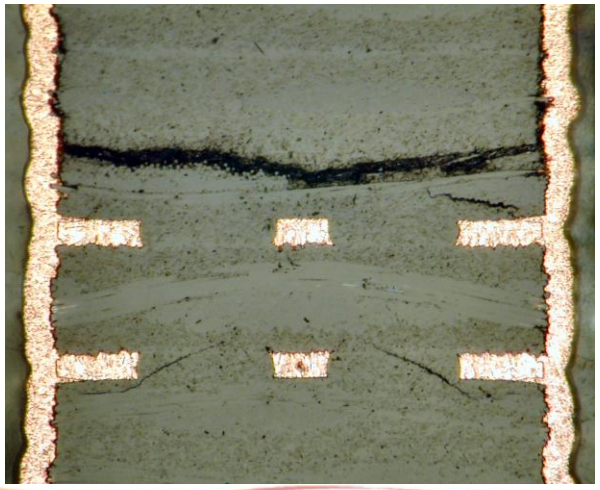


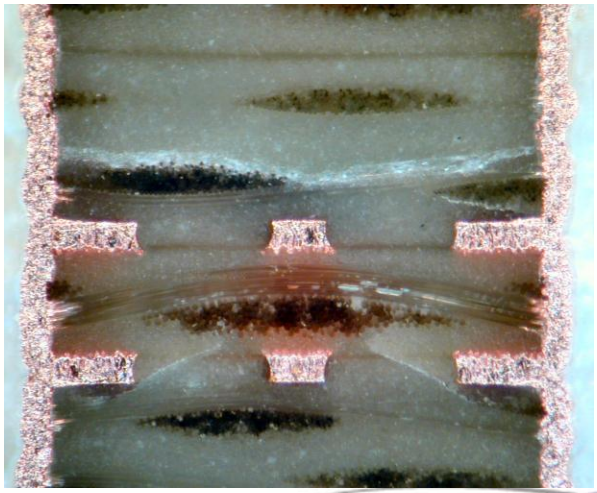
High Speed – Material "Y" 69%

IST DELAM – Finding Material Damage

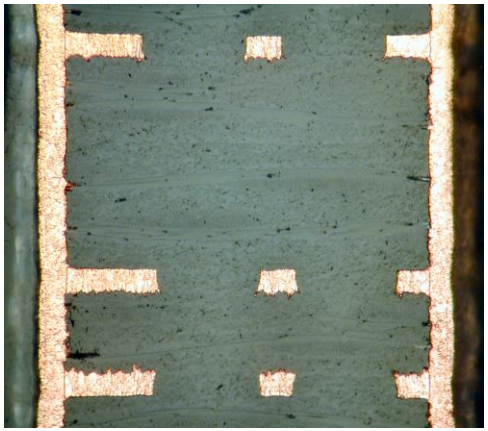


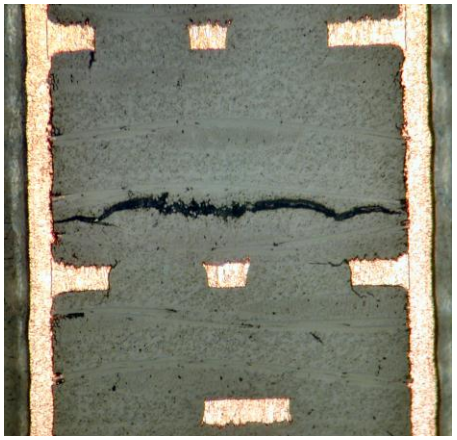




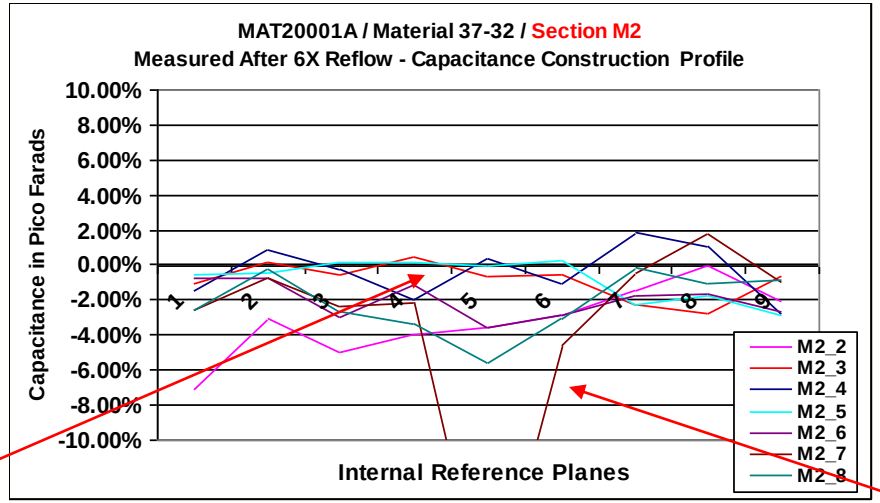


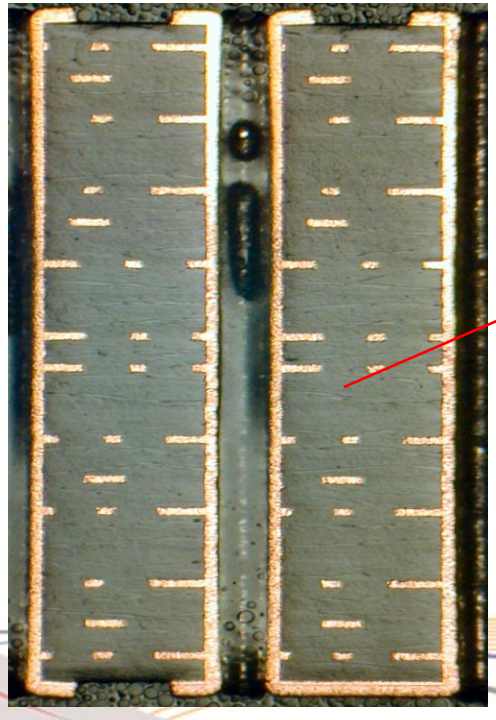
IST DELAM – Finding Material Damage

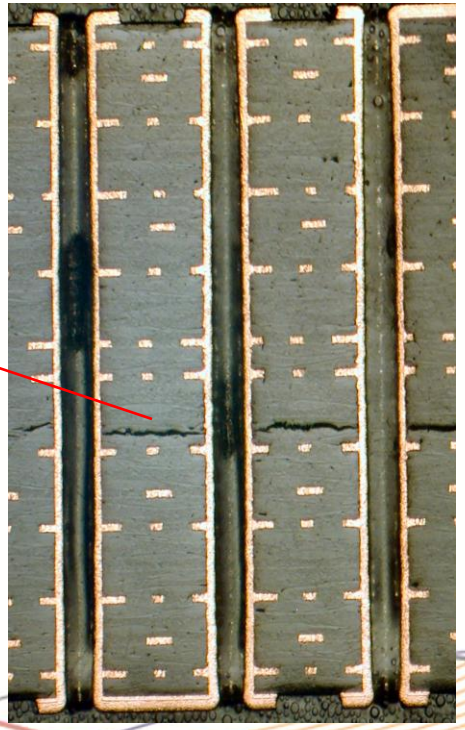




1 material / 2 Results







Solder Float/Microsection Delamination Results

				Cross-sections after Thermal stressing											
				Internal Material Damage after 6X 260C reflow						Internal Material Damage after 6X 288C thermal shock					
Coding	Stackup	Resin Content (%)	Visual Delam after 6X Reflow	1mm ATC	0.8mm ATC	1mm IST	0.8mm IST	CAF - 16 mil HW-HW	CAF - 20 mil HW-HW	1mm ATC	0.8mm ATC	1mm IST	0.8mm IST	CAF - 16 mil HW-HW	CAF - 20 mil HW-HW
	FR4:														
A	A	58	No	No	No	No	No	HWS	HWS	No	MAJ	No	No	No	No
B	B	69	No	No	No	No	No	HWS	HWS	No	MAJ	No	No	No	No
C	A	58	No	No	No	No	No	MAJ	No	No	No	No	No	No	No
D	A	58	No	No	No	No	No	HWS	EB	No	No	No	No	No	No
E	A	58	No	No	No	No	No	No	HWS	No	MAJ	No	No	No	No
F	A	58	No	No	No	No	MED	EB	No	No	MAJ	No	No	MAJ	MAJ
G	B	69	No	No	No	No	MAJ	No	No	No	MAJ	No	No	No	No
H	A	58	No	No	No	No	No	No	HWS	No	MAJ	No	No	No	No
I	A	58	No	No	MAJ	No	MED	No	HWS	No	MAJ	No	No	No	No
J	A	58	No	No	MAJ	No	MAJ	MED	No	MAJ	MAJ	MAJ	MAJ	No	No
	Halogen Free FR4:														
K	A	58	No	No	No	No	MED	HWS	HWS	No	MAJ	No	No	HWS	No
L	B	69	No	No	No	No	No	HWS	HWS	No	MAJ	No	No	HWS	No
M	A	58	No	MED	MAJ	MAJ	MAJ	MAJ	MAJ	MED	MAJ	MAJ	MAJ	MAJ	MAJ
N	B	69	No	MED	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ
O	A	58	No	No	MAJ	No	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ
P	A	58	No	No	No	No	No	No	No	No	No	No	No	No	No
Q	A	58	No	No	MAJ	No	MAJ	HWS	HWS	No	MAJ	No	MAJ	HWS	No
R	A	58	No	No	No	No	No	HWS	No	No	No	No	MAJ	No	No
	High Speed Materials:														
S	A	58	No	No	No	No	No	No	No	No	MAJ	No	MAJ	No	No
T	B	69	No	No	No	No	No	No	No	No	No	No	No	No	No
U	A	58	No	EB	MAJ	MAJ	MAJ	EB	EB	MAJ	MAJ	EB	MAJ	EB	EB
V	A	58	Yes	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ
W	B	69	Yes	MAJ	MAJ	MAJ	MAJ	MAJ	MAJ	No	MAJ	MAJ	MAJ	MAJ	MAJ
X	A	58	No	EB	MAJ	No	MED	EB	No	No	MAJ	No	No	HWS	No
Y	A	58	No	EB	EB	EB	MAJ	EB	No	EB	EB	EB	MAJ	EB	EB
Z	B	69	No	No	EB	EB	MAJ	No	No	No	EB	No	MAJ	EB	No
AA	A	58	No	No	No	No	No	No	No	No	No	No	No	MAJ	No

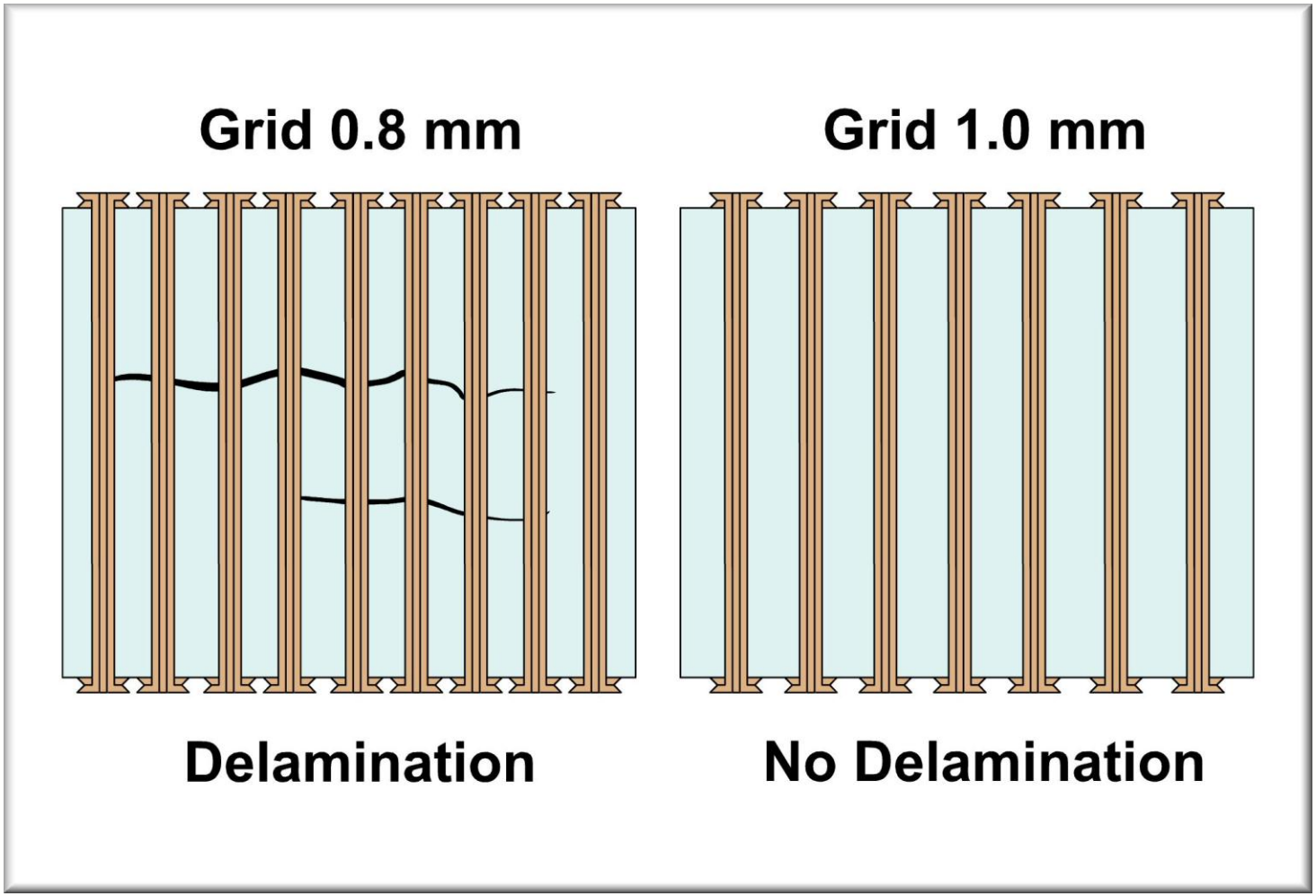
HWS	Hole Wall Separation > 20% is only defect found (note - <20% not listed)
Damage in Zone A only not listed	
MAJ	Major - Delamination, Cigar voids beyond zone A or Snake Delam
MED	Medium damage - May or may not be rejectable (example - medium cigar void)
EB	Eyebrow cracks beyond Zone A

Result of DELAM Analysis Testing After Reflow

Material #	0.8mm / .032" Grid		1mm / .040" Grid	
	Delam Y/N	Type	Delam Y/N	Type
FR4				
A	N	N/A	N	N/A
B	N	N/A	N	N/A
C	N	N/A	N	N/A
D	N	N/A	N	N/A
E	N	*Vertical	N	N/A
F	Y	Barrel to Barrel	N	*Vertical
G	Y	Barrel to Barrel (2 of 8)	N	N/A
H	N	N/A	N	N/A
I	N	N/A	N	N/A
J	Y	Barrel to Barrel (2 of 8)	N	N/A
Halogen Free FR4				
K	N	N/A	N	N/A
L	N	N/A	N	N/A
M	Y	Barrel to Barrel	N	N/A
N	Y	Barrel to Barrel	Y (2 of 8)	Barrel to Barrel
O	Y	Barrel to Barrel	Y (2 of 8)	Barrel to Barrel
P	N	N/A	N	N/A
Q	Y	Barrel to Barrel	N	N/A
R	N	N/A	N	N/A
High Speed Material				
S	Y	Micro Crack	N	N/A
T	N	N/A	N	N/A
U	Y	Barrel to Barrel	N	N/A
V	Y	Catastrophic	Y	Catastrophic
W	Y	Catastrophic	Y	Catastrophic
X	Y	Barrel to Barrel	N	N/A
Y	N	N/A	N	N/A
Z	N	N/A	N	N/A
AA	N	N/A	N	N/A

Note: Electrical Results Confirmed With Microsections

Lead Free Impact on Via Density



HDPUG Material Study Conclusions (1)

- The MRT-3 IST test coupon design proved to be a very effective test vehicle for non-destructively understanding multiple aspects of material performance through Pb free assembly, characterizing material variability and predicting dielectric thickness.
- Material damage through Pb free assembly confirmed the dominant level of damage/delamination was found (using electrical and microsection analysis) in coupons designed on a 0.8mm/.032” grid.
- Twelve of the 27 materials proved unsuitable for 6X 260° C Pb free assembly, specifically on the 0.8mm/.032” grid size.
- The result of conventional 6X solder float testing to 288° C can be strongly influenced by the test vehicle/coupon design.

HDPUG Material Study Conclusions (2)

- Although each material supplier was instructed to build the same glass/resin configuration each construction measured different (unique) profiles, each demonstrating different degrees of consistency between the C and B stage dielectrics.
- Changes within a coupons dielectric layer were easily identified; the non-destructive techniques demonstrated an effective capability to discern small changes within the dielectric thickness.
- Each B-stage dielectric (in the majority of cases) measured between 2x and 4x variability compared to the C stage dielectrics (for the same material). The data ranged from virtually identical results for all coupons (both grids), to a maximum of 15% difference between the 8 coupons from each grid size.
- Based on the small sample size and understanding that each material was being compared based on a single production lot, increased variability should be anticipated if either a larger sample size or multiple production lots were factored into the equation.

Closing Thought
Why Electrical Measurements?

- Microsection
- Customers Rarely Use or Compare Received X-Section Data
- Considered Low Return for ($, € or £) Their Investment
- Increasing Concerns of Relevance to Actual Product
- Electrical
- Creates Products Profiles Using Resistance and Capacitance
- Non-Destructive – Fast – Low Cost – Improved Statistical Validity – Establishes Process and Material Tolerances
- Logic
- Use Electrical Profiling on 100% of Products
- Confirm Profiles with Direction to Selecting Appropriate Coupon to X-Section