A Standard Multilayer Printed Wiring Board for Material Reliability Evaluations

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Abstract
This paper details the Alcatel-Lucent Pb-free Material Reliability Test board (MRT) used in two different High Density Packaging User Group tests covering 56 different constructions and in numerous other independent material analysis studies [1-7]. In total, this test vehicle has been used in over 80 different material evaluations (and still growing) encompassing materials from almost every major material manufacturer and fabricated by multiple PWB manufacturers. The test vehicle, currently in its 5th generation (MRT-5), is very comprehensive and includes sections for evaluation of material survivability through Pb-free reflow at different via hole pitches, air-to-air thermal cycling, interconnect stress testing (IST) – including the new DELAM methodology introduced by PWB Interconnect Solutions [5,9], conductive anodic filament (CAF) evaluation, moisture sensitivity and its effect on Pb-free reflow survivability, electrical characterization, provides BGA pads for pad pull testing, and incorporates specific design features to enable characterization of material properties (such as DMA) in a multilayer construction in a consistent manner. The design is flexible including 3 different standard constructions and resin contents (12 layer, and 20 layer with 2 different constructions) and can be adapted to other configurations if necessary. This paper presents the design and provides example results and information on how to evaluate these results. The design is made available to all in the industry to facilitate a standard test methodology – and has been offered to IPC as a standard test vehicle for multilayer material evaluations.

Introduction
With the advent of Pb-free printed circuit board assembly soldering, specifying laminates for bare printed wiring boards has become considerably more challenging compared to specifying laminates for SnPb assembly. Specifying the glass transition temperature alone, as historically done for SnPb assembly, is not nearly enough. The higher temperatures associated with Pb-free soldering have introduced a number of new reliability failure mechanisms and assembly survivability concerns [1-3,5,6-16]. Additionally, they have a negative impact on the plated through hole reliability [1,17,18]. Expanding the list of basic material properties of the laminates is a starting point for determining Pb-free compatibility and reliability [19-23], but has proved insufficient in itself in determining the viability of materials in the required applications [1,2,20]. Testing of the materials in representative multilayer constructions is the only way to ensure material compatibility with Pb-free assembly and long term reliability.

The design presented is a generic material qualification test board which is designed to enable the testing, characterization, and reliability evaluation of bare board materials in actual multilayer constructions. Multilayer board constructions provide a much more realistic assessment of the material properties and performance in real products, compared to testing of bare laminates. Using proven standard constructions also allows for direct comparisons of material performance. Additionally, a standard set of tests on these constructions can provide a good set of data reflecting how the materials will perform in real products.

The design supports and enables two standard 20 layer constructions and one 12 layer construction with a single artwork and can be modified to other constructions if necessary. Specific sections of the circuit board design enable testing to evaluate:

- Assembly Reflow survival – specifically visual inspection and internal layer cross-sectioning at different pitches, typically after 6X reflow at 260°C +5/-0°C peak temperature (temperature can be modified to reflect actual requirements if necessary). Note – the intent of this section is to not bake the test boards before completing the Pb-free assembly cycles. It is understood that baking is commonly recommended by most material suppliers before material testing, but this is not indicative of typical product use. Moisture effects are addressed separately.
- Thermal Analysis – both before and after assembly reflow (Typically 6X Pb-free), including DMA, TMA, DSC analysis.
- Air-Air thermal cycling of different hole sizes and pitches – including 0.25mm, and 0.66 mm hole sizes and for the 0.25mm hole sizes, patterns are provided for comparing 0.8mm pitch, 1mm pitch, and 2.5mm centers. Air-Air thermal cycling can be directly related to field life.
- IST testing – including both before and after assembly reflow (typical 6X Pb-free) and/or preconditioned using simulated IST Pb-free preconditioning. The IST coupons on this design are specially designed material testing coupons, one with 1mm pitch vias and the other with 0.8mm pitch vias.
- DELAM Testing – Capacitance measurements recorded both as received and after exposure to assembly reflow cycles. Changes in capacitance indicate the presence of material damage, which are subsequently confirmed or

denied by microsection analysis. Additional features include the confirmation of product construction and determination of consistency between the B and C stage materials.

- Electrical testing – S-parameter data for both microstrip and stripline configurations. Permittivity (Dielectric Constant – Dk) and Loss Tangent (Dissipation Factor – Df) can be extracted and plotted using this design.
- CAF Testing – Limited CAF testing – specifically designed to evaluate only the hole-wall to hole- wall CAF performance for through-hole vias and the effect of reflow on the CAF performance.
- Two WIC-20 coupons (based on IBM's WIC-20 design) allow for quick assessment of material survivability and material integrity after Pb-free reflow by the use of TDR and capacitance measurements. They also allow the investigation of the influence of moisture content on this performance.
- SMT pads on the backside of the electrical test section to support pad pull testing per IPC-9708, Test Methods for Characterization of PCB Pad Cratering (in draft at this writing).

Ideally, a material should be tested in all three constructions. More typical is to test either the 12 layer construction or both 20 layer constructions. Experience has shown that many materials that will not survive in the 20 layer constructions will be fine in the 12 layer construction. Similarly, different results on each of the 20 layer constructions are not uncommon. Normally, the high resin content 20 layer construction is the most challenging, but some lower flow materials may find more challenges in the standard resin content construction. The actual configuration(s) tested are generally decided based on the raw material properties and experience with similar performing laminates.

Board Stackup Options

There are 3 different stackup options. The first is a 12 layer, 50% resin content construction that is 2.36 mm (.093 inch) thick (Figure 1). There are also two 20 layer constructions, one at 58% resin content, 2.95 mm (.116 inches) thick, that represents a typical 20 layer construction in that thickness (Figure 2), the other is 69% resin content, 3.0 mm (.118 inches) thick, that is representative of a higher layer construction (typically 26-28 layers) in the same thickness (Figure 3). The microvias in the stackups are specifically used to eliminate concerns with the electrical stub associated with a through via in the S-parameter testing. These stackups provide a representative sample of possible production applications. If needed, the stackups can be modified to address specific unique needs. However, one of the benefits of using the standard stackup constructions is that they allow for clear comparisons of material performance.

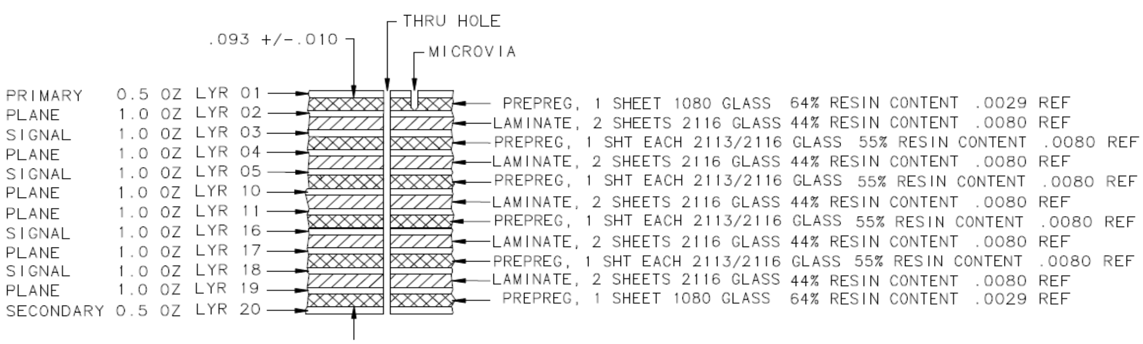


Figure 1: 12 layer, 50% resin construction

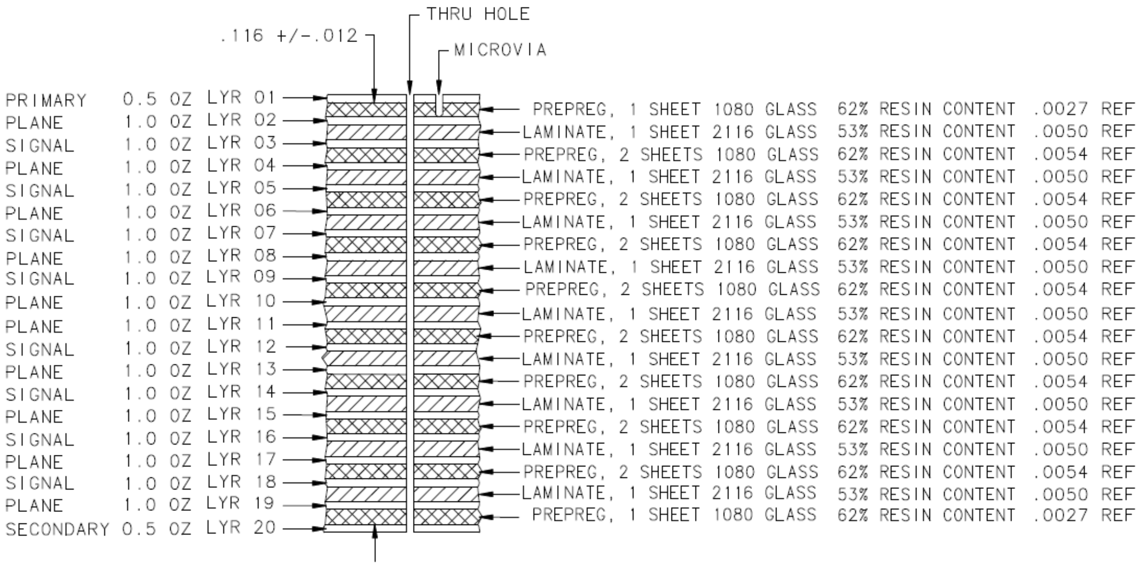


Figure 2: 20 layer, 58% resin construction

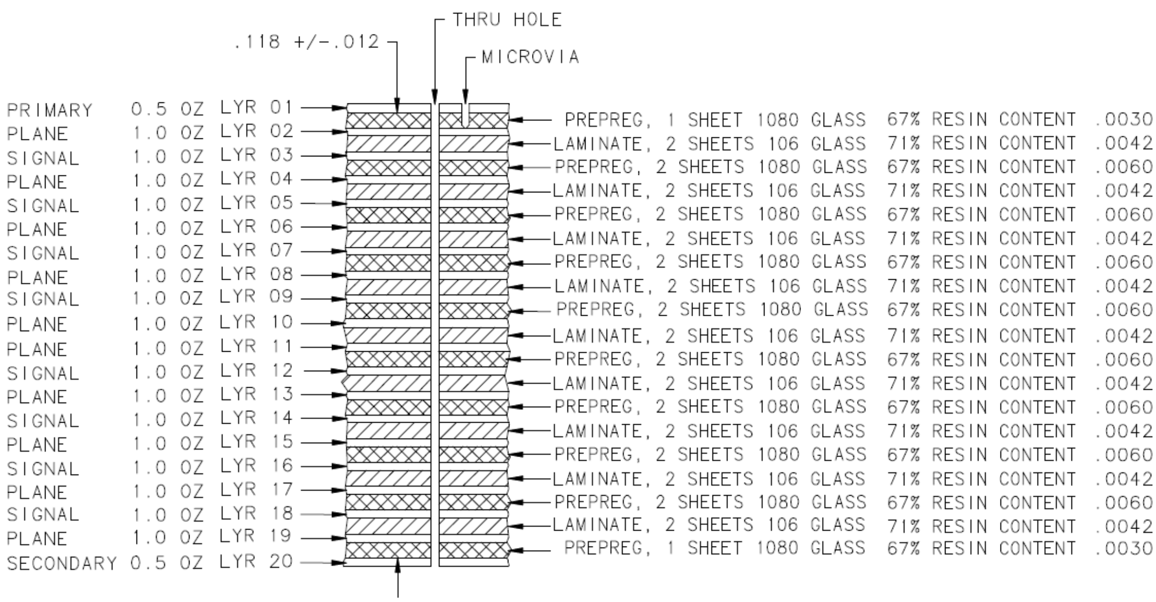


Figure 3: Figure 3, 20 layer, 69% resin construction

Broad Overview of the Design

The following is an overview of the different sections of the test board, showing the areas designated for the different testing. Figure 4 shows the plan view from the drawing with each of the seven different sections identified. Each of these seven sections has a location specifically identified for marking identification of the material and stackup used on the bottom layer (see boxes flagged to note 3 in Figure 4). Figure 5 is a view of the artwork from layer 1 showing these same areas. Figure 6 shows an actual board from the Layer 1.

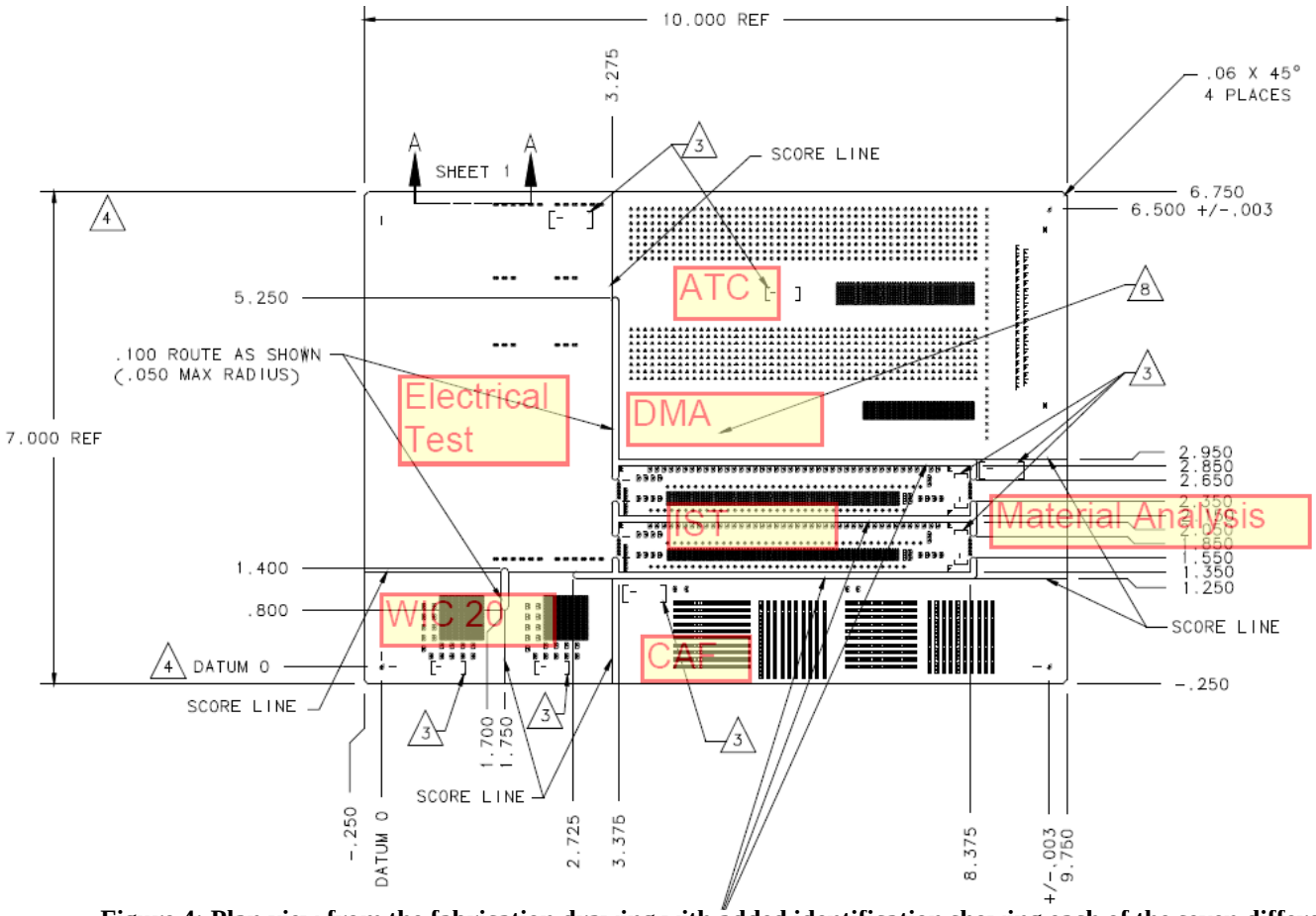


Figure 4: Plan view from the fabrication drawing with added identification showing each of the seven different sections on the test board.

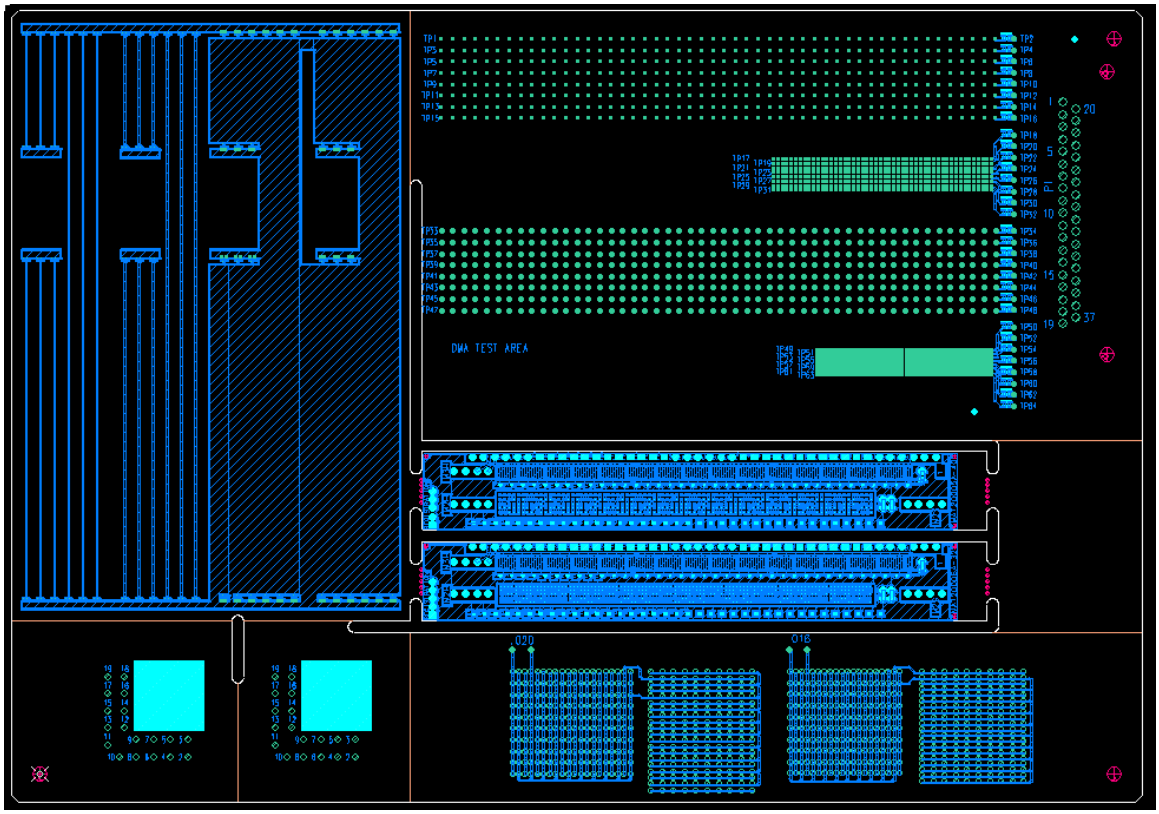


Figure 5: Artwork overview of the test board as viewed from layer 1.

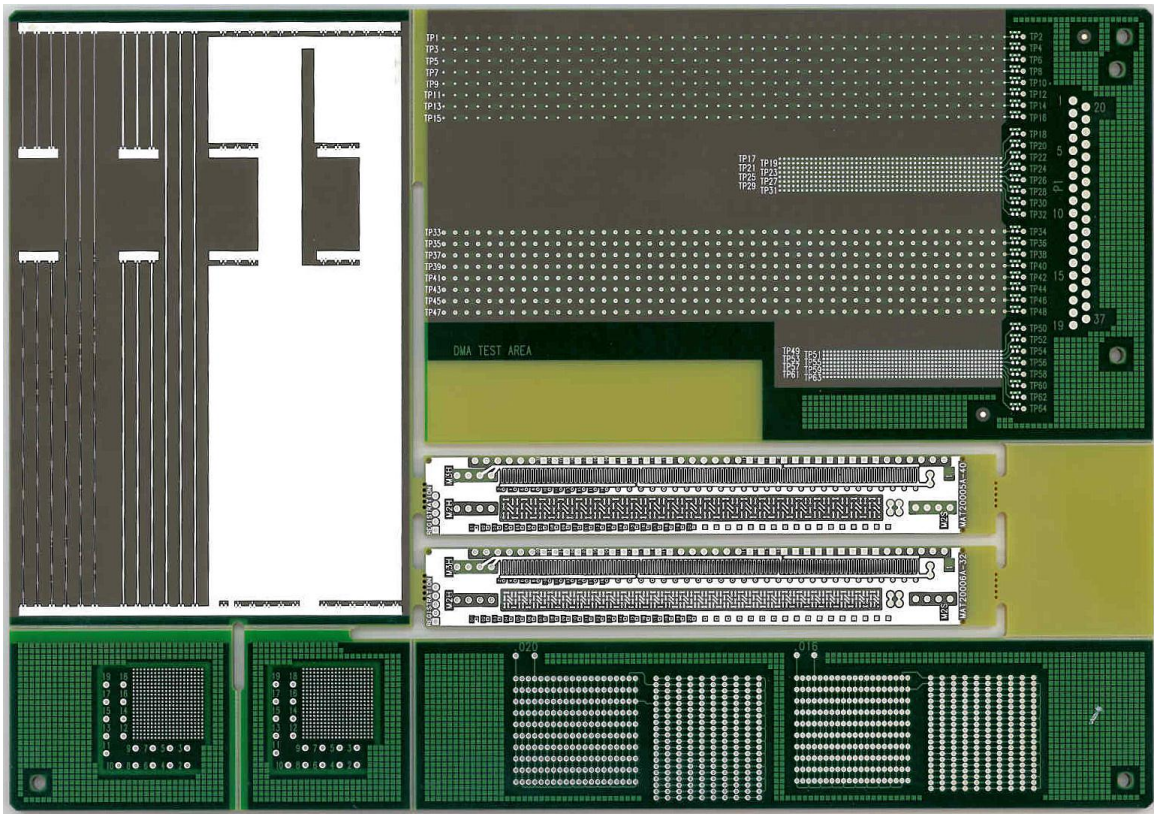
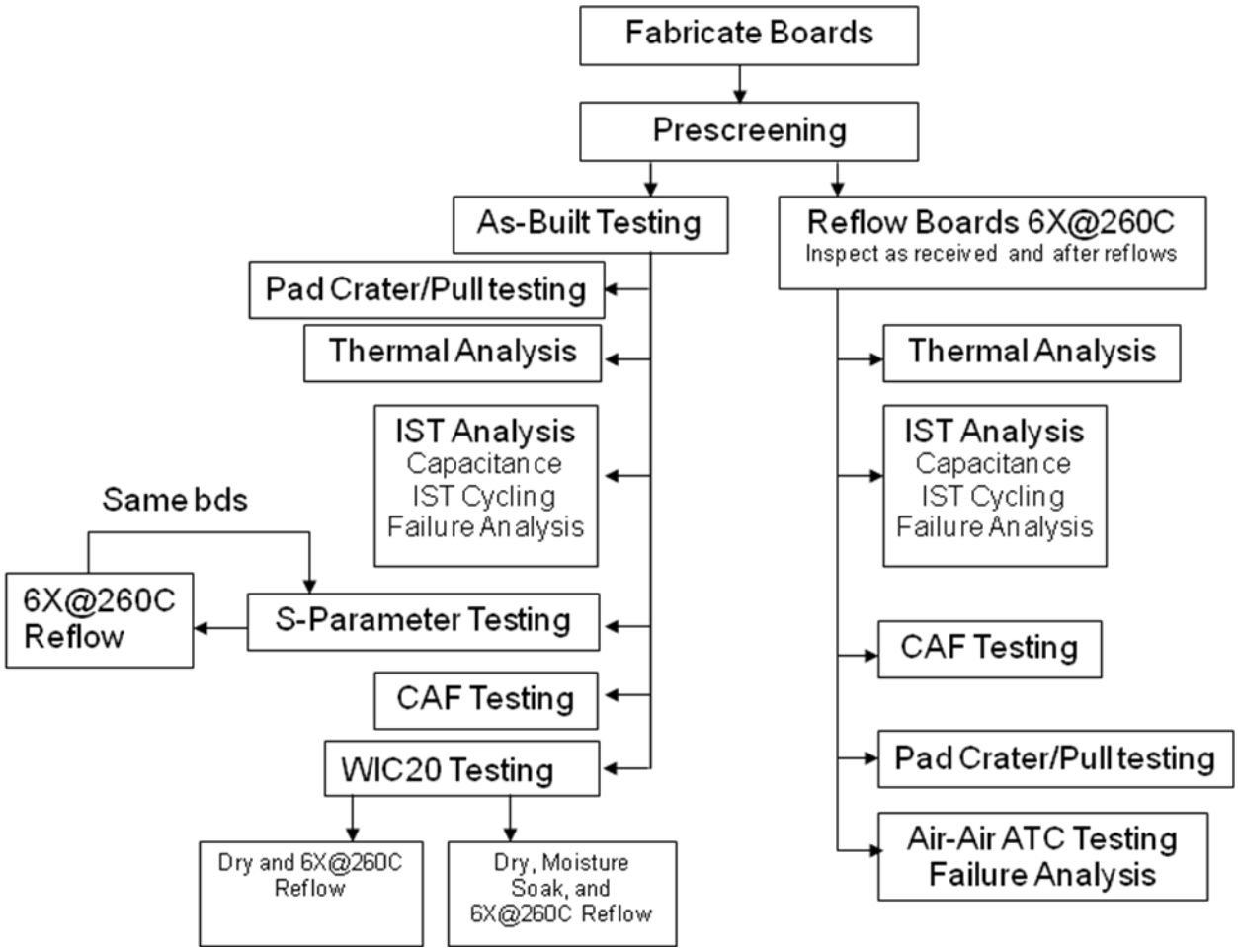


Figure 6: Photograph of an actual MRT-5

Overview of Testing

First fabricate 20 boards. As the board size allows for 4 up on a standard 457 x 610 mm (18" x 24") fabricator panel, there are only 5 panels required. Fabricators may require additional materials to ensure full books or press loads and to account for any yield loss. Additionally, it is strongly recommended that first article boards be cross-sectioned after 6X@288ºC thermal stress (do not bake first) and after 6X assembly reflow at 260°C+0/-5°C in the areas of 1mm and 0.8mm pitch before investing in the other tests. This requires one to two extra boards. These are then separated into two groups of ten. The first group of ten boards is for testing and analysis as fabricated. The second group of ten boards is for testing after reflow. The flowchart below gives an overview.



Of the as built boards, one entire board is dedicated to thermal analysis. The remaining nine are separated into their various sections and the following sections/coupons are required for each test:

Air to Air Thermal Cycling: 0
CAF (as built): 8
S-Parameter Electrical Testing: 1 (minimum, 2 recommended) (Remaining can be used for Optional pad pull testing)
IST at 0.8mm pitch: 6
IST at 1.0mm pitch: 6
IST coupons for Capacitance Robustness testing: 3 each at 0.8mm pitch and 1mm pitch
WIC20 Coupons available for the Moisture Sensitivity Testing: 18

Of the ten boards for reflow (6X@260°C), one entire board is required for thermal profiling of the oven and one entire board is required to be sent for thermal analysis after reflow. The remaining eight boards shall be taken through the assembly reflow profile (6X@260°C) and inspected for visual damage. These boards are then to be separated into their various sections and the following sections/coupons are required for each test:

Air to Air Thermal Cycling: 4
CAF (after 6X): 8
S-Parameter Electrical Testing: 1-2
Remaining S-parameter test section can be used for pad pull testing.
IST at 0.8mm pitch: 6
IST at 1.0mm pitch: 6
IST coupons for Capacitance Robustness testing: 12 – the same 12 used for the IST thermal cycling can be compared to the as built coupons
WIC20 Coupons Testing - not required on these boards – but can be done if desired.

Deliverables

1) Results of pre-screening (cross-section photographs)
2) Thermal Analysis – include summary of results plus the specific TMA, DSC, DMA etc. graphs. Both as built and after 6X reflow.
3) IST results – both capacitance and cycling details. Include the actual data and failure analysis cross-sections.
4) S-Parameter results including graph of Dk/Df over frequency both as built and after 6X reflow on the same graphs for comparison.
5) CAF test results (both before and after 6X reflow) including the raw data in Excel format. Results of any failure analysis if applicable.
6) ATC results and failure analysis. Include the failure by cycle data in Excel format.
7) WIC-20 capacitance and resistance data after each condition, in Excel format and graphs as applicable. Include failure analysis cross-sections if applicable. Impedance testing is optional
8) Hot Pin pull testing data (if performed).

Pre-screening

Before committing materials to the required testing, cross-sections should be taken after 6 cycles of 10 second solder floats at 288°C thermal stress testing (as a minimum) and ideally also after 6X reflow at 260°C. The cross-sections shall be taken in the ATC section at both 1mm and 0.8mm pitch, both of the IST coupons (1mm and 0.8mm pitch), the CAF test sections (across the smallest dimension for each section), and in the WIC-20 coupons. These should be evaluated for material damage/degradation and for copper thickness and hole wall quality. Based on these results, it is up to the material supplier and/or fabricator and/or requesting OEM to make a decision to go forward with the remaining testing.

Example defects that might be found after prescreening include but are not necessarily limited to, edge delamination, blistering, hole wall pull-away, resin recession, visible delamination, hidden delamination, and eyebrow cracking. Some of these are not necessarily considered defects per IPC criteria, but are indicative of material degradation during reflow. The hidden delamination, which is between arrays of vias, will escape visual detection and must be evaluated during material qualification efforts, as it is not seen in production product without cross-sections, and random cross-sections of production samples can easily miss this type of defect. Examples of some of these defect types are shown in Figure 7.

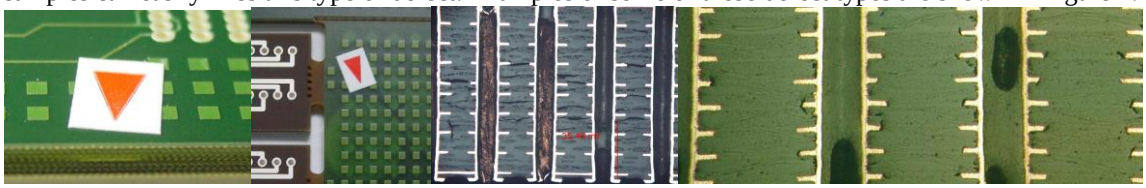


Figure 7: Left-to-right: Edge delamination, Visibile internal delamination, Hidden delamination between vias, Eyebrow cracking

Electrical Test Section

This section is designed for S-Parameter testing and Dk, Df extraction based on Intel's methodology as defined in reference [24]. Note, other methods of extracting the Dk and Df from this S-parameter data may be equally valid. Standard requirements are to test from below 1 GHz to 9 GHz or higher for FR4 materials. Suppliers may wish to extend this for materials that target high frequency/high speed applications. From this S-Parameter data, the Dk and Df of the materials can be extracted. It should be extracted (and plotted vs. frequency) at 1GHz intervals.

Recommended Test Equipment and setup:

- Agilent 8385A 2 Port VNA Network Analyzer or equivalent
- Probes: GGB picoprobes GS/SG of 225µm pitch
- IF Bandwidth: 100Hz
- Log sweep set from 300KHz to 9 GHz
- No of points: 1601
- Calibration: GGB CS-8 calibration substrate with SOLT

Methodology:

- Two line method is used for determining the propagation constant
- Dielectric constant is calculated from the phase constant
- Loss tangent is calculated by curve fitting the attenuation constant

The following assumptions in the analysis are typical:

- No variation in trace width and thickness due to the processing

- No surface roughness (note that it is possible to estimate the trace roughness from this data by comparing the wider and narrower traces)
- Dielectric thickness is assumed from the stackup (or from microsections if available in the area tested).

Figure 8 is a picture of the Electrical Test Section of this board.

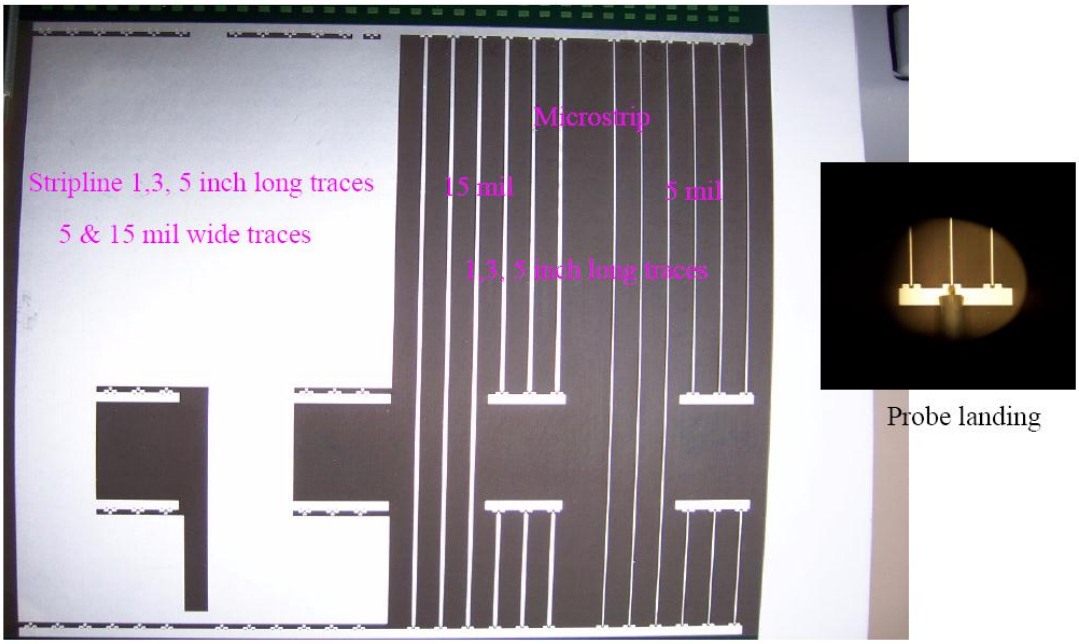


Figure 8: Electrical Test Section of the Test Board

Sample Size for Electrical Test

A minimum of one board should be tested as built and the same one tested after 6X Pb-free reflow. A sample size of at least two is recommended. Since the intent of this is not only to characterize the electrical performance of the material, but also to determine what changes in the electrical characteristics after reflow (if any), larger sample sizes are recommended such that the results can be averaged or the same board be tested both before and after reflow.

Evaluating the Electrical Test Data

The electrical test data characterizes the material performance (Dk, Df) over frequency. Also it enables an understanding of the impact of 6X Pb-free reflow on these electrical parameters. For good materials, the effect of reflow is minimal. However, a significant change in the electrical properties of the materials may be seen, in either Dk or Df. This is indicative of something changing in the material during reflow. Figure 9 shows examples (two different materials) where the electrical characteristics of the material changed dramatically after 6X Pb-free reflow.

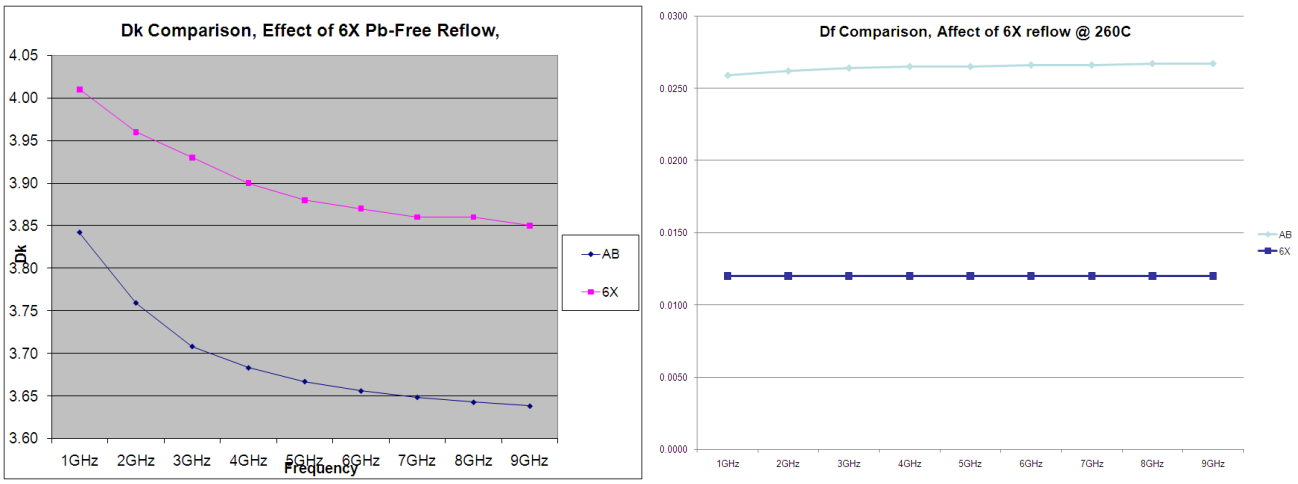


Figure 9: Typical plot of Dk over frequency (left) and Df over frequency (right). These two plots are shown where the changes in the materials after reflow are major.

Air-Air Thermal Cycle Test Section

This section is designed specifically for air to air thermal cycling to evaluate PTH long term reliability using a method that can be directly related to field conditions. See Figure 10. A number of thermal cycle conditions are acceptable for testing, but to minimize test time and cost, a thermal cycle of -40ºC to +135ºC is preferred when testing high Tg materials (Tg >160ºC). For a material with a lower Tg, in the range of 140ºC to 160ºC, the high temperature should be reduced to 125ºC. The thermal profile should have a dwell of at least 10 minutes at the temperature extremes and ramp rates between temperature extremes that don't exceed 20ºC/minute. All air-air thermal cycling should be done after 6X assembly reflow preconditioning. This not only represents actual use conditions, but typically shortens the test time and cost.

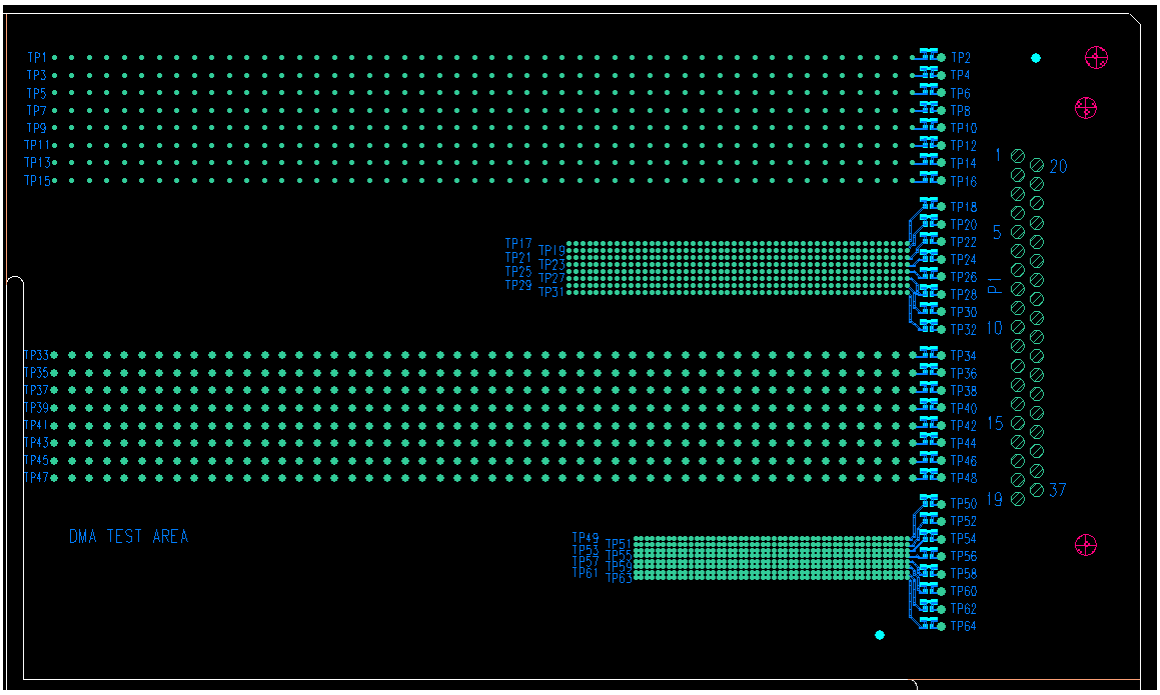


Figure 10: Air-Air thermal cycling test section

The design of this section consists of four groups of eight chains of 50 vias. The first and third groups are on 2.5mm centers, the second group is on 1mm centers and the fourth group is on 0.8mm centers. The first, second and 4th groups are 0.25 mm drill size, representing what is typically the smallest hole size used in production for the products under consideration. The third group is a 0.66 mm (.026 inch) drill size that represents a typical (smaller) compliant pin hole size. This enables direct comparison of the performance of widely spaced vias vs. vias at the smallest spacing used on actual boards. The tighter spaced holes are typically much more prone to thermal issues (delamination, eyebrow cracking, etc.) than the wider spaced holes. The daisy chain net connections are on layers 2 and 19 (2 and 11 on the 12 layer version) so that both barrel cracking or foil cracking (if it occurs) will be caught. It is understood that the thermal cycling test vehicle will not detect corner cracking as a failure mode.

The via chains are wired to the connector pattern. The ground/returns on each chain return to pins 33-37 on the connector pattern. Connections for the ground returns are on all internal plane layers to ensure that failures identified are from the via chains, and not the ground/connector connection. The individual net chain connections to the connector are located on layers 10 and 11 to minimize the possibility of failures at these locations. Similarly, the hole sizes in the connector pattern are considerably larger (1.33 mm finished) so that they will typically fail after the via chains.

During thermal cycling, nets should be monitored continuously in-situ using event detectors or data loggers. Thermal cycling should be continued until at least 63% of the chains of the 0.25 mm hole sizes fail at each of the different pitches or (assuming the standard thermal cycle conditions) 3000 thermal cycles are reached. Ideally, a similar failure rate of the larger vias is good, but this may take considerably longer and increase the test cost significantly. Note that if the larger 0.66 mm holes fail rapidly, this is usually indicative of a foil crack failure mode or interconnect separation on layers 2 and 19. This should show up in failure analysis and also will typically result statistically in a better fit to a Weibull distribution rather than

the Log Normal distribution typical of a barrel crack failure mode. If a different thermal cycle condition is used, the maximum number of thermal cycles should be adjusted to compensate. The intent of this testing is to generate failures and a failure distribution. A test to "X" number of cycles with no failures is of limited value. The failures should be plotted both Weibull and log normal and analyzed accordingly. Failure analysis crossections should be completed at a minimum on the 0.25 mm hole sizes on 2.5mm centers, 1mm centers, and on the 0.8mm centers. If there are no failures in 3000 cycles, cross sections should still be taken at the 1mm and 0.8mm pitch locations after completion of the testing. Note that internal delamination or material degradation can artificially increase the number of cycles to failure. If the Weibull/Log Normal analysis indicates multiple failure modes, or potential different failure modes on an individual hole size, or between hole sizes, additional failure analysis may be necessary.

Sample size for the Air-Air Thermal cycle Testing

Thirty-two nets of each hole size shall be monitored (thus 63% failures is 20 fails and generates good statistics). This requires four of these test sections and a total of 128 nets to be monitored (the typical capacity of a small event detector) per each stackup evaluated, assuming all nets are monitored.

Note that the design incorporates locations for the optional attachment of 0402 resistors in the air-air daisy chains. This is only a potential option when data loggers are used (not event detectors) and enables the paralleling of daisy chains (up to eight per net) where failures are identifiable as a step increase in the resistance of the parallel chains as one (or more) of the nets fails. In the event this is used, the net short jumpers need to be cut to put the resistors in the circuits. If this option is utilized, it greatly complicates the data collection and analysis.

Boards with evidence of delamination, either from the visual inspection or from the IST capacitance measurement may perform "falsely" better in air-air testing (or IST testing) as the stresses on the plated through holes are relieved by the delamination. However, the IST coupons, which have tighter hole pitches (one at 1mm centers and one at 0.8mm centers) than the 2.5 mm center section of the air-air thermal cycle test section may delaminate quicker than the 2.5 mm center air-air section and it may still be worthwhile to proceed with air-air testing even if the capacitance testing on the IST coupons shows possible internal delamination (not visually obvious). This judgment is left up to the material supplier/fabricator conducting the testing.

Evaluating the ATC data

The air to air thermal cycle data provides information about both the plated through hole lifetime and about the material performance itself. The plated through hole lifetime is a function of both the material properties and the quality of the plating. The primary purpose of this test vehicle is to evaluate the material performance, but the data can also be used to evaluate the long term plated through hole reliability. First thing to evaluate is the 0.66mm hole size. If these fail before or nearly equivalent to the smaller 0.25 mm hole sizes, this indicates that there is either a foil crack failure mode or some type of interconnect separation occurring. A foil crack is a material failure related to very poor layer copper quality or ductility and/or very high Z-axis CTE of the material driving this failure mode. Normally, both are fatal issues when evaluating materials. If a foil crack occurs, the failure distribution will typically be Weibull, rather than log normal. For a plated through hole barrel crack wear-out failure mechanism (the normal and desired failure mode), the distribution is typically log normal, not Weibull. If the cause of this failure is interconnect separation, this is a plating problem and all the other data is suspect. See Figure 11 for an example of a foil crack failure that was identified with this test vehicle. Note, if foil cracking is found on the larger holes, it is also occurring on the smaller hole sizes, but is much more difficult to find in subsequent failure analysis, since the predominant failure mode will typically be barrel cracking fatigue on the smaller holes.

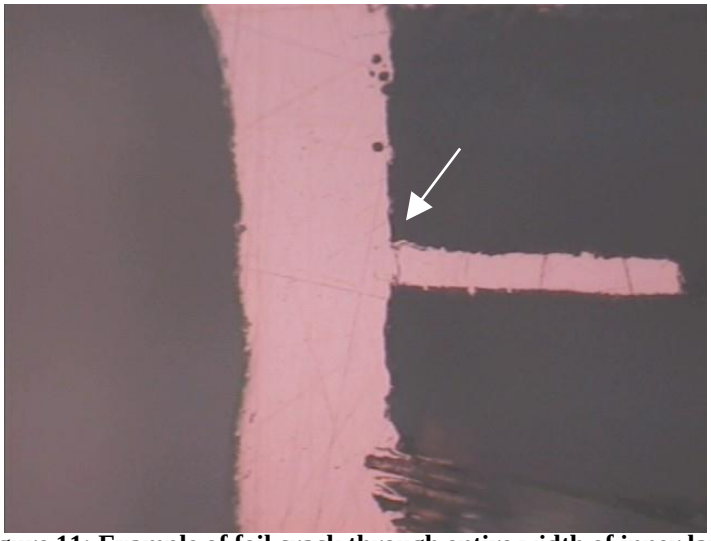


Figure 11: Example of foil crack through entire width of inner layer

The air to air thermal cycling can also indicate if material damage occurs. For example, normally the 2.5mm, 1mm and 0.8mm pitch vias will have similar failure distributions, with only a small impact from the different pitches on the cycles to failure. Similarly the slopes of the failure distributions, when plotted on a Weibull or log normal plot will be the same. However, if material degradation occurs, and this typically happens more as the pitch of the vias becomes smaller, this will show up in either one or both of two results. The first result is a marked difference in the failure rates of the different pitches. This is typically because the material degradation (possibly delamination) will relieve the stresses on the plated through holes and result in a false improvement in the results. The second result is the slope of the plot (beta on a Weibull plot, SigF on a Log Normal plot) will be markedly different, indicating another failure mode. Failure analysis is typically required to identify the root cause, but material degradation is the common cause. Figure 12 shows an example on a previous generation of this test vehicle (MRT-2) where there is a marked change in this slope for the 0.8mm pitch vias on the 69% resin construction compared to all the other via failures in this same test. Subsequent failure analysis identified some rather difficult to find degradation in the material, that would have escaped typical cross section analysis had the data not indicated something was wrong. This failure data necessitated greater scrutiny in the failure analysis on that specific construction and via pitch.

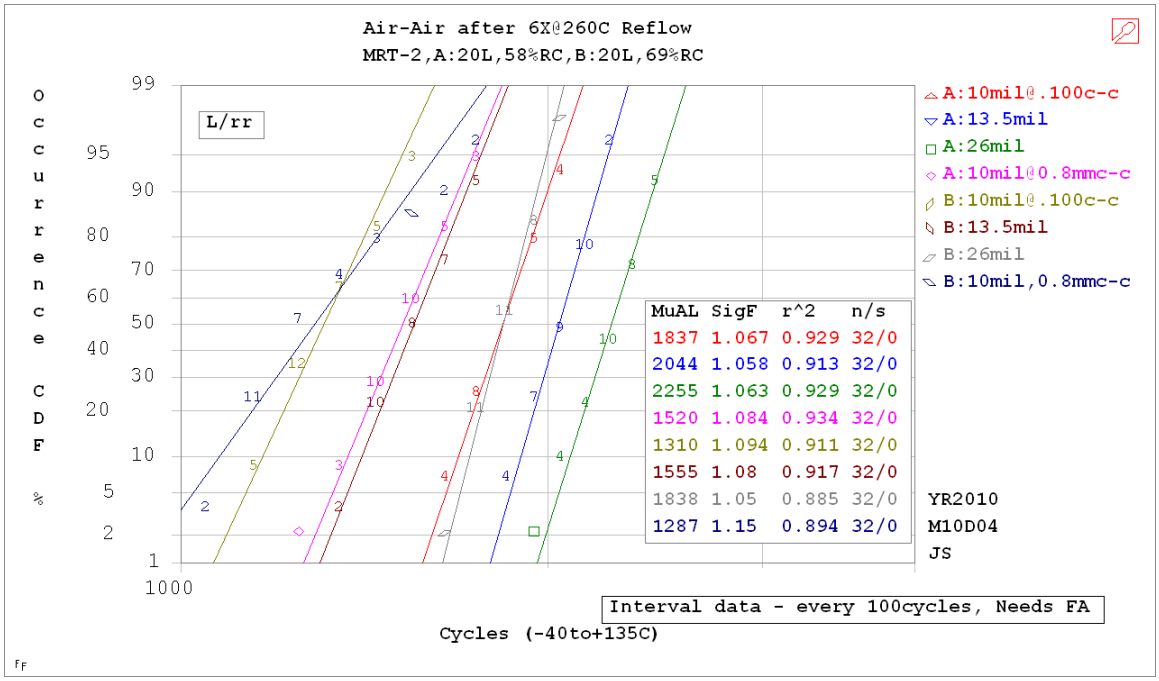


Figure 12: Log Normal plots of air-to-air failure data showing a slope change on the 0.8mm pitch construction with 69% resin content

IST Coupons (two per test board)
The test procedure is as follows:

Test per IPC-TM-650 Method 2.6.26
Test conditions: Single sense testing, heating from ambient to 150°C in three minutes, cooling to ambient in two minutes.
Compensation: Set to None (Calculated not required)
Failure Criteria: Coupon testing stops at 10% increase in resistance
Test Duration 3000 cycles (or until everything fails, whichever comes first)
No failure analysis is required. However, if reflowed samples perform worse than as built samples, failure analysis is strongly recommended.
Data shall be supplied in Excel format for further analysis.

Two IST coupons are in each board design as shown in Figure 13. They are specific material test through hole test coupons MAT20006A-32 and MAT20005A-40 at 32 mil (~0.8mm) and 40 mil (~1mm) pitch respectively. Note the design is generic and is designed for both 20 layer and 12 layer constructions. The layers removed to create a 12 layer construction do not affect the function of the coupon. However, when testing – it must be recognized on the 12 layer version that layers 6 through 9 and 12 through 15 do not exist in this version. As such, in the 12 layer version of this board, the capacitance holes for these layer connections are not connected and the capacitance measurements on the 12 layer boards should be made from the layer connections for layers 5-10, and 11-16 on the 12 layer boards (in addition to the other layers still existing). Complete details of the construction and testing of these coupons are available.

Four different sets (two each at 1mm pitch and 0.8mm pitch) of six IST coupons should be tested as follows:

- As built
- After 6X assembly reflow preconditioning using an actual reflow oven. The profile should conform to a standard SnAgCu Pb-free solder reflow profile with a peak temperature of 260+5/- 0ºC. 6X assembly simulation (using the IST tester) reflow preconditioning to 260ºC can also be done on a separate set of coupons.

If capacitance testing on the IST coupons after 6X reflow suggests delamination or material degradation then the delaminated after 6X reflow coupons do not need to be tested. They should be cross-sectioned to identify the delamination or material degradation. Note the 0.8mm pitch coupons are typically much more susceptible to internal delamination than the 1mm pitch coupons. If only the 0.8mm pitch coupons delaminate, the 1mm pitch coupons should still be tested.

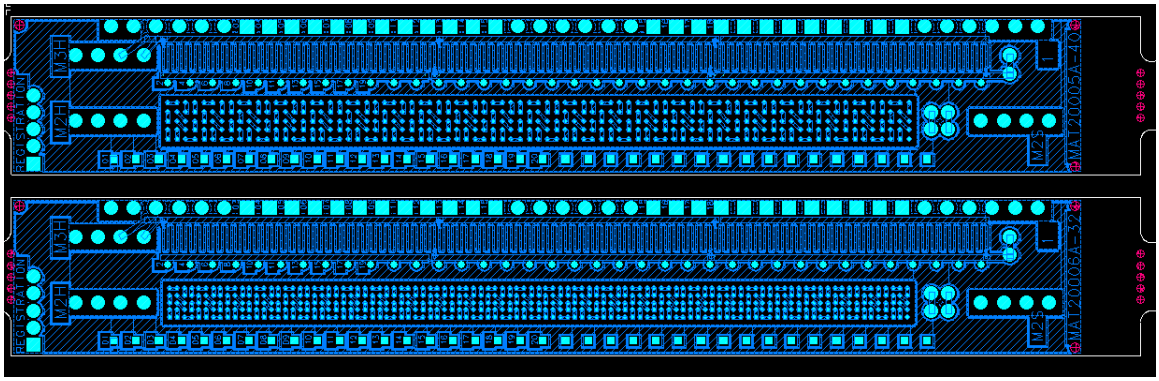


Figure 13: The two IST coupons used on the MRT-5 design.

Confirmation of Construction
The construction section is designed utilizing the border area of the coupon where identical copper plates (planes) are created on all internal/external layers (Figure 14 identifies the filled areas which represents a single plate). Individual connections to the plates are achieved using a drilled and plated through hole. The holes (one for each layer in the construction) are located on a specific spacing (grid/pitch) to enable measurements to confirm the capacitance values for each dielectric pair using a probe or test fixture. One of the surface layers (usually layer 1) should contain a numbering scheme (illustrated in area "A2") that confirms which holes are connected to each of the external and internal layers. In addition to the capacitance section are the conventional registration vias ("A1"), used to measure the drilled hole to internal layer registration.

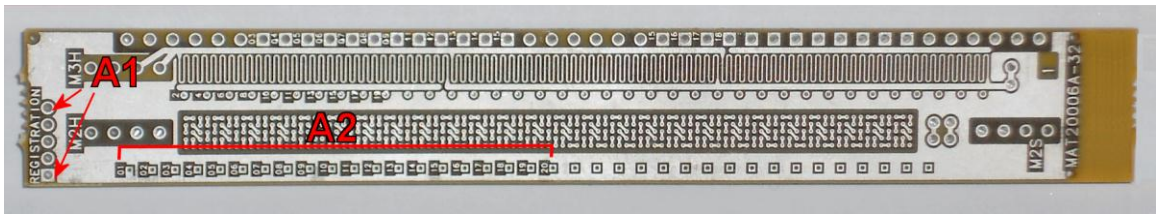


Figure 14: IST, Filled areas

The plates for each layer are designed to be identical in size/area (the thickness of copper foils or additional inner layer plating are not a factor); by measuring the capacitance for each pair of holes (L1 to L2, L2 to L3, etc.) you are effectively determining a bulk capacitance value associated to the combination of dielectric thickness and dielectric constant (Dk). Knowing/expecting that the B and C stage materials "should" have a consistent Dk, the most dominant factor affecting any changes in capacitance value will be related to the dielectric thickness between the two plates. Based on this principle we are able to correlate the relationship between the measured capacitance and the expected dielectric thickness. An initial microsection of the test vehicle is initially recommended to confirm the relationship between the electrical and mechanical measurements.

After the construction section measurements are collected the data can be plotted to illustrate the full product construction. Figure 15 shows an example of a 28 layer board, confirming the product was built symmetrically. Following the measurement of the first lot a capacitance reference profile is established, which is then used for comparison to any future panels or production lots, any changes to the profile are potential differences in dielectric spacing, or Dk properties. This creates a very useful tool for the PWB manufacturer because it gives a non-destructive capability to confirm that all coupons/panels/products are built with the same material construction. It is also very useful for determining material and process variations to establish tolerances for controlled impedance products.

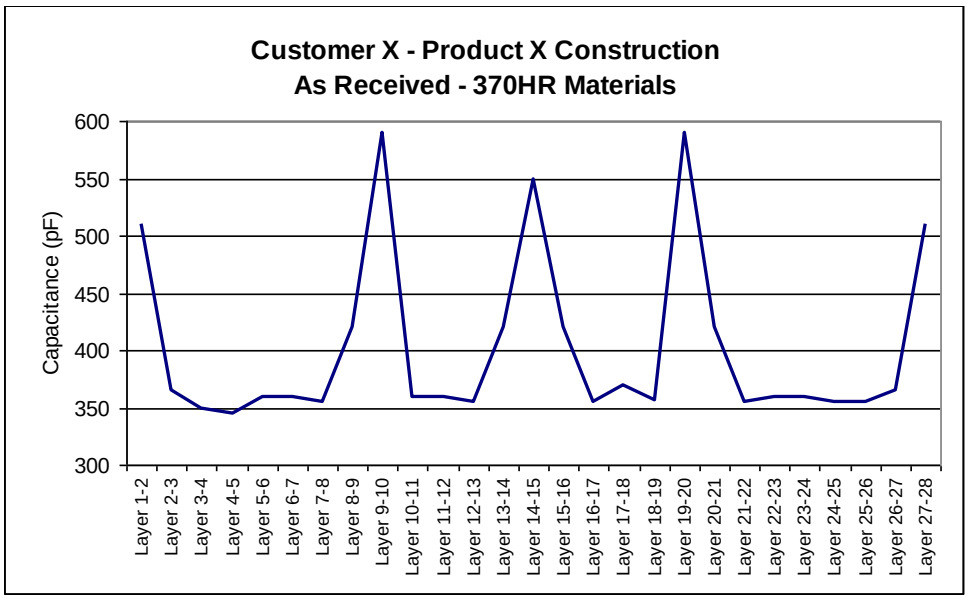


Figure 15: Construction Profile – Capacitance Readings

Converting the capacitance data into estimated thickness measurements can be achieved by completing initial microsection analysis on coupons previously measured with capacitance. Statistical comparison of the data can be used to generate algorithms and/or graphs to enable thickness predictions with future production lots. Figure 16 is an example of how the capacitance data can be converted into estimated copper to copper dielectric thickness measurements, to create a construction profile.

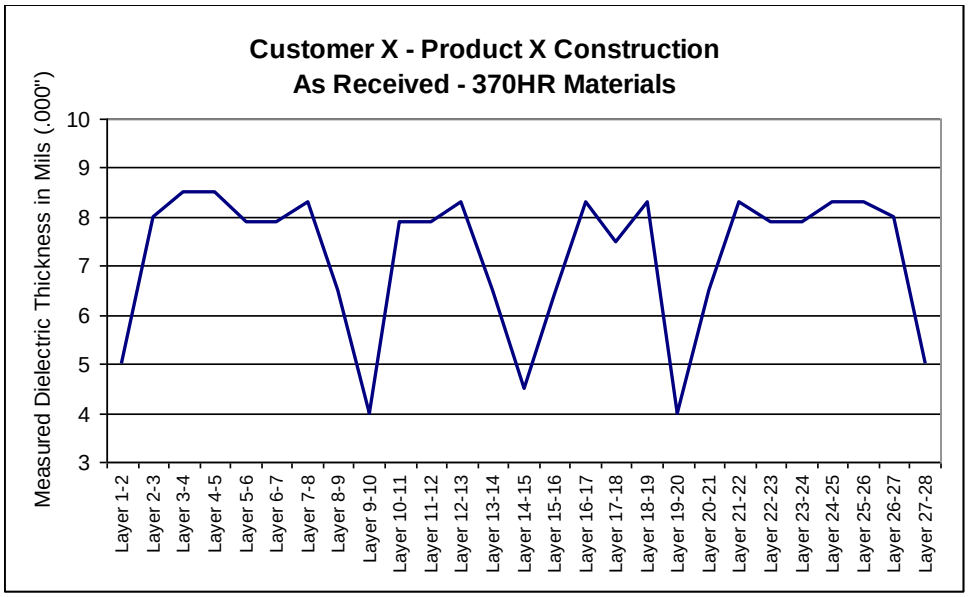


Figure 16: Construction Profile – Estimated Dielectric Thickness

Figures 17 and 18 illustrate how the capacitance values and the dielectric thickness measurements can be compared to establish an effective reference for future production lots. Figure 17 contains microsection measurement data that confirmed the majority of B and C stage dielectric layers measured between .006" (0.15mm) and .012" (0.3mm), with one exception of a measurement of .003" (0.08mm). In this case it is necessary to extrapolate the expected correlation between the thickness' of .003" (0.08mm) and .006" (0.15mm).

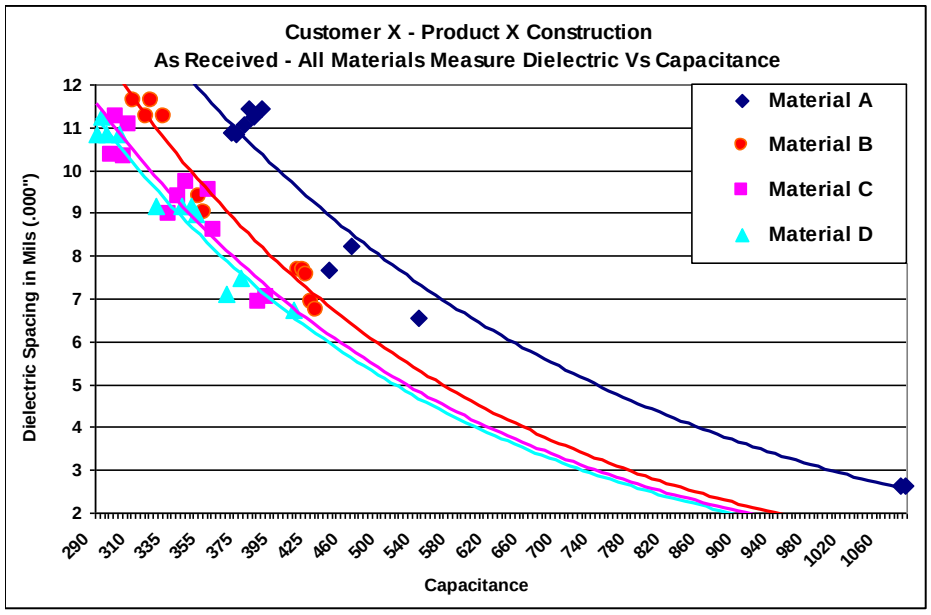


Figure 17: Dielectric vs. Capacitance

Figure 18 contains data from the smaller thickness delta of 006" (0.15mm) to .012" (0.3mm); this enables a more precise prediction to determine the anticipated dielectric thickness. If the baseline graphs are complimented with additional comparative data it assures a higher level of confidence in confirming product construction using capacitance data.

It is important to understand that if the PWB manufacturer uses more than one type of base material to build the same product it is necessary (due to the small differences in Dk) to establish the correlation between the capacitance value and the measured dielectric thickness for each individual material type.

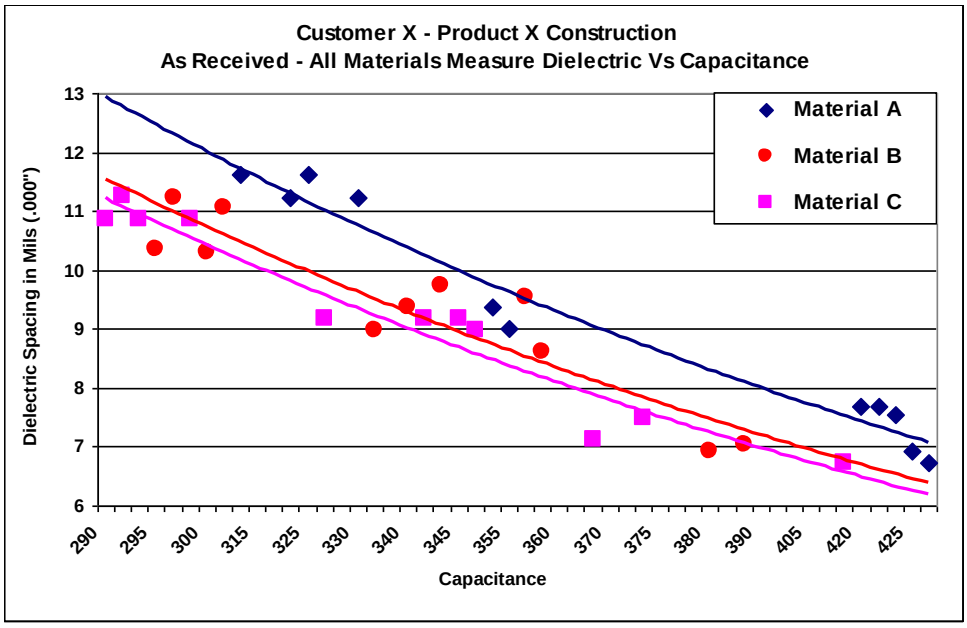


Figure 18: All Materials – Dielectric vs. Capacitance

Once the relationship/correlation between capacitance and measured thickness has been established it is the PWB manufacturer's decision which technique offers the greatest advantage for decision making on product construction. Important Considerations: The capacitance measurement is non-destructive, the thickness profile can be established with minutes rather than the hours and cost associated with microsection analysis. Using the capacitance profiles creates a baseline reference for subsequent measurements take after exposure to elevated temperatures experienced during the assembly and rework phase. The capacitance data combines the influences of dielectric thickness and material Dk; ultimately it is the electrical environment (not the absolute dielectric thickness) that is crucial for producing controlled impedance products.

IST Testing using DELAM protocol: Assembly Survivability

The IST Test section (shown in Figure 19) is similar to a conventional IST coupon, the testing protocol still requires the coupon to be heated on the IST tester in order to thermally cycle and measure for both via reliability and materials change. The coupon is designed with a "super-heat" circuit (four-pin connector shown as "B1"), located in the upper and lower layers and a traditional sensing circuit (four-pin connector shown as "B2") connecting the plated through vias from the top to the bottom layers. Area "B3" defines the hole to hole spacing (grid/pitch), it should be consistent with both the smallest grid/pitch in the product and the IST coupon. The capacitance holes ("B4") are connected to each of the internal copper planes; these connections are similar but not identical to product construction section.

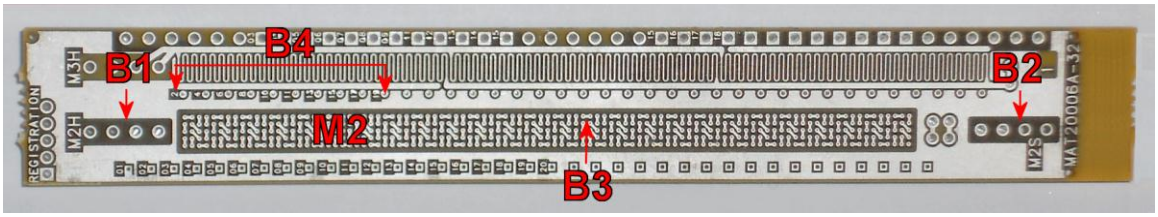


Figure 19: IST Test Section

The IST testing section contains two specifically designed circuits; one for heating and the other for measuring relative changes in via resistance. In addition each internal or external copper plane is connected; using a drilled plated through hole, to permit the measurement of capacitance, which if changed signifies the onset, or propagation of damage. There are differences related to the inner layer construction between each section; the product construction section (M1) is designed with plates on all external and internal layers, permitting the ability to measure every individual dielectric layer. The DELAM section (M2) is constructed with the same stack-up as the product, generally resulting in copper plates on every other layer (strip line). This means that each capacitance measurement is a combination of both a B and C stage material.

The primary difference in philosophy compared to the M1 coupon is that the M2 coupon is commonly tested before and after assembly temperatures, thermal cycling is usually completed to elevated levels which are designed to represent the Pb-free

reflow and/or rework thermal environments, commonly reaching temperatures up to 260°C. This level of temperature cycling is significantly higher than the standard IST test temperature of 150°C, used in traditional reliability testing. It must be understood that increasing the IST test temperatures to these elevated levels will change the fundamental understanding of measuring product performance.

For each section the capacitance values should be measured and recorded to establish a reference. The data from both sections (M1 and M2) should complement each other, regarding the B/C stage construction of the product. This information delivers effective feedback to the PWB manufacturer, assembler, or end use customer to confirm if the values are within expected ranges; non-compliance would generally be followed by traditional microsectioning to confirm (or refute) the findings. The benefit of combining the data from the M1 and M2 sections is that it offers a common platform for reference, based on the product construction.

The IST test protocol (testing to 150°C) is approved industry standard, as defined in the IPC Test Methods Manual (TM 650 Method 2.6.26 - DC Current Induced Thermal Cycling). This methodology allows a very rapid evaluation of a representative coupon's overall reliability. It is particularly sensitive to measuring wear-out and fatigue associated to failures found in barrel cracking, micro via failures and interconnects separation, which makes it an ideal test for evaluating the effect following leaded and lead free assembly/rework.

Capacitance measurements (using a standard capacitance meter) should be made on coupons before and after assembly reflow or reflow simulation. Significant change (greater than 4% reduction) in the capacitance after reflow is typically an indication internal delamination or other defects. Should these changes occur, it may be best to discontinue further testing of the material (after 6X Pb-free reflow) and perform immediate failure analysis. Since this testing gives quick feedback on the survivability of the material to assembly reflow, it is recommended that it be done as soon as possible and before committing materials to additional post reflow testing (IST, air-air, etc.). This may (for example) enable a quick screening of the ability of a material to survive one or both of the higher complexity 20 layer stackups, before committing to the cost, time and expense of the testing.

Three each of the 0.8 and 1mm pitch IST coupons should be IST preconditioned to 260ºC, with the capacitance measurements after each preconditioning cycle, until the measurements change indicating delamination or 12 cycles have been completed. This is a quick measure of the thermal robustness of the material.

All results will be reported in a spreadsheet format, identifying the coupon number, circuit type, failure mode and number of cycles to failure.

Data analysis of via failures in IST thermal cycling should also be done on a log normal plot, similar to the air-air thermal cycling. Failure analysis and the results of the air-air thermal cycling are needed to make a final judgment. The comparison of the IST results to the air-air results allow for a proper baseline for monitoring of production plating using IST.

Evaluating the IST Data

IST sample sizes are typically smaller than that for ATC, however they can perform similar functions. The speed and lower cost of the IST testing also allows for comparison of as-built to after reflow performance of the materials.

To evaluate the capacitance data, it is best to plot the changes in the capacitance after 6X reflow at 260°C compared to the as built construction. When using the simulated reflow of the IST tester, this should be recorded after each reflow. A change in capacitance of 4% is typically considered a major change, but some allowance for moisture may be necessary. Comparison of the plots as shown for the WIC-20 coupons later is also applicable for the capacitance testing on the IST coupons. If delamination occurs in the materials, the failures will typically be near the center of the board (layers 8-12 on the 20 layer construction). Figure 20 is an example plot of capacitance changes showing material degradation. Figure 21 is an example plot of capacitance changes on a more robust material. Note that both of these do show changes in the material through reflow.

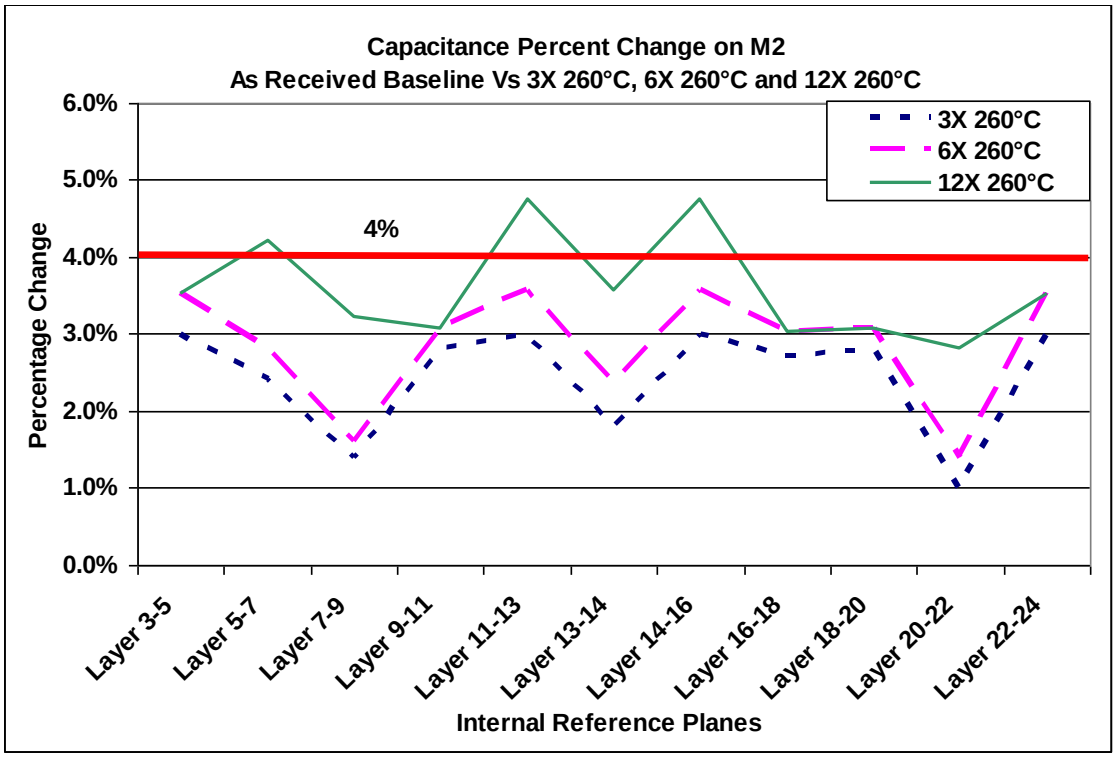


Figure 20: Example of Capacitance change on the M2 circuit with reflow, showing material degradation.

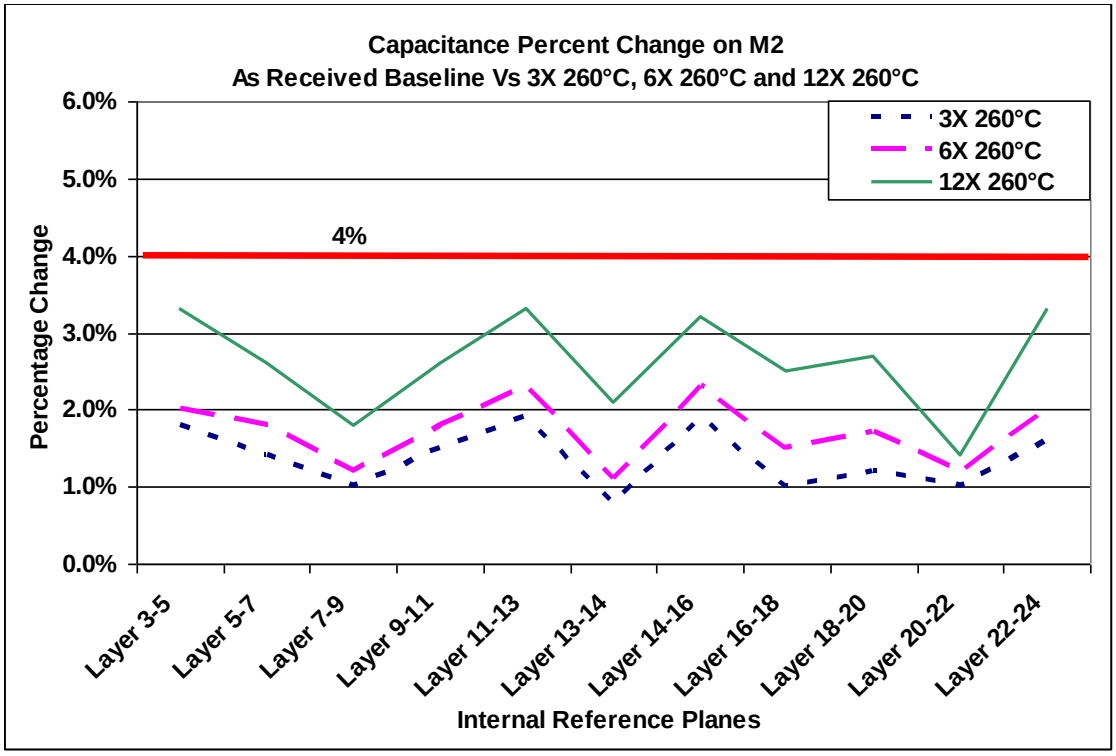


Figure 21: Example of Capacitance change on the M2 circuit with reflow, showing excellent performance.

IST thermal cycling should typically show a reduction in life after 6X reflow. If the data reflects an increase in life, the coupons likely show material degradation. There will typically be differences between the performance at 1mm pitch and 0.8mm pitch. As with air to air thermal cycling, if these are significantly different, they should be investigated further. Because of the smaller sample size, the slope of the failure distribution when plotted Weibull or log normal is not as sensitive to material degradation as the air to air thermal cycling, but a major slope change should be investigated.

CAF Test Section:
The CAF test section is a limited hole-wall to hole-wall CAF test specifically designed to evaluate whether CAF performance degrades after 6X assembly reflow. As such, testing is required with samples both before and after reflow. Figure 22 below gives an overview of this section.

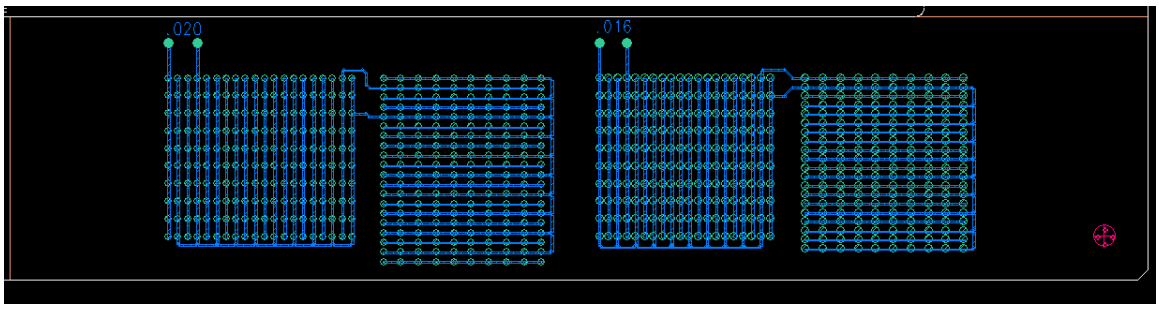


Figure 22: Through Hole Wall-Wall CAF test section

There are groups of holes at .020 inch and .016 inch wall to wall spacing. The sample size on the board is 380 (190 in X and 190 in Y) locations at each minimum spacing. The required sample size is eight (or more) coupons before reflow and eight after, with both dimensions tested (a total of 32 nets for each construction tested) for continuous monitoring in CAF. The goal is to generate failures, and the .016 hole wall spacing will typically fail before 1000 hours in this testing even on CAF resistant materials. This enables comparison of the failure performance before and after reflow.

The test procedure is as follows:

Test per IPC-TM-650 Method 2.6.25 (except using these test coupons)
Test conditions: 65°C/87+3/-2% Relative Humidity
Test Voltage: 100V
Test Duration 1000 Hours (or until everything fails, whichever comes first)
Precondition as required by the test method (note – do NOT exceed the bake period)
No failure analysis is required. However, if reflowed samples perform worse than as built samples, failure analysis is strongly recommended.

Data shall be supplied in Excel format for further analysis.

Evaluating the CAF Test Data
The CAF data provides a basic characterization of the material performance at hole wall spacings of 16 and 20 mil. The hole size used in this is intentionally relatively large (35 mil drill size prior to plating) to minimize the impact of drilling on the CAF results. The CAF results are typically plotted vs. time as shown in the example in Figure 23. These results may also be plotted Weibull or three parameter Weibull. Figure 24 shows an example of a three parameter Weibull plot showing degradation after Pb-free reflow. The results can be directly related to different environmental conditions and hole spacings [25-33]. The 20 mil hole-wall to hole-wall spacing is a good representation of through vias on a 0.8mm pitch BGA and the 16 mil hole-wall to hole-wall spacing allows for some margin on this number to reflect the reality that manufacturing processes, not just material properties, play a role in CAF performance. In addition to characterizing the basic CAF performance of the material under test, a number of different results are common when testing CAF with this coupon. These include;

- Degradation of CAF performance after reflow. This typically suggests material degradation with Pb-free reflow.
- Improvement of CAF performance after reflow [7]
- No significant differences between CAF performance before and after reflow
- Differences in CAF performance specifically between stackups. This typically reflects the challenges in wetting certain glass styles.

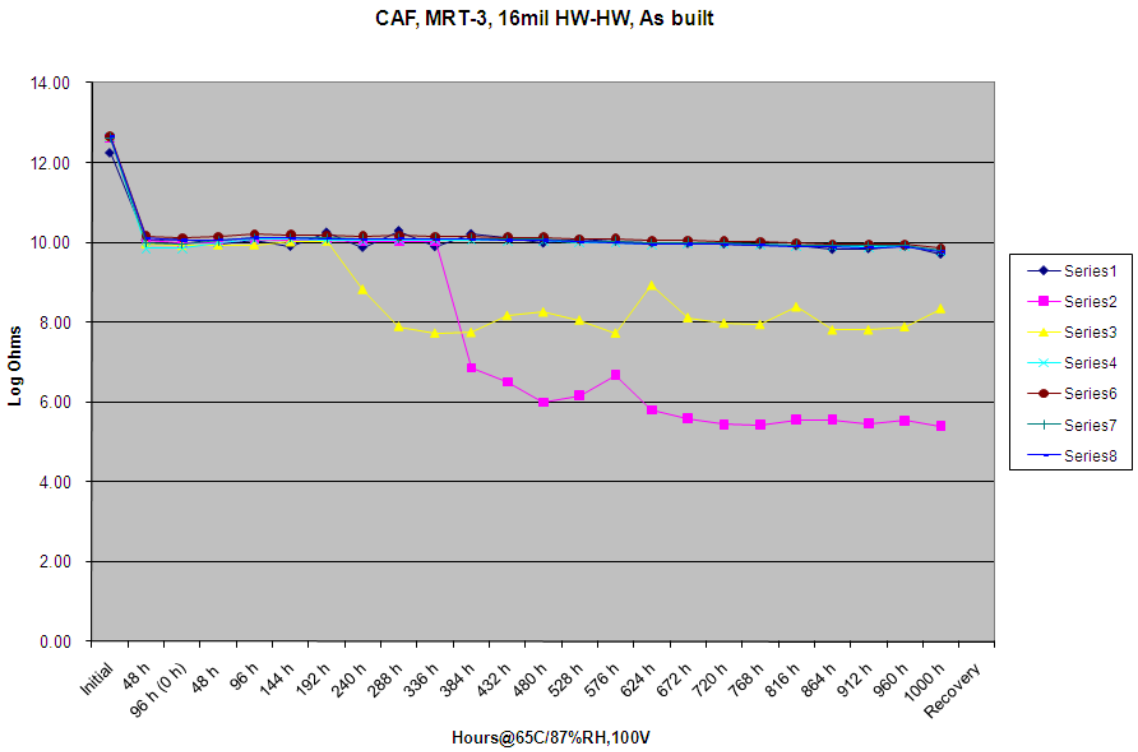


Figure 23: Typical CAF data plot, showing first failures at 240 hours

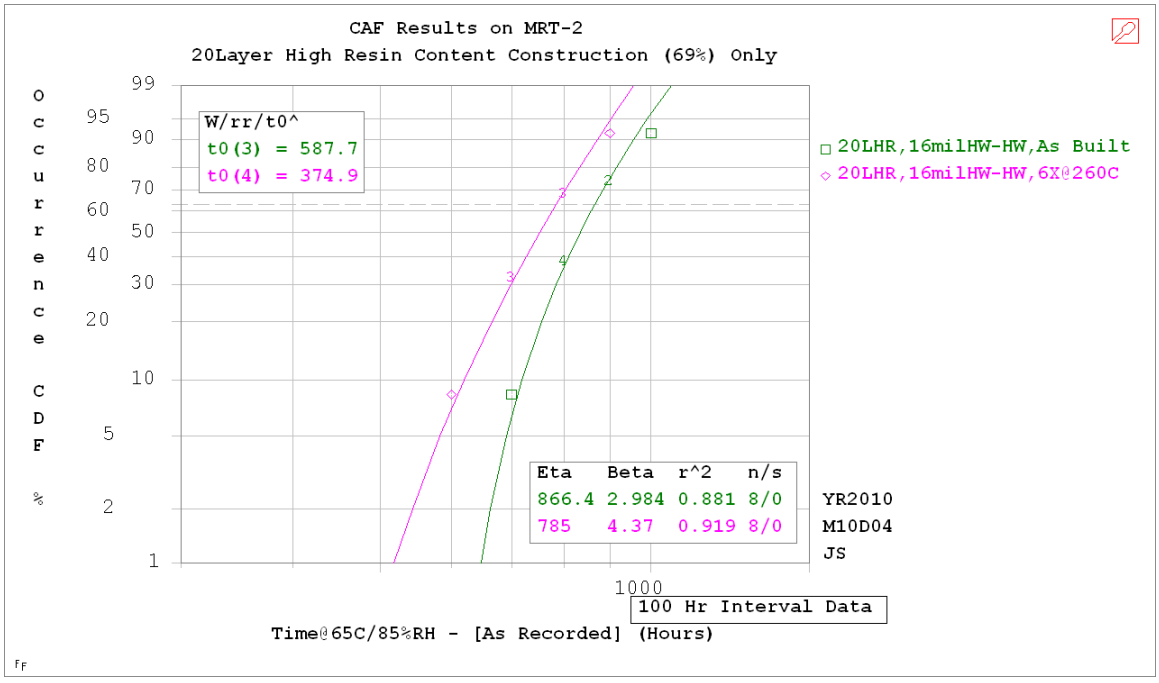


Figure 24: 3 parameter Weibull plot of CAF data showing degradation of CAF performance after Pb-free reflow.

Thermal Analysis

Thermal analysis, Dynamic Mechanical Analysis (DMA), Thermo-Mechanical Analysis (TMA), Differential Scanning Calorimeter (DSC) shall be done on the finished boards both before and after 6X Pb-free assembly reflow. The following data both before and after reflow should be reported at a minimum:

Tg (by DSC, TMA) (IPC-TM-650 Method 2.4.24, TMA, DSC)
Modulus (from DMA) (IPC-TM-650 Test, Method 2.4.24.2)
CTE Z% (50-260C) (IPC-TM-650 Test, Method 2.4.41)

CTE <Tg (IPC-TM-650 Test, Method 2.4.41)
CTE >Tg (IPC-TM-650 Test, Method 2.4.41)
Td (IPC-TM-650 Method 2.3.40 or IPC-TM-650.2.4.24.6)
T-260 (IPC-TM-650 Method 2.4.24.1)
T-288 (IPC-TM-650 Method 2.4.24.1 modified per paragraph 6.1 to 288°C)
T-300 is also recommended but not mandatory (IPC-TM-650 Method 2.4.24.1 modified per paragraph 6.1 to 300°C)
All thermal analysis (except DMA) shall be done in the thermal analysis test area, which is void of copper on all layers. The DMA test area (also void of copper) is for DMA testing. See figures 4, 5, and 25. The same data may also be taken in areas with copper.

A comparison to supplier data sheets for the material(s) tested is also useful.

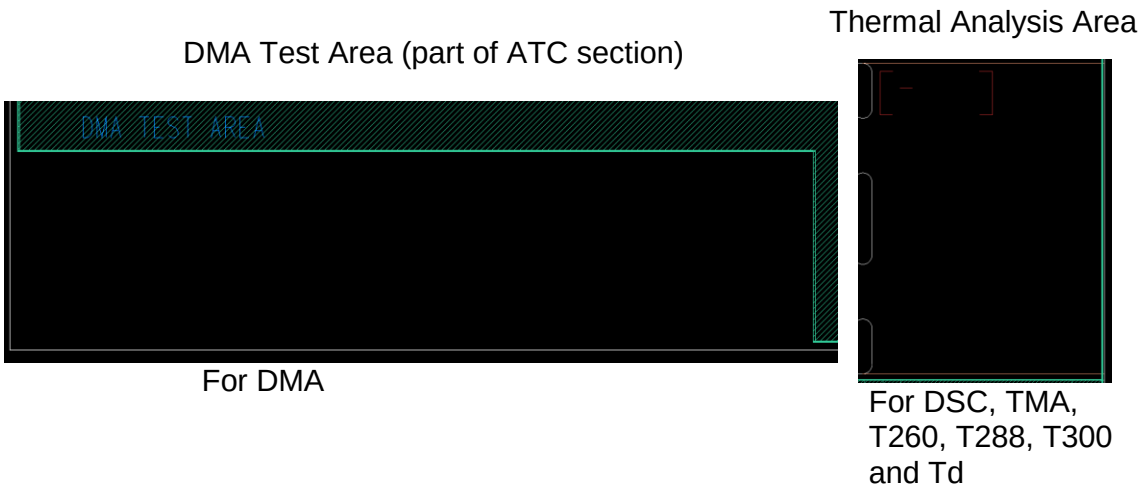


Figure 25: Close of the DMA and Thermal Analysis Test areas shown in figures 4 and 5. Note that they are void of copper on all layers.

Using the Thermal Analysis Data
The thermal analysis data is valuable in understanding how the material behaves in an actual multilayer printed wiring board and the thermal margins of the materials. Additionally the data can be used to predict plated through hole performance, either empirically or statistically [1,4,18]. As a good data set is collected on a number of materials the data becomes more valuable in understanding material performance.

WIC-20 Coupons
This design includes two identical IBM WIC-20 style coupons, specifically preconfigured for this design. An example is shown in Figure 26. TDR Impedance measurements can be made, if desired, on the inner row of test points which are identified by layer numbers 3, 5, 7, 9, 12, 14, 16, and 18 with the associated reference plane for these TDR measurements in the outer row of test points identified by layer numbers 2, 4, 6, 8, 10, 11, 13, 15, 17 and 19. Capacitance measurements are made between the plane pairs identified by the colored pairs of arrows. For the 12 layer construction, layers 6 through 9 and 12 through 15 are not fabricated. The Yellow arrows show that capacitance measurements should be made between test points for layer 4 and 10 and also 11 and 17, in addition to the pairs at layers 2 and 4, 10 and 11, 17 and 19. Note that the layer 4-10 and 11-17 measurements (series capacitance) are also a good check on the accuracy of the individual measurement on the 20 layer constructions.

These coupons include a 20 by 20 array of 0.25mm through hole vias on 0.8mm pitch and test points for making Time Domain Reflectometer (TDR) impedance measurements and capacitance measurements. Alternate layers include traces for TDR surrounded by reference planes for the TDR, which also serve as capacitance planes. Capacitance measurements shall be taken before and after 6X@260°C reflow. Changes exceeding roughly 2% (this is only a guideline) in capacitance should be investigated by cross-section for material degradation. The best way to identify this is to plot the results, investigate outliers (if any). Outliers (even if less than 2% change) typically identify material degradation. See Figure 27 below for an example of the plots and further explanation.

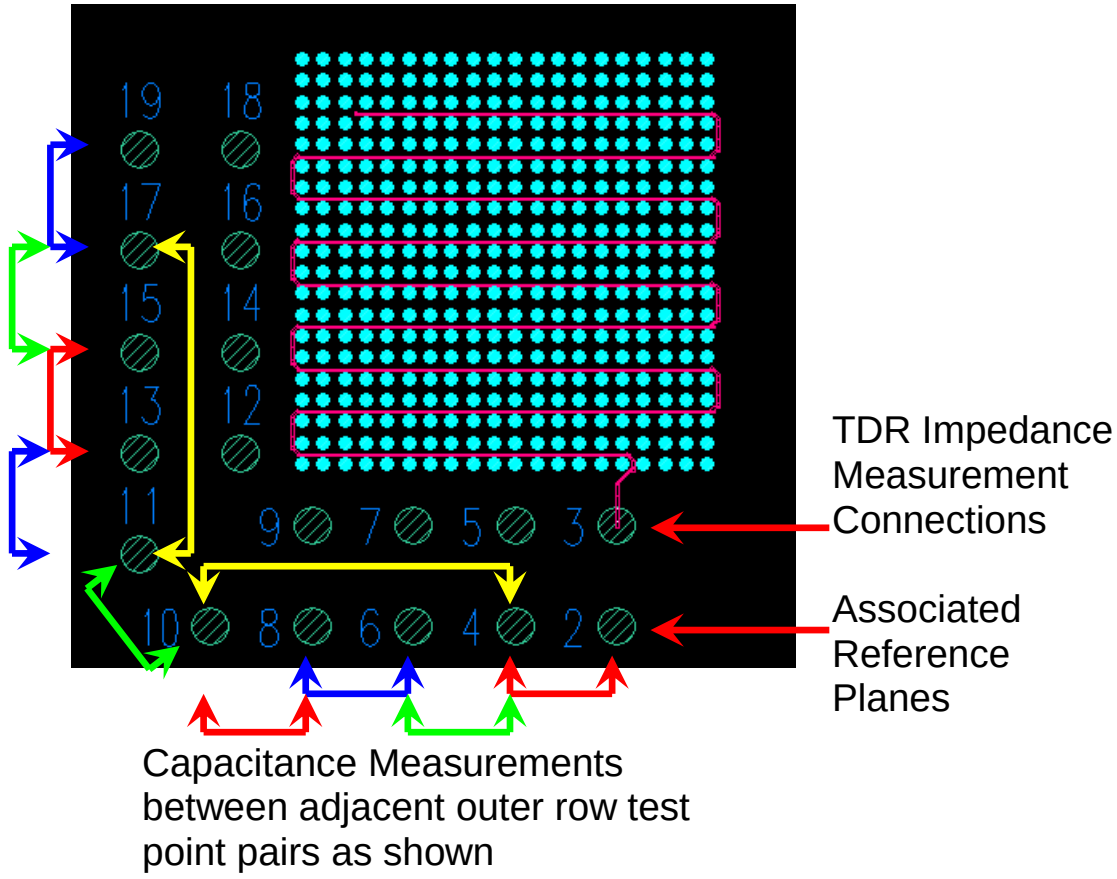


Figure 26: Example of WIC-20 Coupon. Layer 1 and Layer 3 shown.

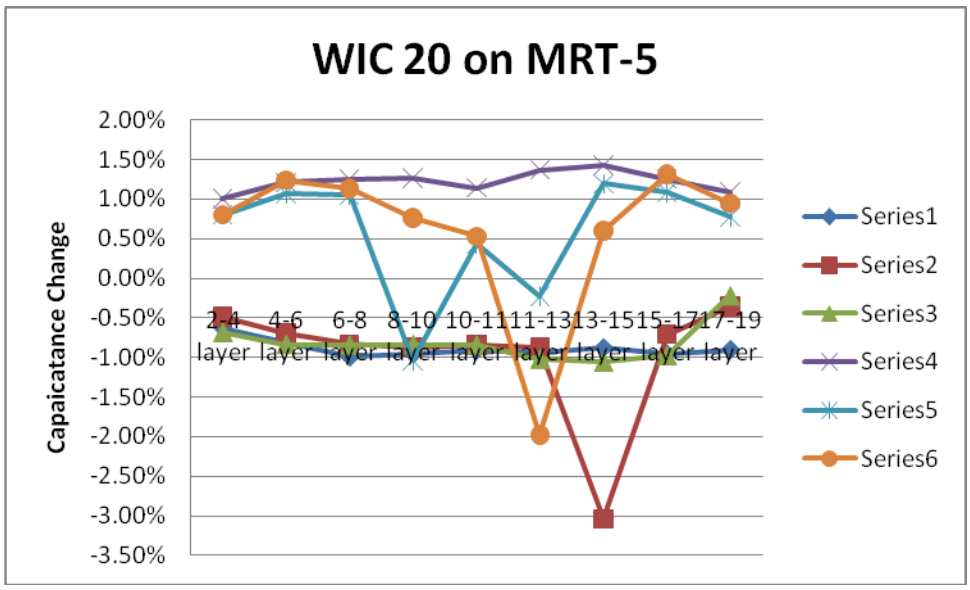


Figure 27: Example plot of capacitance changes after reflow compared to before reflow. In the above example, Series 1,2 and 3 are "dry" (after 24 hours @125°C°) and then reflowed, and Series 4, 5, and 6 are "wet" (after 168 hours of 85°C/85%RH). Series 2, 5 and 6 are clearly indicating internal material damage.

This coupon design allows for a quick method of determining material integrity at 0.8mm pitch, and the sensitivity of the material and construction to moisture.

Testing of this coupon design has shown that the TDR is often insufficiently sensitive to internal delamination (unless it is severe). As such, TDR requirements are optional (though they still can be valuable) and the focus should be on capacitance.

Measure the capacitance (using a standard LCR meter) before and after 6X reflow at 260°C. If changes in capacitance occur greater than approximately 2% (best to plot the data and analyze outliers as detailed above), cross section and analyze the cause. This should be done on all boards going through reflow. Note it is optional, but may be in the material supplier's/fabricator's interest to measure these after each reflow cycle rather than only as built and after reflow. Depending on the application, it may be useful to know at what reflow degradation begins. This is only possible if measurements are made between each reflow cycle.

The following test shows the robustness of the material to moisture ingress. It is very similar to the IPC-JEDEC J-STD-020 testing for moisture sensitivity level 1 modified for 6X reflow (to better represent what actual bare boards experience) that is used to classify moisture sensitivity of components. Six or more coupons (18 preferred) should be used for this testing.

Procedure:

- Bake the coupons for 24 hours minimum at 125 +5/-0 °C. This step is intended to remove moisture from the coupons so that they will be ''dry.'' Longer baking time may be necessary to ensure this starting condition.
- Weigh a sampling (at least three) of these coupons accurately using a high precision scale to establish the dry weight. Record these measurements.
- Measure and record the capacitance as detailed above.
- Split the coupons into two groups, ½ shall be tested dry, and ½ shall be tested after moisture soak.
- Place ½ of the coupons in a clean, dry, shallow container so that they do not touch or overlap each other. Place these in a temperature/humidity chamber at 85°C/85% relative humidity for 165+5/-0 hours.
- A sampling (at least three – same three as previously measured) of the moisture soaked coupons should be weighed after removal from the temperature humidity chamber to record determine the moisture content (percentage increase from dry measurements).
- Measure and record the capacitance of the moisture soaked coupons as detailed above.
- Not sooner than 15 minutes and not longer than 24 hours after removal from the temperature/humidity chamber, subject the coupons to six cycles of 260+5/-0 °C reflow. The time between reflows shall be five minutes minimum. Dry coupons should be tested similarly.
- Measure and record the capacitance as detailed above. If changes occur greater than 2% in capacitance or a plot of the data shows outliers in the distribution compared to the prior to reflow measurements, cross section and analyze the cause. Note that it is not necessary to cross-section all coupons if delamination/material degradation is found. A sample is adequate.
- Compare the results between the dry and moisture soaked coupons. Plot these three different measurements (dry, after moisture soak, and after 6X reflow). The capacitance will change between these, but the trend should be similar. Outliers typically indicate internal material damage.

Boards that pass this without changes greater than 2% in capacitance or outliers in the plots are clearly not moisture sensitive. They would be the equivalent of IPC/JEDEC MSL1 for components. If they cannot pass this, then they should be treated as moisture sensitive.

Pad Pull Testing

The MRT-5 incorporates five BGA pad patterns located on the bottom side of the Electrical Test section. They include pad sizes diameters of.025" (27 x 27 mm 256 PBGA footprint), .020" (17 x 17 mm 172 PBGA footprint), .014" (7.4 x 5.7 mm 40 PBGA and 10x 10 mm 100 PBGA footprints), and .012" (5.35 x 5.35 mm PBGA footprint). These are provided to enable pad pull or shear testing. Many in the industry consider that the results of this type of testing are indicative of whether or not the materials are prone to pad cratering. However, there is conflicting data with this. If done, testing should typically be done per the upcoming (but not yet released) IPC-9708, Test Methods for Characterization of PCB Pad Cratering. The .025" and/or .020" pads are recommended for this testing. Note, shear testing (with solder balls attached) and pull testing (hot and/or cold bump pulls, or hot pin pull) may give different results and this may or may not be indicative of pad cratering performance of the material.

Summary

- A multilayer board will much better represent actual material use than will bare material samples.
- A standard multilayer printed wiring board for material reliability evaluations has been presented and is made available to all and offered to the IPC as a standard test vehicle. Having a standard design enables comparisons between materials and not only enables evaluation of the materials, but provides data that can lead to improved material performance.

- The design has already been used on over 80 different materials from virtually every major material supplier worldwide.
- The design not only provides needed data for thermal and electrical characterization of materials, but is specifically designed to understand the Pb-free assembly survivability and reliability of these materials. Sections are designed specifically to support testing and evaluation of plated through hole reliability using air-to-air thermal cycling and IST, impact on material damage, product construction, consistency of B and C stage materials, electrical characterization, CAF, moisture sensitivity and pad pull strength.
- The design has sufficient flexibility to cover many different possible constructions.

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A Standard Multilayer Printed Wiring Board for Material Reliability Evaluations

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Wayne Rothschild, IBM (retired), NY

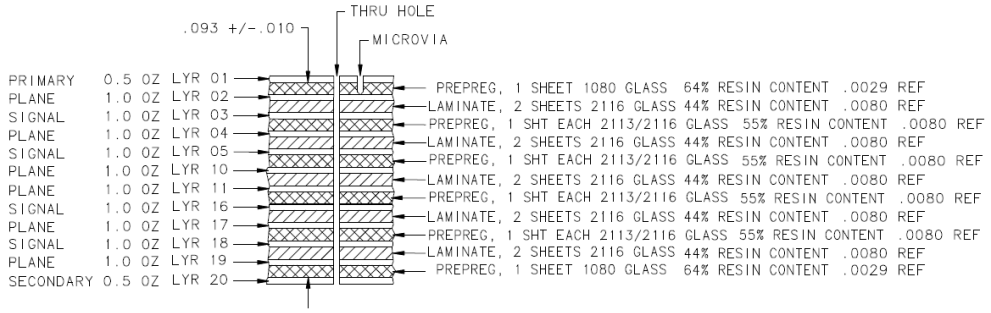
IPC/APEX, April 2011, Las Vegas, NV

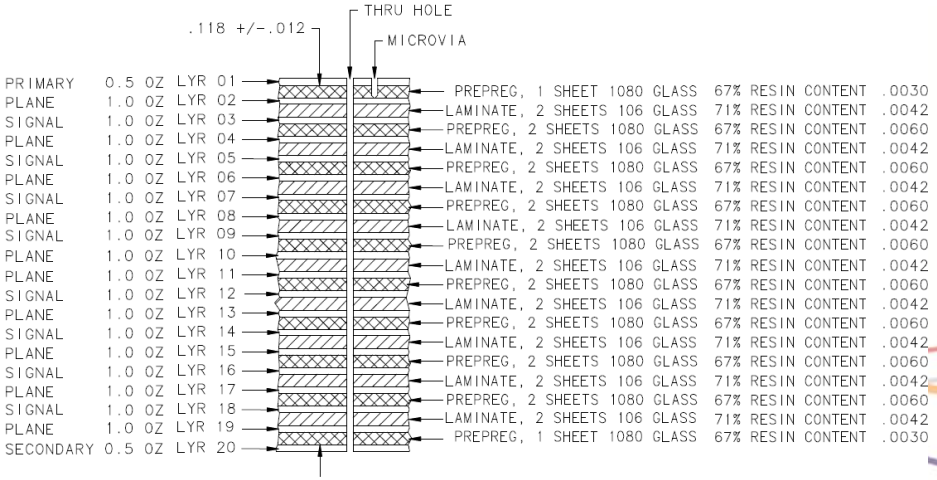
Introduction

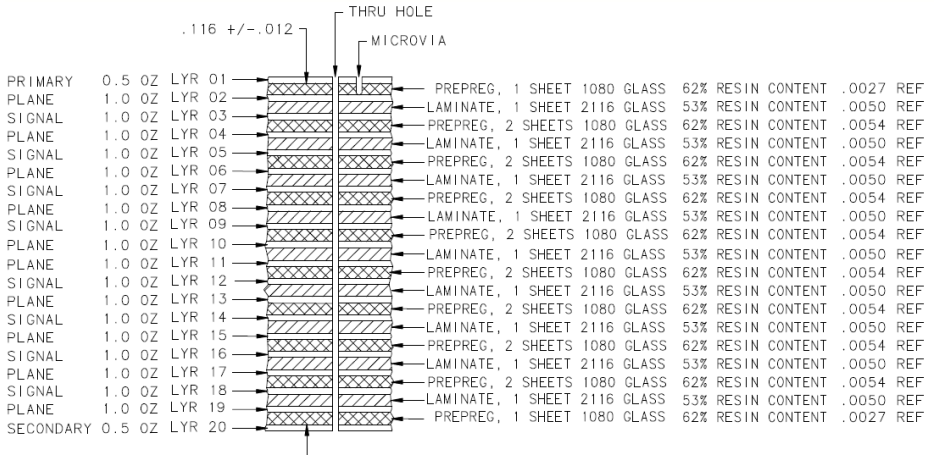
- Specifying Laminates for Pb-free assembly compatibility is much more difficult that with SnPb.
  - Tg alone is not nearly enough
  - Properties of materials give a starting point but inadequate of themselves
  - Testing/evaluation required
    - Over 80 materials (and growing) tested on this generic multilayer test vehicle design
      - <20% are acceptable in complex constructions

Generic Test Vehicle

- One artwork, 3 standard constructions – fully detailed
  - 12 layer 50% RC, .093”
  - 20 layer 58% RC, .116” thick
  - 20 layer 69% RC (High resin), .118” thick
    - Represents HLC board ~ 26-28 layer in similar thickness
- Test Ideally all 3 constructions, more typical 1 or 2







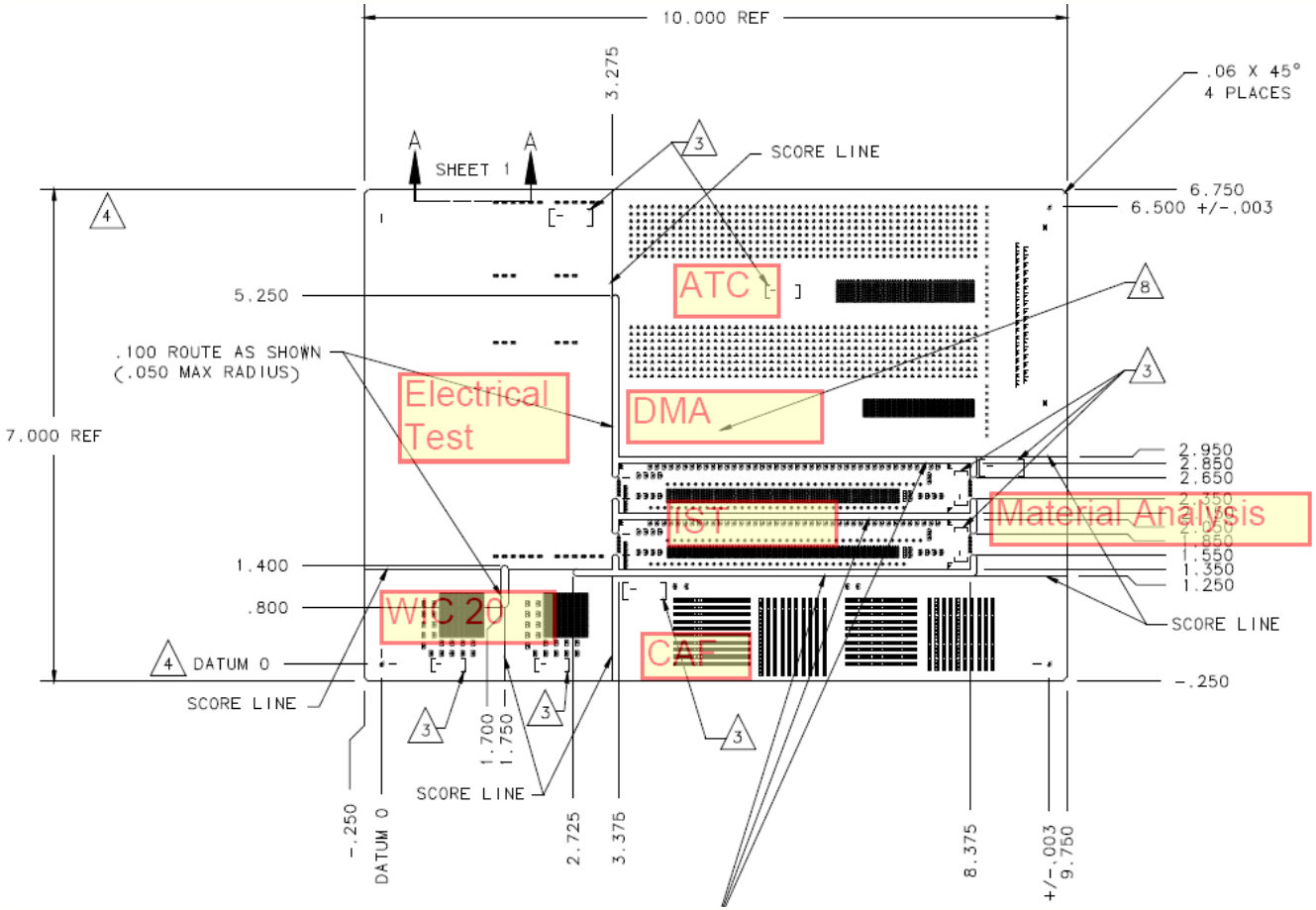
What To Evaluate (1 of 2)

- Assembly Reflow survival – Visual and Cross-section after 6X@260ºC reflow (6X@288ºC solder float)
  - Various locations/via pitches
  - Without baking – not typical of actual product use
- Thermal Analysis – both before and after assembly reflow (Typically 6X Pb-free), including DMA, TMA, DSC analysis.
- Air-Air thermal cycling (typically after 6X reflow only) of different hole sizes and pitches
  - Air-Air thermal cycling can be directly related to field life.
- IST testing –before and after assembly reflow (typical 6X Pb-free) and/or preconditioned using simulated IST Pb-free preconditioning.
  - Specially designed material testing coupons, one with 1mm pitch vias and the other with 0.8mm pitch vias.

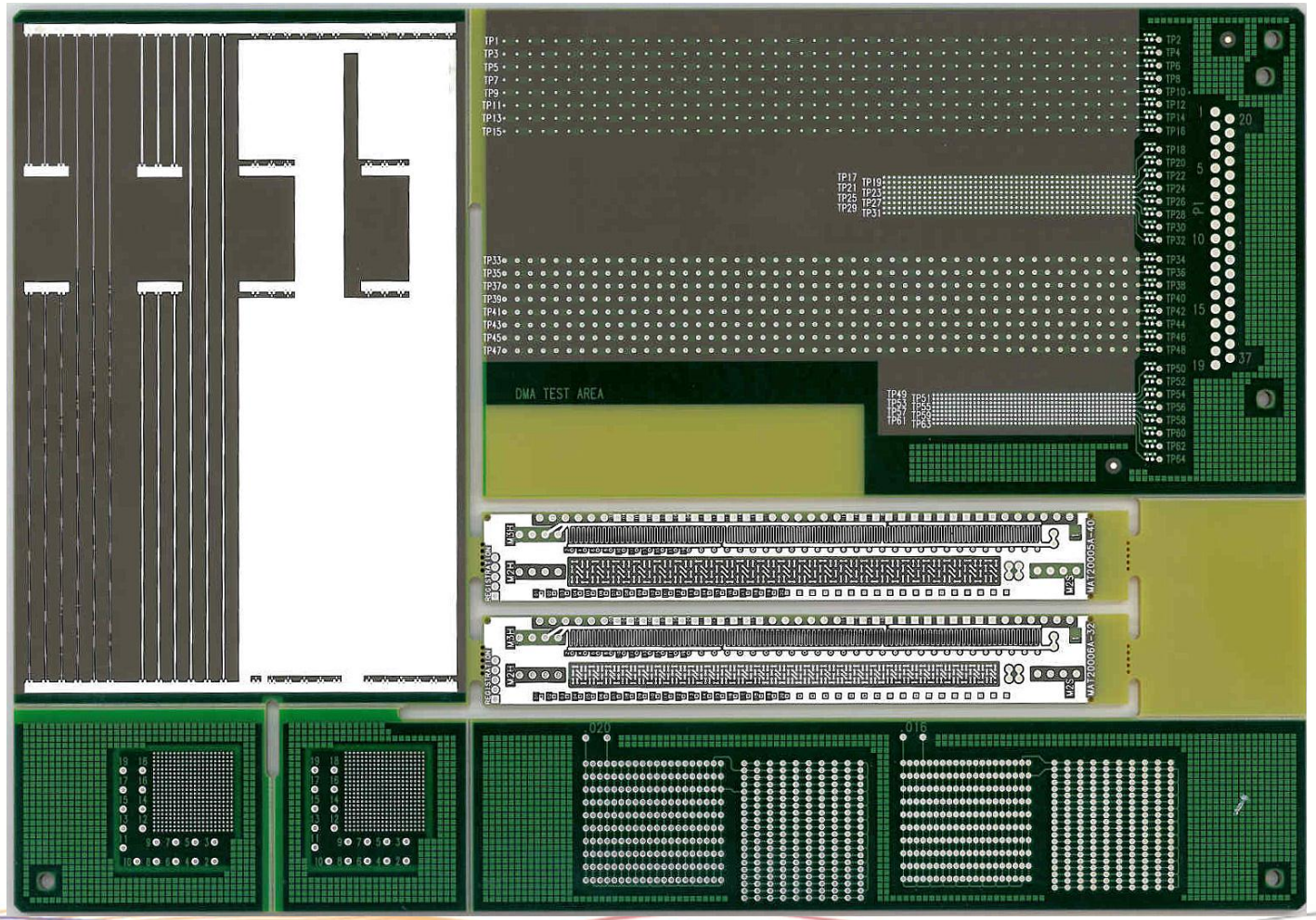
What To Evaluate (2 of 2)

- DELAM Testing – Evaluation by Capacitance measurements recorded both As Received and after 6X reflow.
  - Changes in capacitance indicate the presence of material damage
  - Subsequently confirmed or denied by microsection analysis.
  - Also confirmation of product construction and determination of consistency between the B and C stage materials.
- Electrical testing – S-parameter data for both microstrip and stripline configurations. Permittivity (Dielectric Constant – Dk) and Loss Tangent (Dissipation Factor – Df) can be extracted and plotted using this design.
- CAF Testing – Limited CAF testing – specifically designed to evaluate only the hole-wall to hole- wall CAF performance for through-hole vias and the effect of reflow on the CAF performance.
- Two WIC-20 coupons (based on IBM's WIC-20 design) allow for quick assessment of material survivability and material integrity after Pb-free reflow by the use of TDR and capacitance measurements. They also allow the investigation of the influence of moisture content on this performance.
- SMT pads on the backside of the electrical test section to support pad pull testing per IPC-9708, Test Methods for Characterization of PCB Pad Cratering (in draft at this writing).

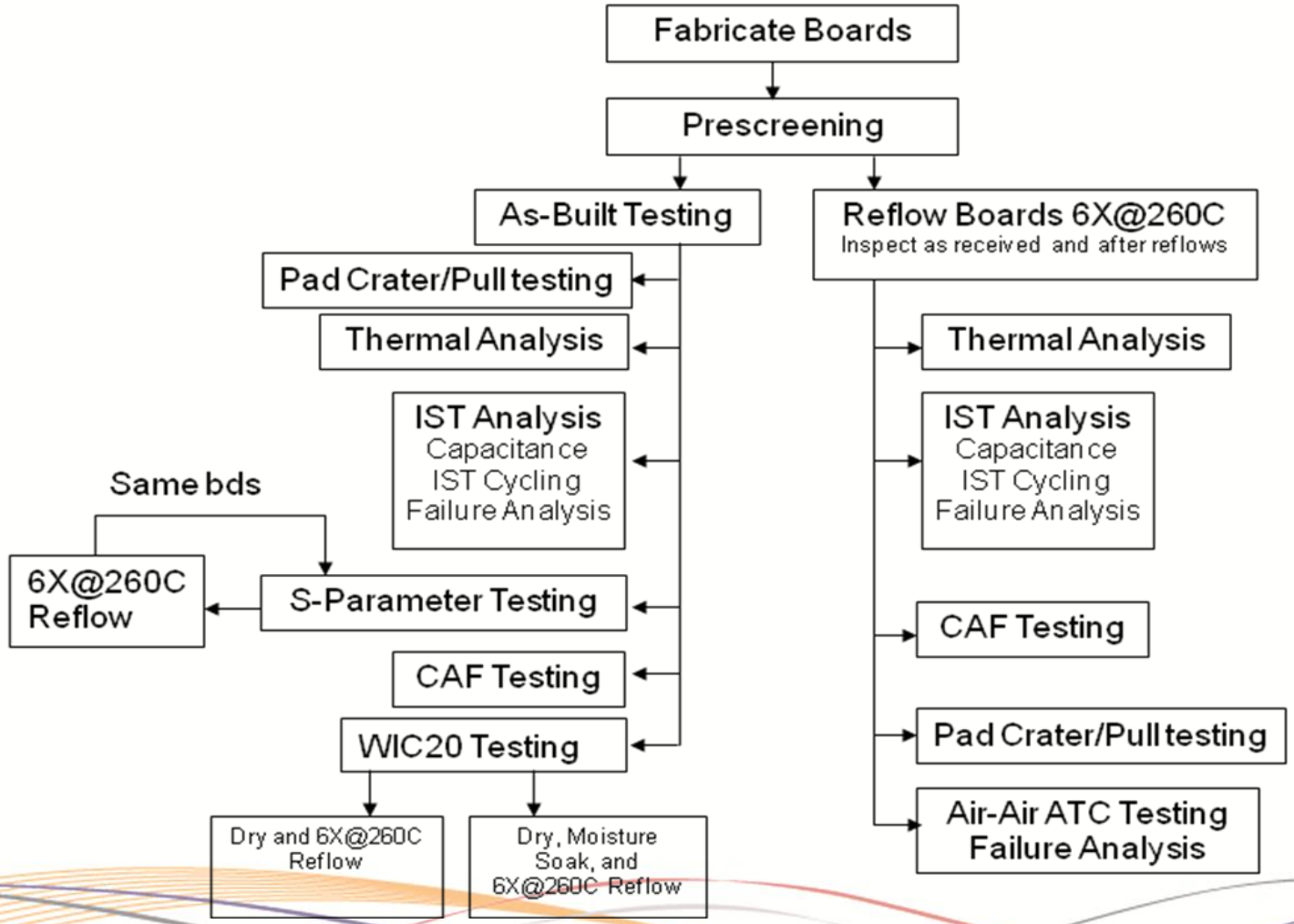
Design Overview



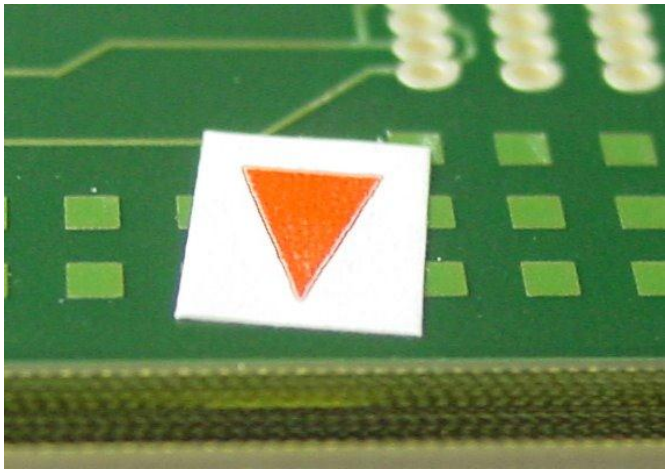
Actual Test Board

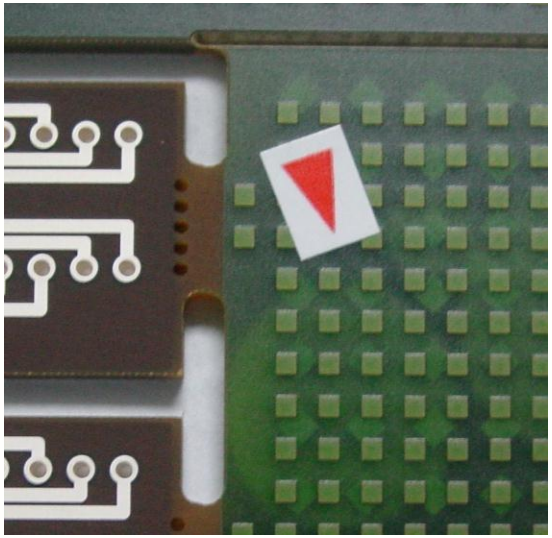


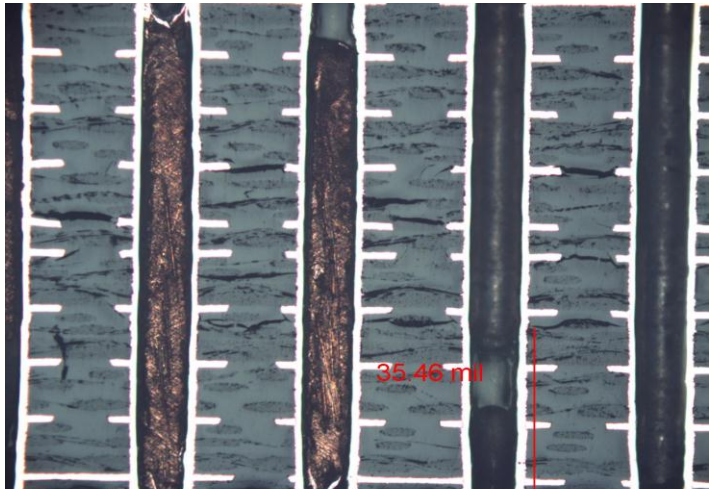
Test Flow Chart – 20 boards plus 1-2 for Prescreening



Some typical Reflow defects



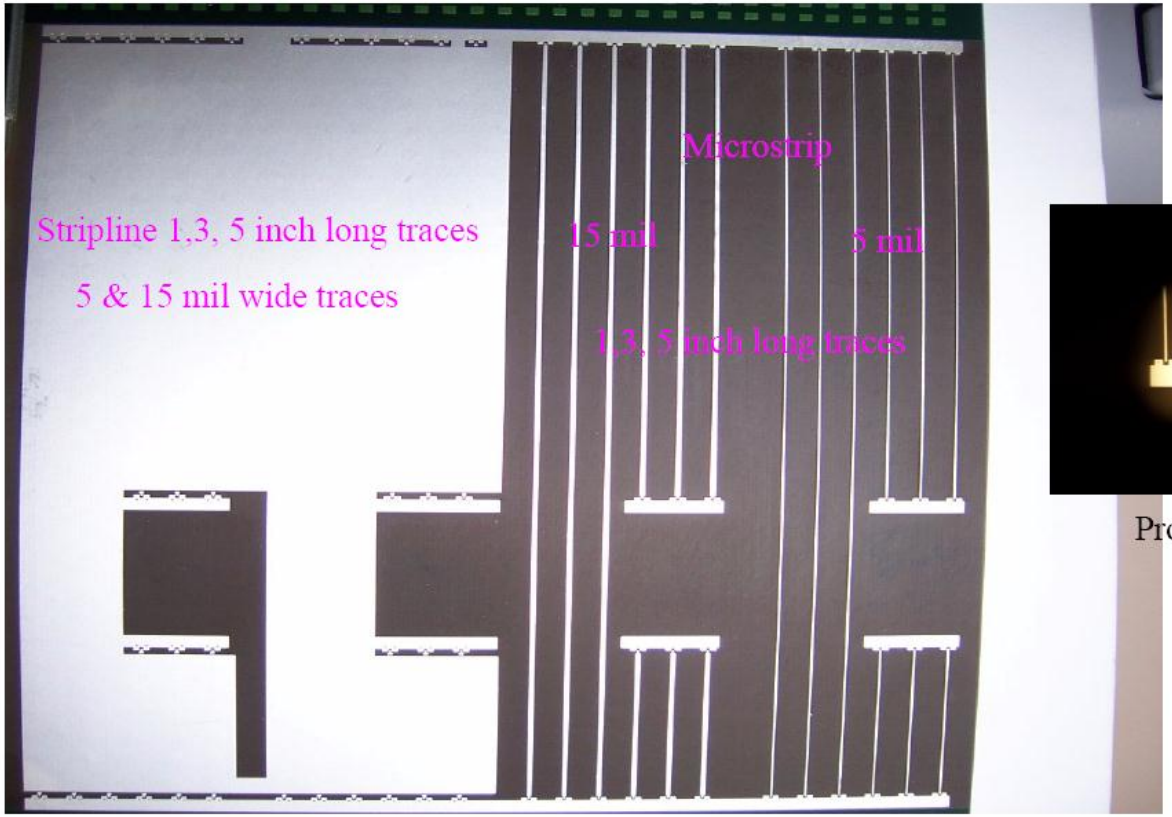


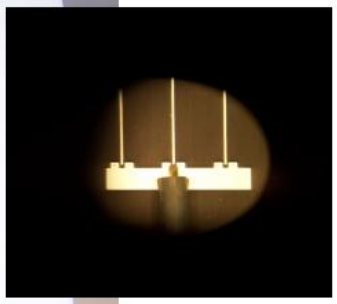


Edge delamination, Visible internal delamination, Hidden delamination between vias, Vertical Eyebrow cracking

Electrical Characterization

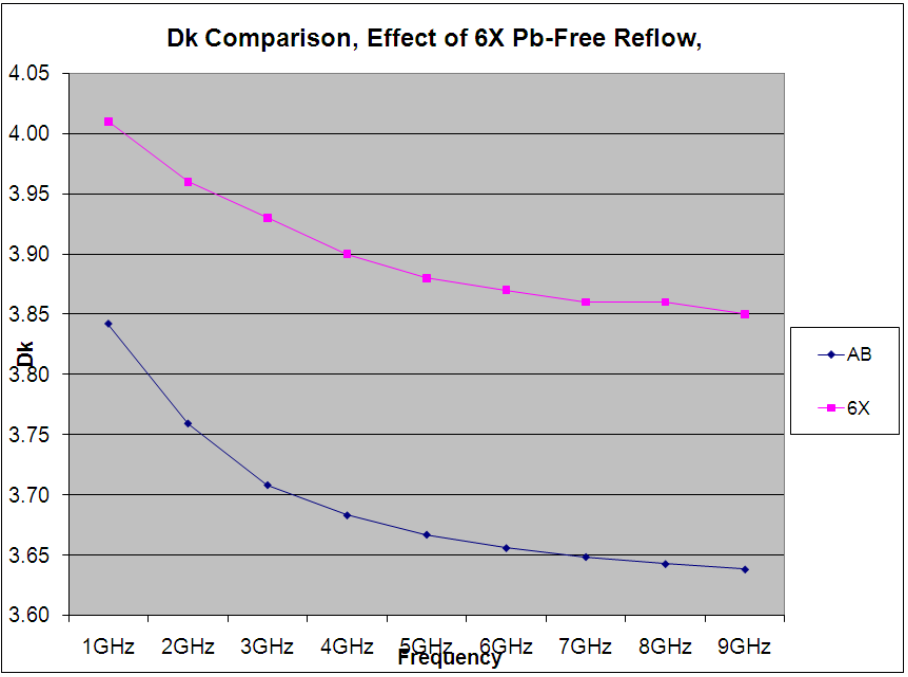
S-Parameter Testing and Dk/Df extraction based on Intel methodology. Typically tested 1-9GHz but can go higher for High Speed materials

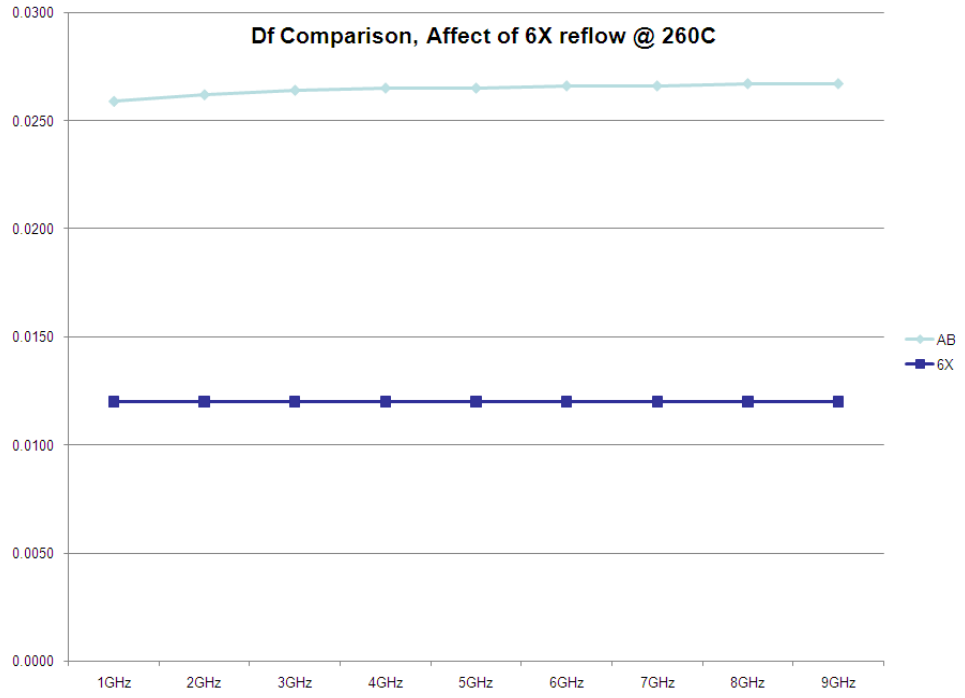




Probe landing

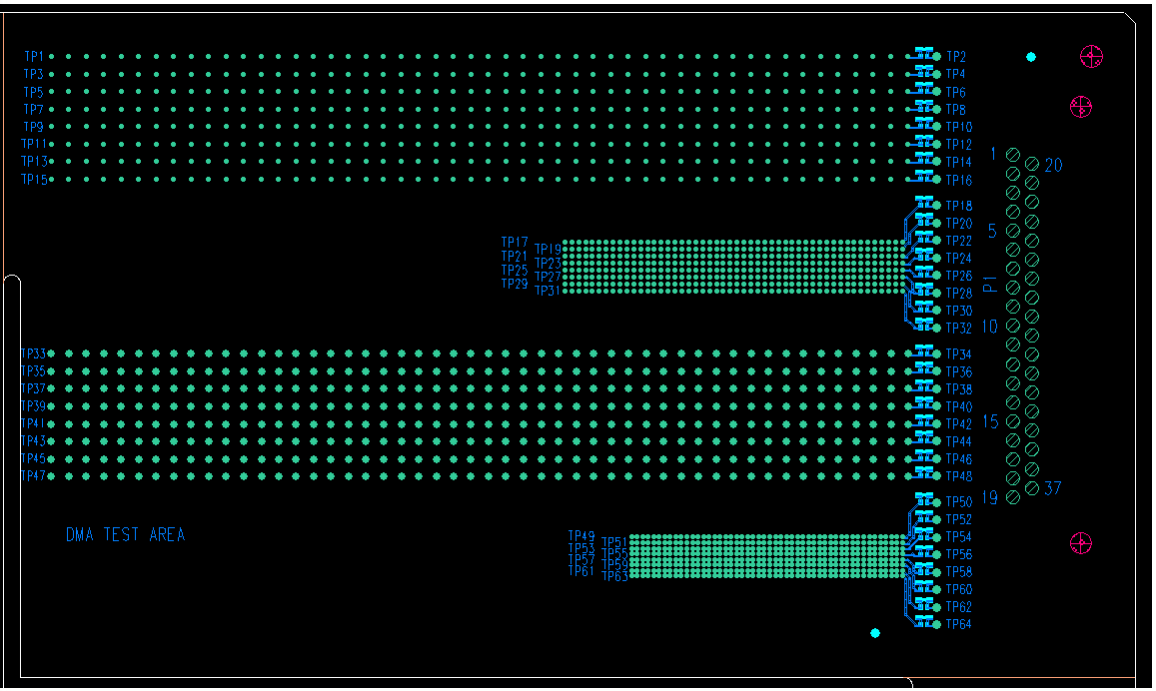
Electrical Effects after Reflow





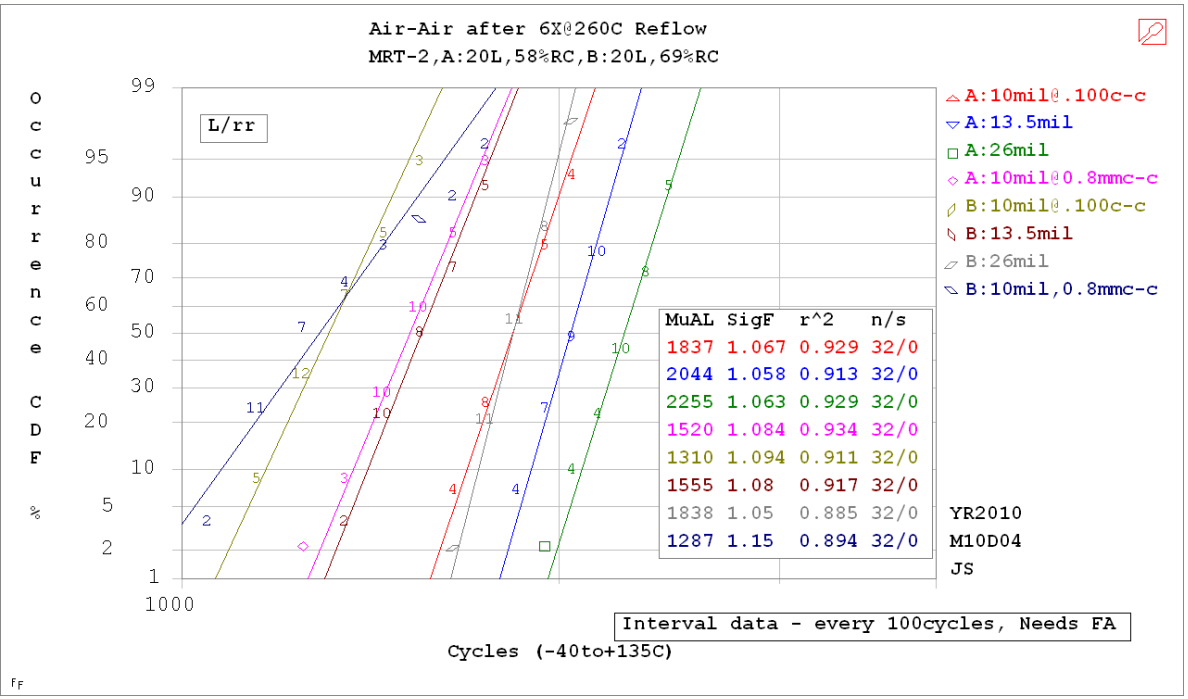
Examples for 2 materials that had significant changes in electrical performance after reflow

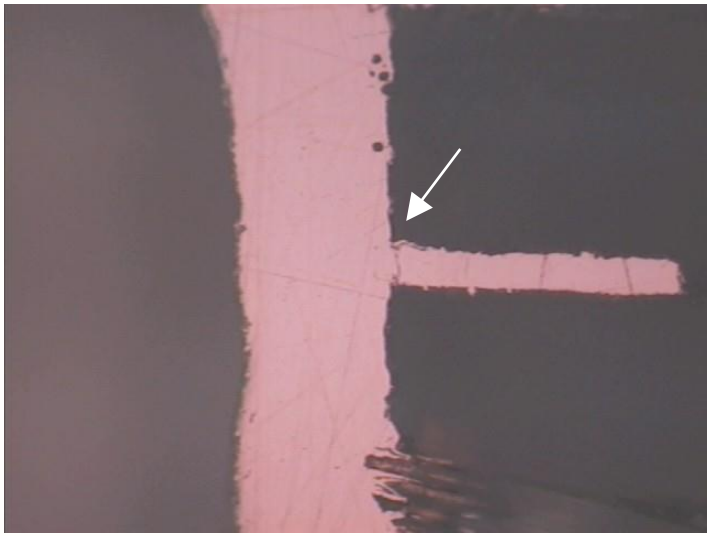
Air-Air Thermal Cycle Section



- .010” drill
  - .100”, 1mm, 0.8mm pitch vias
- .026” drill
  - To identify ICS
- Typically test -40º to +135ºC (or +125ºC depending on Tg)

Evaluating ATC data

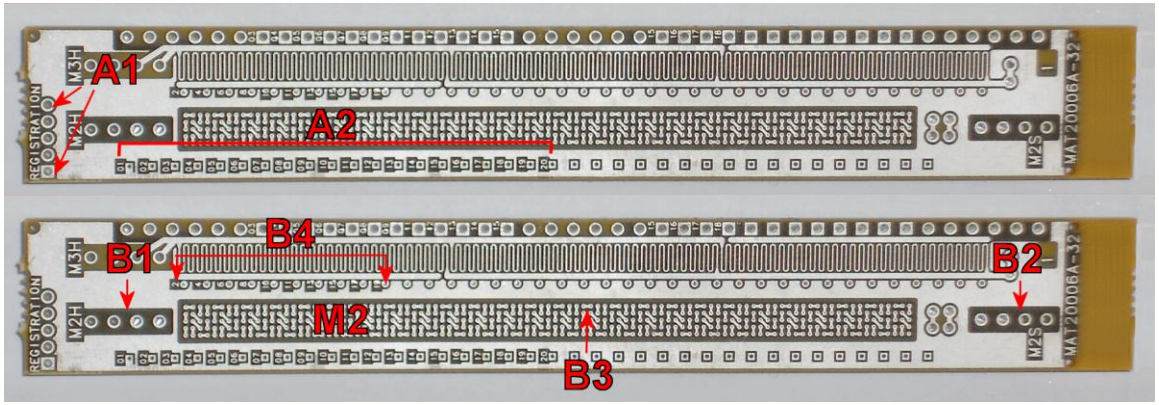




In this example, significant slope change at 0.8mm pitch – suggests material degradation

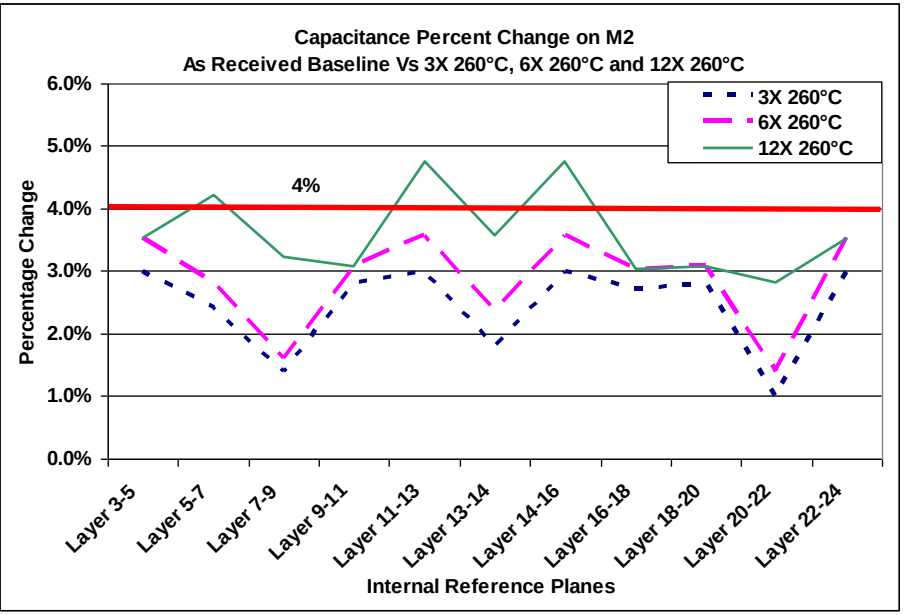
Foil Crack Failure Mode (or ICS if it occurs) will show up in early fails of the larger hole size

IST Coupons

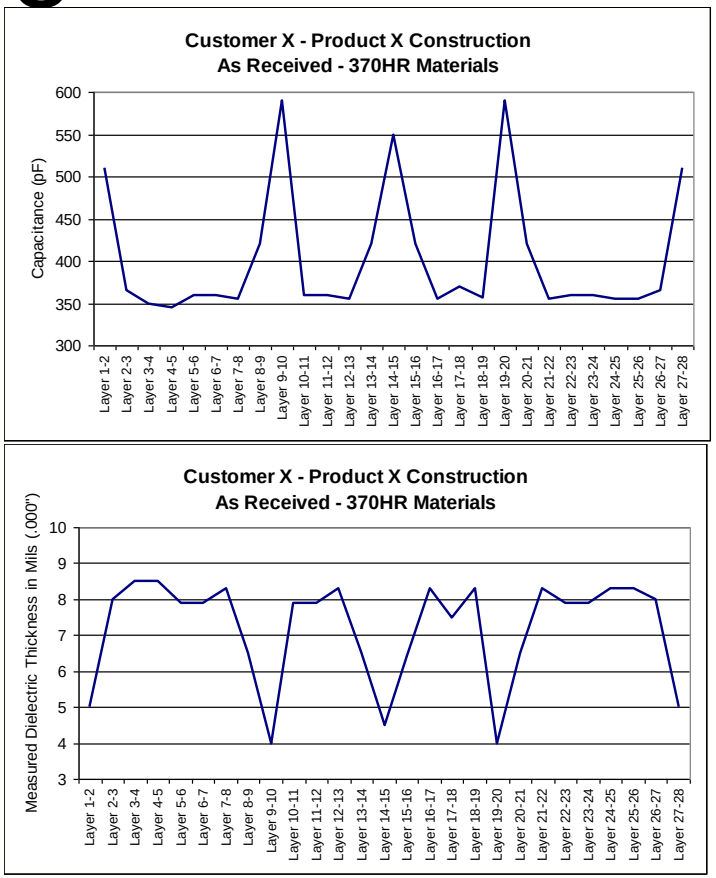


- Construction Confirmation
  - Estimating thickness from Capacitance
- “DELAM” testing – Assembly survivability – change in capacitance
- IST thermal cycling

Evaluating IST

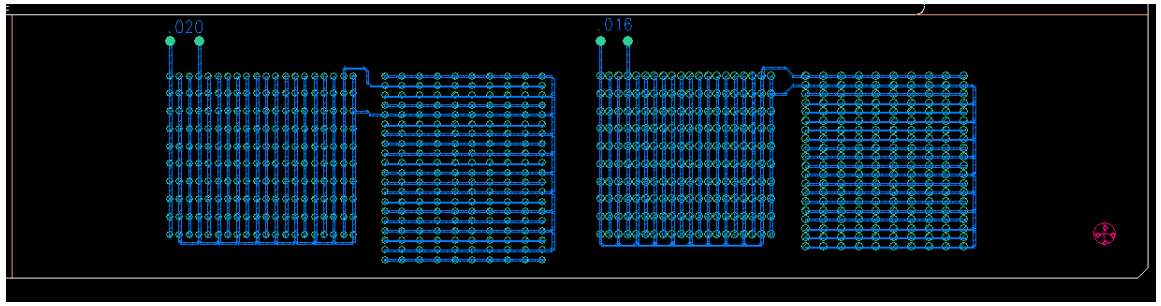


Capacitance Change Showing Material Degradation (DELAM)



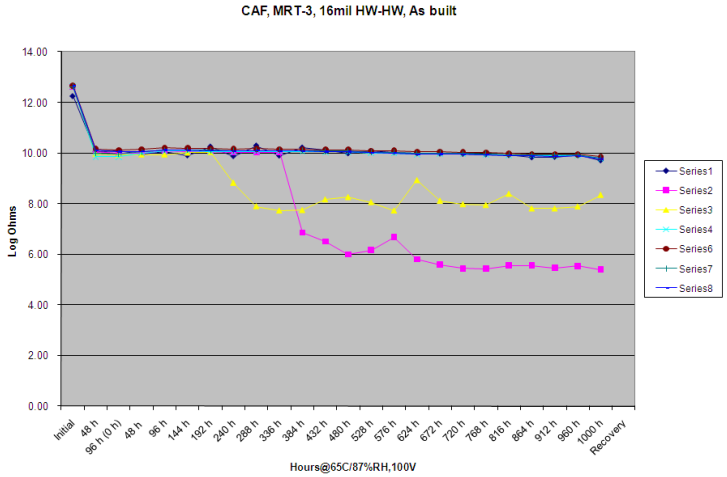
Example of Construction Confirmation – estimating thickness from Capacitance

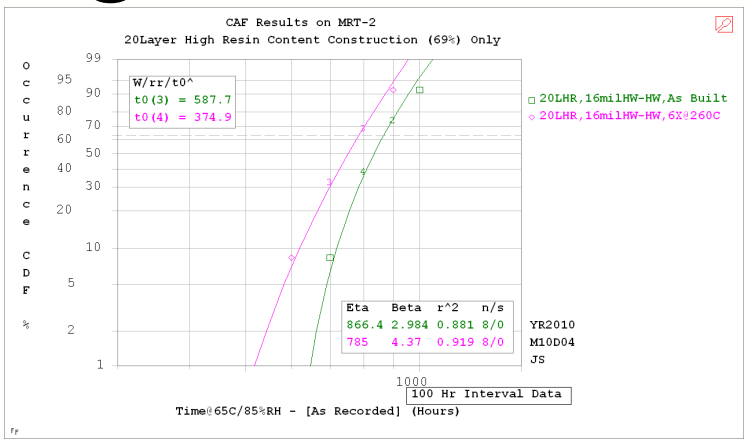
CAF Test Section



- Sample Size – 190X, 190Y
- 20 and 16 mil HW-HW

Evaluating CAF





Typical CAF plot – Fails at 240 Hours

3P Weibull plot showing degradation after 6X reflow

- Degradation of CAF performance after reflow. This typically suggests material degradation with Pb-free reflow.
- Improvement of CAF performance after reflow - sealing effect
- No significant differences between CAF performance before and after reflow
- Differences in CAF performance specifically between stackups. This typically reflects the challenges in wetting certain glass styles. (106 glass effect)

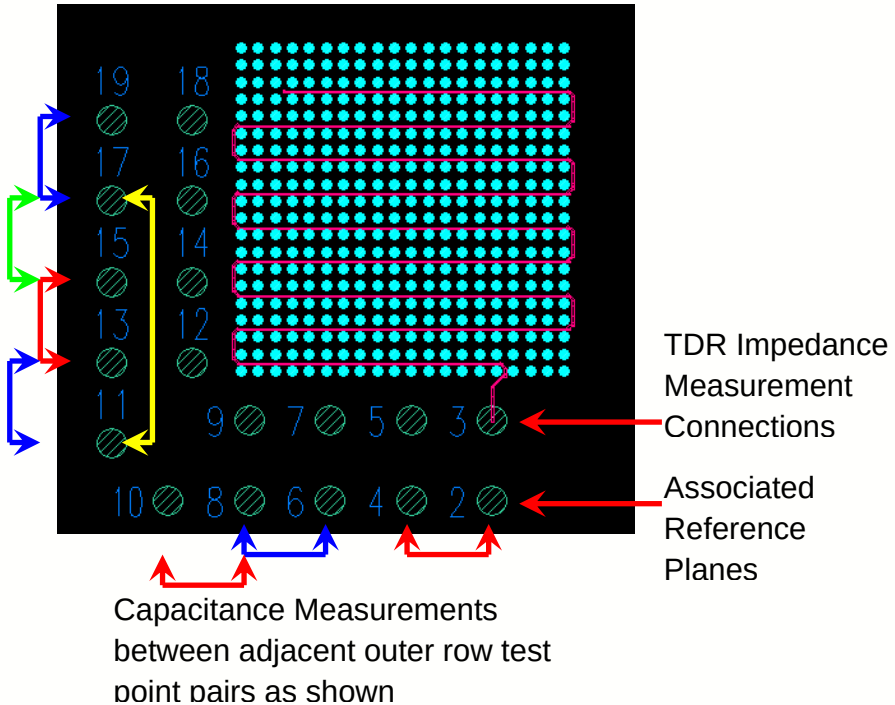
Thermal Analysis on the Multi-layer Board

Thermal analysis, Dynamic Mechanical Analysis (DMA), Thermo-Mechanical Analysis (TMA), Differential Scanning Calorimeter (DSC) shall be done on the finished boards both before and after 6X Pb-free assembly reflow. The following data both before and after reflow should be reported at a minimum:

- Tg (by DSC, TMA) (IPC-TM-650 Method 2.4.24, TMA, DSC)
- Modulus (from DMA) (IPC-TM-650 Test, Method 2.4.24.2)
- CTE Z% (50-260C) (IPC-TM-650 Test, Method 2.4.41)
- CTE <Tg (IPC-TM-650 Test, Method 2.4.41)
- CTE >Tg (IPC-TM-650 Test, Method 2.4.41)
- Td (IPC-TM-650 Method 2.3.40 or IPC-TM-650.2.4.24.6)
- T-260 (IPC-TM-650 Method 2.4.24.1)
- T-288 (IPC-TM-650 Method 2.4.24.1 modified per paragraph 6.1 to 288° C)
- T-300 is also recommended but not mandatory (IPC-TM-650 Method 2.4.24.1 modified per paragraph 6.1 to 300° C)

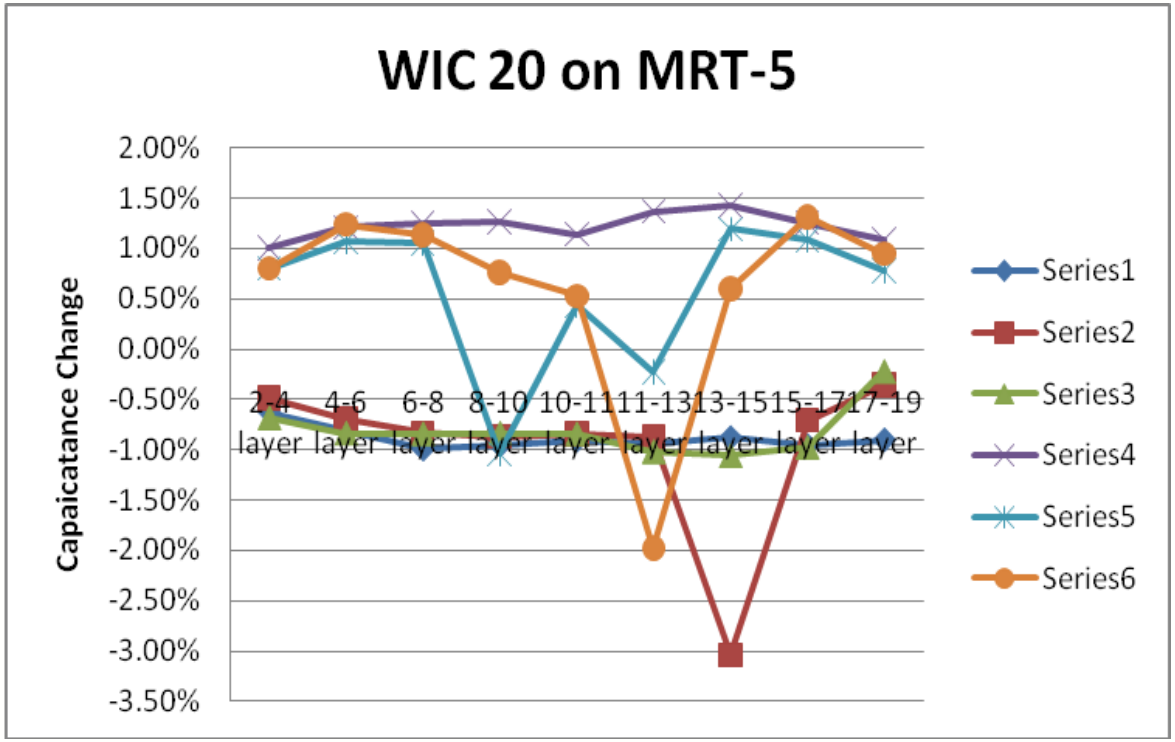
Measure in areas with No Cu, or with Cu

WIC-20 (Water, Impedance Capacitance)



- Evaluate by Capacitance and Impedance material survivability through 6X Assembly Reflow
  - Confirm defects by X-section
- Evaluate Moisture Effects (168Hr, 85C/85RH) before reflow

Evaluating WIC-20



Example plot of capacitance changes after reflow compared to before reflow. In the above example, Series 1,2 and 3 are "dry" (after 24 hours @125° C°) and then reflowed, and Series 4, 5, and 6 are "wet" (after 168 hours of 85° C/85%RH). Series 2, 5 and 6 are clearly indicating internal material damage.

Summary – Part 1

- Materials need testing/qualification for Pb-free in Multilayer applications
- A multilayer board will much better represent actual material use than will bare material samples.
- A standard multilayer printed wiring board for material reliability evaluations has been presented
  - Available to all
  - Offered to the IPC as a standard test vehicle.
  - Having a standard design enables comparisons between materials and not only enables evaluation of the materials, but provides data that can lead to improved material performance.
- The design has already been used on over 80 different materials from virtually every major material supplier worldwide.

Summary- Part 2

- The design not only provides needed data for thermal and electrical characterization of materials, but is specifically designed to understand the Pb-free assembly survivability and reliability of these materials.
  - Sections are designed specifically to support testing and evaluation of
    - PTH- air-to-air thermal cycling and IST
    - Impact of Pb-free reflow on material damage,
    - Product construction verification
    - Consistency of B and C stage materials,
    - Electrical characterization
    - CAF
    - Moisture sensitivity
    - Pad Pull Strength
- The design is set up for 3 standard constructions has sufficient flexibility to cover many different possible constructions.