A Designed Experiment for the Influence of Copper Foils and Oxide Replacements on Impedance, DC Line Resistance and Insertion Loss

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Abstract
With ever increasing data transfer rates, insertion loss has become a limiting factor on today's systems.

Insertion loss can be separated into dielectric loss and copper loss. While dielectric loss can be influenced by choosing a base material with the appropriate dissipation factor, copper loss is more complex.
Copper loss is a function of bulk resistivity, cross sectional area of the conductor, conductor surface roughness as well as frequency. Conductor surface roughness is influenced by the copper foil type (STD, LP, VLP,…) and the oxide replacement process during PCB manufacturing.

To better understand the contributing factors to copper loss, the influence of the copper foil roughness, 'as received' and 'modified by the oxide replacement' was evaluated.

A DOE was performed with three different types of copper foils (RTF, VLP, ultra low profile) and ten different oxide replacement chemistries. Insertion loss as well as impedance and DC line resistance were measured on the various test samples. The results were compared using a statistical ANOVA approach.

The paper describes the performed measurements and will discuss in detail the influence of copper foil, oxide replacement, line width and copper thickness on the key parameters impedance, DC line resistance and insertion loss. An 'analysis of variances process' is used to understand the level to which the contributing factors affect the electrical parameters.
A measurement at two different frequencies is used to demonstrate the varying influence of the independent variables on insertion loss.

Introduction
To support Moore's law, clock rates and transfer rates are increasing all the time. While just a few years ago, controlling the impedance on the blank PCB was sufficient to ensure working products, this is changing rapidly. Initially, bare board customers started to specify DC line resistance to have a simple to measure parameter to control loss. For lower frequencies, this can be an acceptable workaround, but is not sufficient at the higher speeds of today's boards.

After impedance and DC line resistance testing entered the 'mainstream' PCB world, the last couple of years showed various attempts to get higher data rates over copper based transmission lines. The use of lower Dk / Df base materials has increased from the odd computer or infrastructure board to a large percentage of the boards. Backdrilling vias to make them more transparent to the signals is common today. Board designers are influencing the choice of glass styles to reduce the glass weave effect.

In the process of squeezing out higher data rates of the boards, the influence of the roughness of the copper traces is becoming more and more important. On critical boards, the use of smoother copper foils like VLP and H-VLP instead of STD [1] is required by the customer.

On the other hand side, specifying the copper foil roughness of the base materials is only impacting one side of the traces. The second side will be changed by the oxide replacement prior to lamination.

To get a handle on the impact of the base copper foil roughness and the oxide replacement chemistry on the insertion loss, a set of test boards was manufactured. The insertion loss was measured on them and the results were evaluated, using a statistical method, analysis of variances (ANOVA) [2,3,4,5].

Description of Test Equipment and Test Structure
For the measurement of the DC line resistance an Agilent 34401A multimeter in 4-wire configuration was used. To prevent errors in data collection, the resistance values were transferred to a computer via a GPIB connection.

Impedance readings were taken with a Polar Instruments CITS900s4 and handheld probes.

The S-parameters were measured on an Agilent 8510B vector network analyzer with an 8515A S-parameter test set and an 8340B synthesized sweeper (system is capable of measurements up to 26.5GHz) [6].
Similar to the DC line resistance measurements, the system was connected with a computer via GP-IB to allow for automatic system set-up and data transfer.
Probing of the test vehicles was done with GGB Industries Picoprobes (see Figure 1). Calibration was performed at the tip of the probes with an appropriate calibration substrate.

Figure 1 Probing of the Test Vehicle

The test vehicle was constructed on an 8 layer stackup, containing two offset striplines (L2-L3-L4 and L5-L6-L7) and two contact layers. The two inner signal layers hold 14" long single striplines in 5 different line widths from 7.25mil to 8.25mil nominal line width. In addition, each test vehicle contained a small differential impedance test coupon in the border area.
To reduce the effect of dielectric loss on the test results, Isola FR408 was used as a base material. The glass styles and resin contents of the core and prepreg layers were chosen to yield similar thicknesses around 8mils.
The copper on layer 6 was a standard 1oz foil; for layer 3 a customized foil with a 0.2mil higher thickness has been applied. The copper foil on both layers was a reverse treated foil (RTF).
The manufacturing panel contained three identical coupons and a set of 3 panels was produced of each test cell.

The innerlayer cores for all test vehicles were produced on our normal manufacturing equipment. A subsequent split into 10 lots of 3 panels each allowed running the samples over different oxide replacement chemistries.
After oxide replacement, they were relaminated to multilayers and finished on our standard processing lines.

In addition to the 10 oxide replacement variations in combination with RTF foil, two additional sets of boards were produced with a lower roughness copper foil and run over the reference oxide replacement chemistry.

A complete list of investigated oxide replacement chemistries and copper foils is given in Figure 2.

- MacDermid Multibond 100 (primary site) + RTF foil
- MacDermid Multibond 100 (alternative site) + RTF foil
- MacDermid Multibond LE + RTF foil
- MacDermid Multibond HP + RTF foil
- no oxide replacement + RTF foil
- reduced black oxide + RTF foil
- Enthone Alpha Prep + RTF foil
- OMG Cobra Bond + RTF foil
- MecEtch Bond CZ-8100-R/M + RTF foil
- Atotech Secure HFz + RTF foil
- MacDermid Multibond 100 (primary site) + VLP foil
- MacDermid Multibond 100 (primary site) + ultra low profile foil

Figure 2 Oxide Replacements and Cu Foils tested

Measurement of Impedance and DC Line Resistance

As a first step, all test coupons were subjected to impedance and DC line resistance testing. Both, the border impedance coupon and the insertion loss test structures were measured.

After collecting all the data, the results were evaluated, using an Analysis of Variances (ANOVA) approach to see the influence of the various independent variables.

For impedance testing of the border impedance coupons, only small variations were detected over the 3 panels of each test cell, which indicates a stable manufacturing process.

Comparing the 3 images on each panel showed much lower differential impedance values on image #1 compared to the other two images. This is easily explained by the fact that the differential impedance coupon of image #1 was close to the edge of the manufacturing panel, where the other two images had their coupon more central on the panel (see Figure 3). Since it is very typical, that the prepreg thickness decreases close to the panel edge, the reduction in differential impedance was no surprise.

Figure 3 Location of Differential Impedance Coupon

Since layer 3 was using a higher copper weight compared to layer 6, the change of impedance over the layers was also expected, as was the fact, that the oxide replacement chemistry had a significant impact on the impedance readings (see Figure 4).

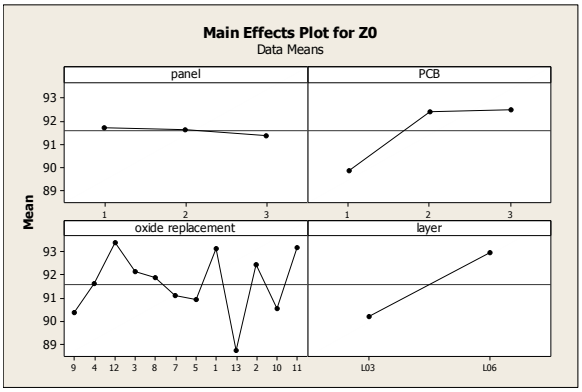

Figure 4 Main Effect Plot for Differential Impedance (Edge Coupon)

The evaluation of DC line resistance in the border differential impedance coupon showed very similar characteristics with the exception that, naturally, the change in dielectric thickness / the test coupon location on the manufacturing panel had no impact (see Figure 5).

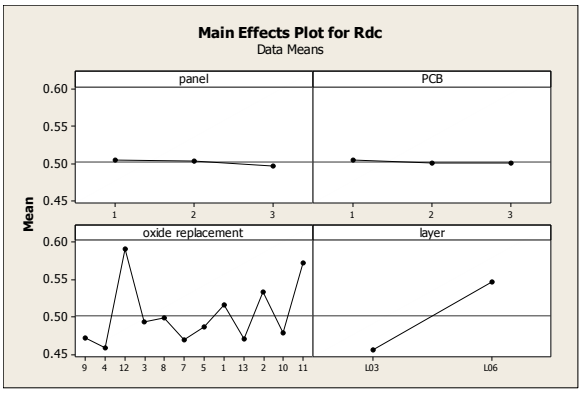

Figure 5 Main Effect Plot for DC Line Resistance (Edge Coupon)

The second type of structures tested were the transmission lines used for insertion loss testing also. Again, only small changes were detected within the set of 3 panels, indicating a stable process.
The location of the coupon on the panel showed a significant influence, with the highest impedance values measured for the center coupon. Since the prepreg thickness is usually higher near the center of the panel, this is easily explained.
Again, the thicker copper on layer 3 caused the impedance to be lower than on layer 6.
Since the transmission lines for insertion loss testing were put on the coupon with 5 different line widths, the main effect plot shows this additional independent variable. The expected correlation of increasing line width and decreasing single ended impedance was confirmed.
Finally, the choice of oxide replacement influences the impedance values significantly (see Figure 6).

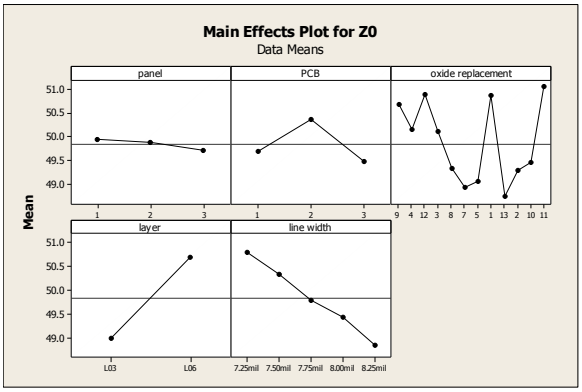

Figure 6 Main Effect Plot for Single Ended Impedance (Loss Coupon)

Evaluating the DC line resistance in the loss coupon produced expected results. The panel and the PCB number had only a minor effect. The thinner copper on layer 6 resulted in higher DC line resistance values than on layer 3 and the resistance decreases with increasing line width. Again, oxide replacement chemistry showed a major impact (see Figure 7).

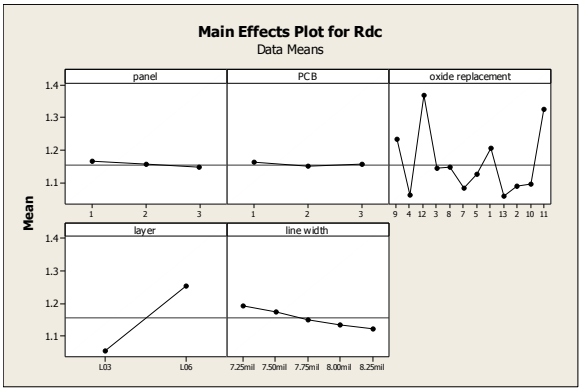

Figure 7 Main Effect Plot for DC Line Resistance (Loss Coupon)

Measurement of Insertion Loss

After measurement of single ended and differential impedance and DC line resistance, the coupons were tested for single ended insertion loss on the vector network analyzer. A full 2-port SOLT calibration was performed at the tip of the microprobes. The 14" long transmission lines were then probed and the S-parameters over the chosen frequency range were recorded and transferred to the computer for post processing.

The first check was plotting the S21 curves for all 5 line widths, two layers and 3 panels into one chart each for all test cells. By doing this, measurements with unusual behavior would be found very easily.

The comparison showed the S21 values for all 5 line widths and on all 3 panels to have only low variance for layer 3, and similar small variance for layer 6. However, the series of curves of layer 3 and of layer 6 differed significantly (see Figure 8).

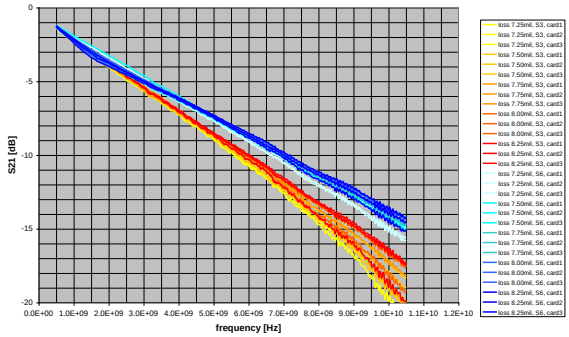

Figure 8 Example of S21 Curves for one Test Cell

To better show the difference between the two layers, an average over the 3 panels and the 5 line widths was calculated, and the chart re-plotted (see Figure 9).

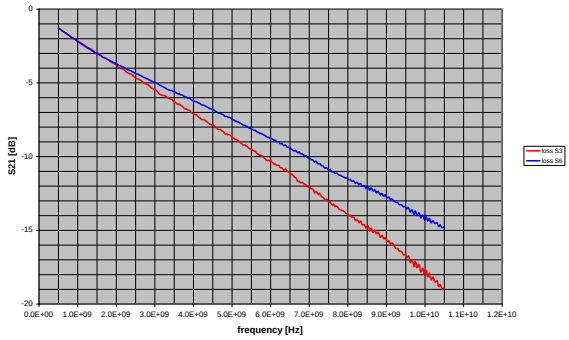

Figure 9 Comparison of S21 between L3 and L6

To quantify the impact of the oxide replacement chemistry on the insertion loss, S21 was plotted over frequency for all test cells. Each trace was the average over the 3 panels in each set. Figure 10 shows the spread for layer 3 and the center line width. As shown in the chart, the difference in insertion loss between the oxide replacements exceeds 1.8dB at a frequency of 5GHz already.

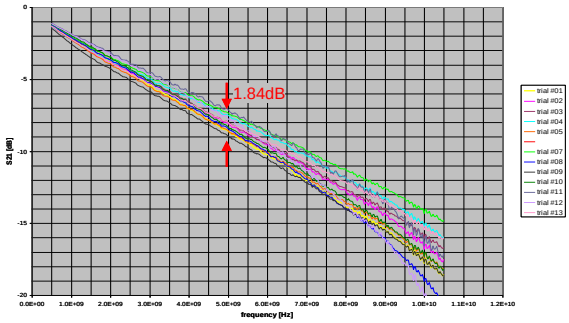

Figure 10 Spread of S21 Values

To investigate the influence of the various independent variables, an analysis of variance was performed at two distinct frequencies, one in the lower/medium frequency range (750MHz) and one in the higher frequency range (5GHz).
The main effect plot at 750MHz shows small variations between the 3 panels. Increasing the line width is reducing the insertion loss, however the effect is very minor.
The increase of insertion loss for the thicker copper on layer 3 was not expected, although the difference is very small. But since the thicker copper is having a higher roughness than the standard 1oz copper, the skin effect is negating any positive effect of the larger cross sectional area.
Most important, the choice of oxide replacement is the biggest contributor to the variance in insertion loss (see Figure 11).

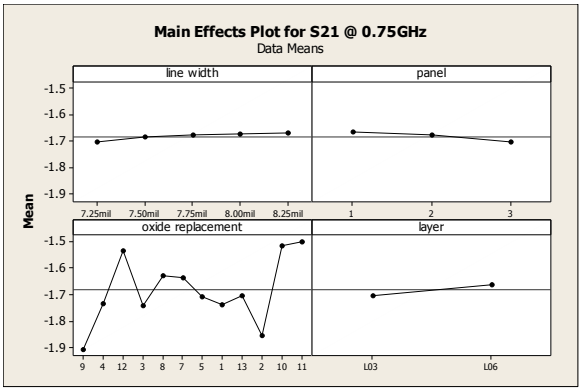

Figure 11 Main Effect Plot for S21 at 750MHz

The evaluation at the higher frequency of 5GHz confirmed the same basic effects. Line width and panel number do not play a prominent role in affecting S21. But the influence of the copper thickness / layer is increasing significantly. The standard 1oz copper on layer 6 is having a much smaller insertion loss compared to the thicker copper on layer 3. Since the copper roughness will be larger on the thicker copper, the main cause here is skin effect. The increase of the frequency from below 1GHz to 5GHz is sufficient to make the copper thickness one of the two main contributors.
The second main contributing variable for insertion loss is the oxide replacement. A standard oxide replacement, like the one with the label '1' is showing poor insertion loss results.
On the other hand, the oxide replacements with a low etch rate or even 'non-etching adhesion promoters', as well as the use of a less rough base copper foil in combination with the standard oxide replacement (numbers 7, 4, 11) is resulting in a significant reduction of the insertion loss (see Figure 12).

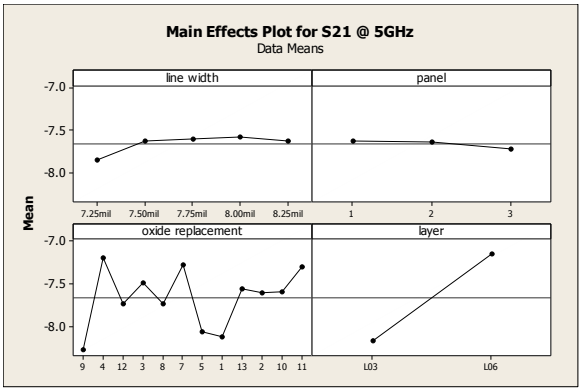

Figure 12 Main Effect Plot for S21 at 5GHz

Looking at the numerical output from the ANOVA evaluation, at 750MHz, there is only one significant factor – the oxide replacement, which accounts for 66% of the variation (see Figure 13).
Going to the higher frequency of 5GHz is changing this picture somewhat. The oxide replacement is still a significant factor, accounting for 21% of the variation. But it addition, the layer (i.e. the copper thickness) is also a significant factor and accounts for 51% of the variation (see Figure 14).

```
• Analysis of Variance for S21 @ 0.75GHz, using Adjusted SS for Tests

• Source              DF   Seq SS   Adj SS   Adj MS      F      P
• line width           4  0.05282  0.05282  0.01321   1.86  0.117
• panel                2  0.08512  0.08512  0.04256   5.99  0.003
• oxide replacement   11  5.28071  5.28071  0.48006  67.55  0.000
• layer                1  0.15498  0.15498  0.15498  21.81  0.000
• Error              341  2.42352  2.42352  0.00711
• Total              359  7.99715

• S = 0.0843036   R-Sq = 69.70%   R-Sq(adj) = 68.10%
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Figure 13 Numerical ANOVA Results at 750MHz

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• Analysis of Variance for S21 @ 5GHz, using Adjusted SS for Tests

• Source              DF    Seq SS   Adj SS   Adj MS       F      P
• line width           4    3.2201   3.2201   0.8050    6.02  0.000
• panel                2    0.6133   0.6133   0.3067    2.29  0.103
• oxide replacement   11   38.6102  38.6102   3.5100   26.23  0.000
• layer                1   92.5717  92.5717  92.5717  691.77  0.000
• Error              341   45.6319  45.6319   0.1338
• Total              359  180.6473

• S = 0.365811   R-Sq = 74.74%   R-Sq(adj) = 73.41%
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Figure 14 Numerical ANOVA Results at 5GHz

Comparing a few of the better performing oxide replacements, we could get an improvement of up to 1.19dB in case the copper thickness was kept at the special thicker value. If in addition the copper foil was changed back to a standard 1oz foil, the improvement could be up to 1.96dB.
Since the oxide replacement chemistry can not be changed easily for small production volumes, we also checked on what would happen, if we changed from a RTF foil to a 1oz VLP foil, but still used the standard oxide replacement. The improvement by this was up to 1.45dB (see Table 1).

Table 1 – Improvement of Insertion Loss

Oxide replacement	S21 @ 5GHz 1.14oz copper	S21 @ 5GHz 1oz copper
RTF + standard OR	8.74dB [ref]	7.48dB [1.26dB]
RTF + NEAP	7.61dB [1.13dB]	6.78dB [1.96dB]
RTF + low etch OR	7.55dB [1.19dB]	7.00dB [1.74dB]
VLP + standard OR	- - -	7.29dB [1.45dB]

Verification of Geometrical Attributes
After the electrical measurements, cross sections were taken out of boards from each test cell to verify, that the structural dimensions of all boards were within the defined range.
It was ensured, that the dielectric thicknesses showed a normal distribution (see Figure 15) and copper thickness for both, the thicker version on layer 3 as well as for the standard 1oz version on layer 6 were within the typical range (see Figure 16).
Finally, it was controlled that the line widths did not show any unusual behavior and actual width followed closely the nominal width (see Figure 17).

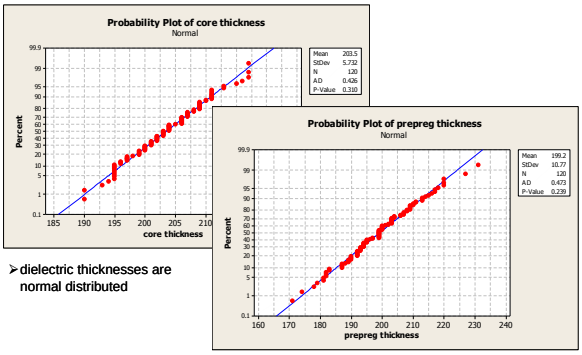

Figure 15 Distribution of Core and Prepreg Thickness

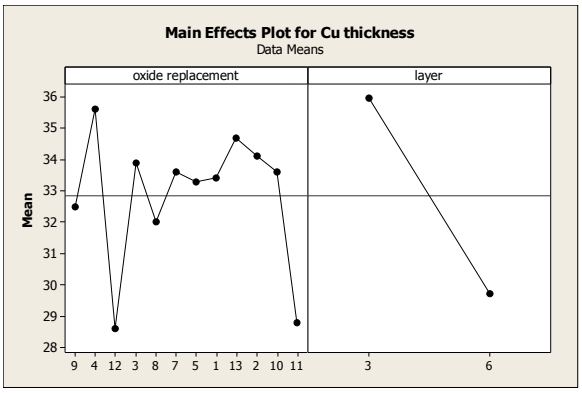

Figure 16 Copper Thickness Values

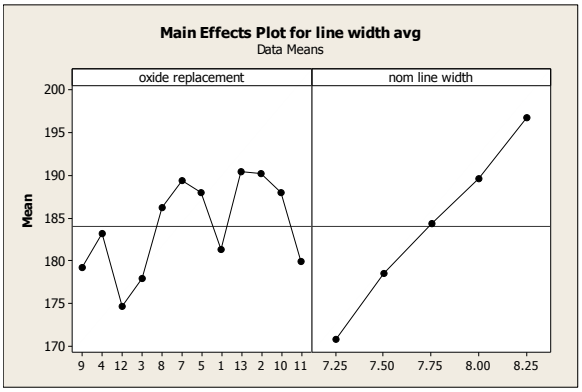

Figure 17 Line Width Values

Optical Appearance of the Copper Foil

During insertion loss testing, it was noticed, that the thicker copper foil on layer 3 showed a higher loss than the thinner copper foil on layer 6. Since the signal traces on layer 3 had a higher cross sectional area than the traces on layer 6, this was somewhat surprising at first. However, considering the manufacturing process of copper foils, the roughness will typically increase with the higher nominal thickness, since this will be achieved by using a higher current density during the electroplating process.

To verify the higher roughness, SEM pictures were taken of both, the nonstandard and the 1oz copper foils. This was done 'as received' and after the complete innerlayer process, including the oxide replacement.

Figure 18 compares the 'as received' SEM pictures, Figure 19 is shows the same foils after oxide replacement.

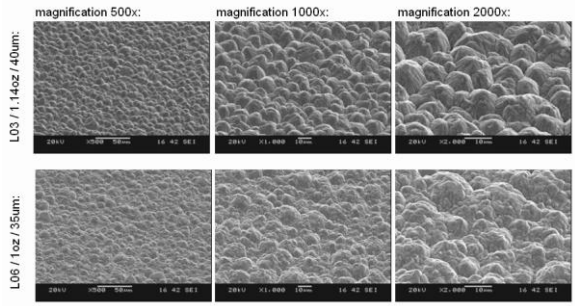

Figure 18 SEM of Copper Surface 'As Received'

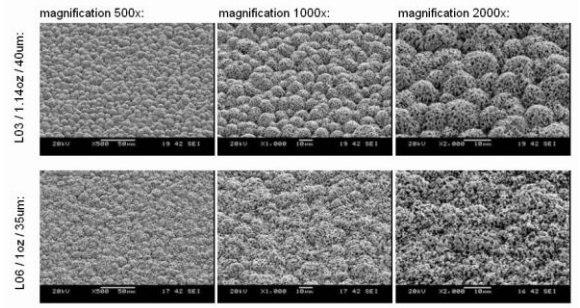

Figure 19 SEM of Copper Surface 'after Oxide Replacement'

The surface pictures clearly show different appearances of the copper. Cross sections were made to find out, if the etch attack also show variances. Figure 20 compares two samples that clearly show a strong metal removal along the grain boundaries and one sample produced with an oxide replacement with significantly less etch attack.

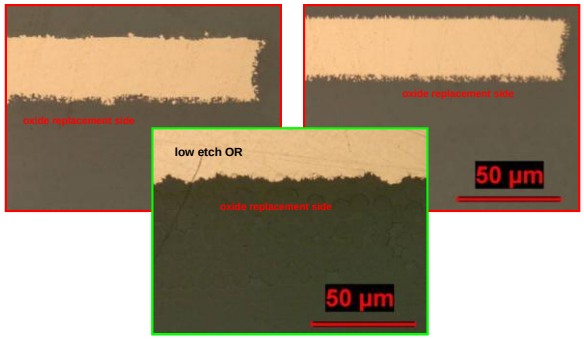

Figure 20 Cross Sections of Corrosion

Reliability

From a signal integrity point of view, the use of oxide replacements with a high etch rate seem a bad choice at first. However, these chemistries were designed to improve the adhesion of the resin to the copper. So, any reduction in etch rate or even more the use of a non-etching adhesion promoter is causing concerns regarding the reliability of the resulting product.

In order to understand if the lower roughness oxide alternatives are feasible, samples were stressed with both solder shock and repeated reflow testing. Solder shock was performed 6 times at 288 deg C., and reflow was repeated six times with a standard eutectic reflow profile with 230 deg C. peak temperature.

During the thermal stress testing, samples of only two test cells showed delaminations. One was the control cell with no oxide replacement at all.

Summary

The conducted testing clearly showed that the choice of oxide replacement chemistry is affecting insertion loss characteristics to a significant amount. Traditional oxide replacements with a higher etch rate performed worse, where lower etch rate chemistries and non-etching adhesion promoters showed significant improvements.

It was shown, that in case of a STD or RTF foil used, the change to a VLP foil, while keeping the oxide replacement, was nearly as efficient.

Furthermore it was demonstrated, that increasing copper foil thickness to reduce low frequency resistance is counter productive at higher frequencies and causes significant deterioration of insertion loss.

References

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Influence of Copper Foils and Oxide Replacements on Insertion Loss

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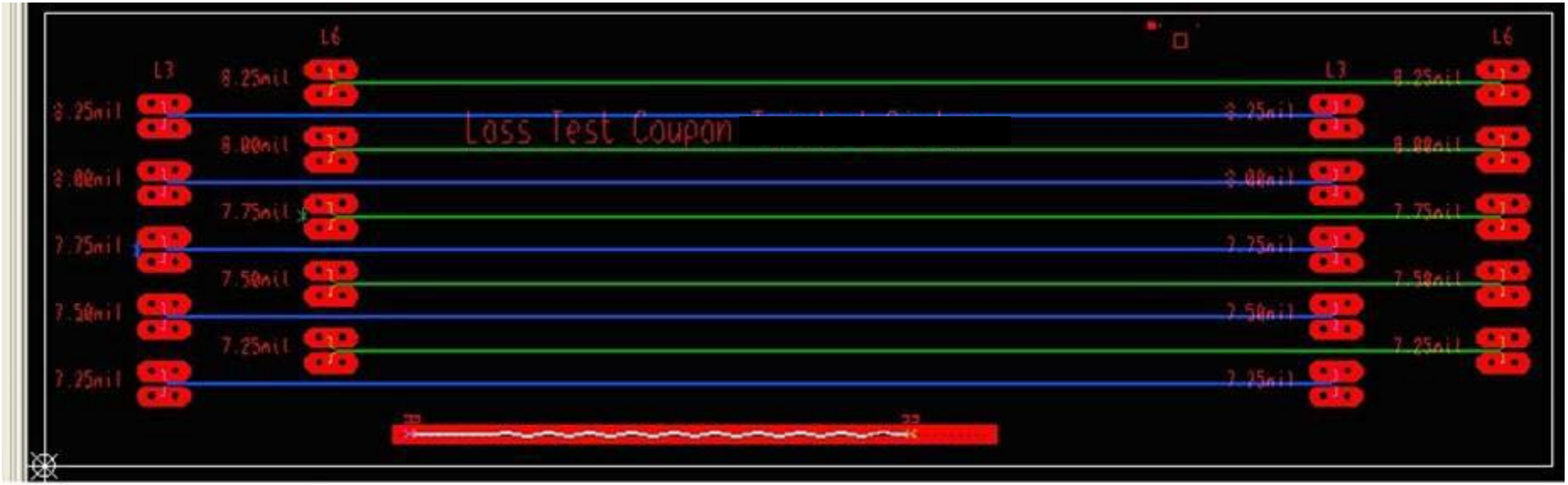
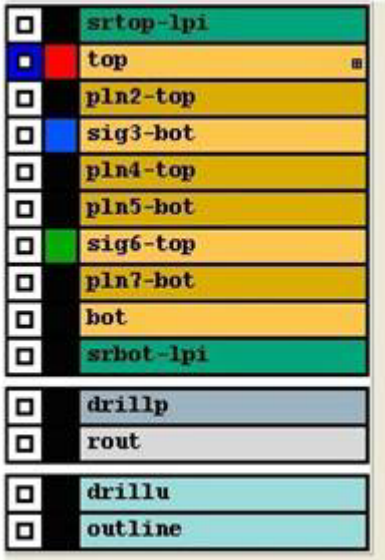
test design – single image





measured coupons

- coupon has 5 different line widths (7.25 - 8.25mil)
- coupon is routed on two layers (L3 – 40um Cu and L6 – 35um Cu)
- coupon is 3x on each panel
- 3 panels produced per test cell
- 12 test cells (different oxide replacements, different copper treatment styles)
- measured for insertion loss, impedance and DC line resistance

test design – panel design

stackup

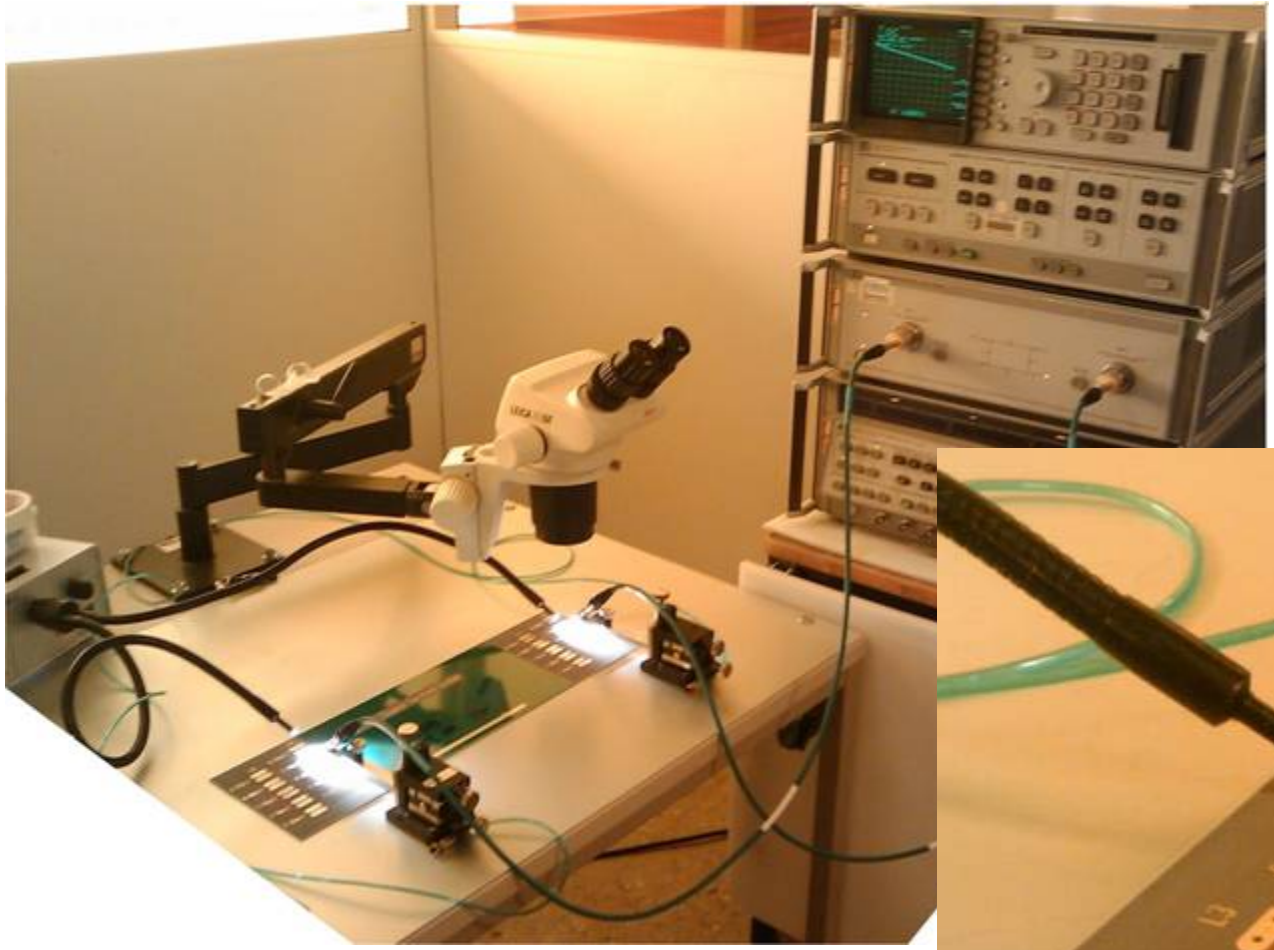
Layer type	#	Layer description	For dielectric layers: Material selection, Multek Code For copper layers: copper utilization in %	Via Structure	Multek Material code	glass style	resin content [%]	dielectric constant @ 5 GHz	Thickness nominal thickness. [um]	Thickness after lamination [um]	Thickness after lamination [mil]
Air											
soldermask									10	10	0.4
Top	1	Primary Side Traces			17um foil, thinned to 7um + plated copper				105	105	4.1
prepreg			QI 5.52mil (2116)		P-QI001	2116	56%	3.46	140	134	5.3
pln	2		85%		1.14				**35**	39	1.5
core			QI 8mil 40/40 (2x2116)		**C-QI900**	**2x2116**		**3.71**	**203**	**203**	**8.0**
sig	3		15%		1.14				**35**	39	1.5
prepreg			QI 9.43mil (2116+2113)		P-QI001+P-QI005	2116+2113	57%	3.45	239	191	7.5
pln	4		85%		1				**31**	35	1.4
core			QI 8mil 1/1 (2x2116)		**C-QI036**	**2x2116**		**3.71**	**203**	**203**	**8.0**
pln	5		85%		1				**31**	35	1.4
prepreg			QI 9.43mil (2116+2113)		P-QI001+P-QI005	2116+2113	57%	3.45	239	194	7.7
sig	6		15%		1				**31**	35	1.4
core			QI 8mil 1/1 (2x2116)		**C-QI036**	**2x2116**		**3.71**	**203**	**203**	**8.0**
pln	7		85%		1				**31**	35	1.4
prepreg			QI 5.52mil (2116)		P-QI001	2116	56%	3.46	140	135	5.3
Bot	8	Secondary Side Traces			17um foil, thinned to 7um + plated copper				105	105	4.1
soldermask									10	10	0.4
Air											

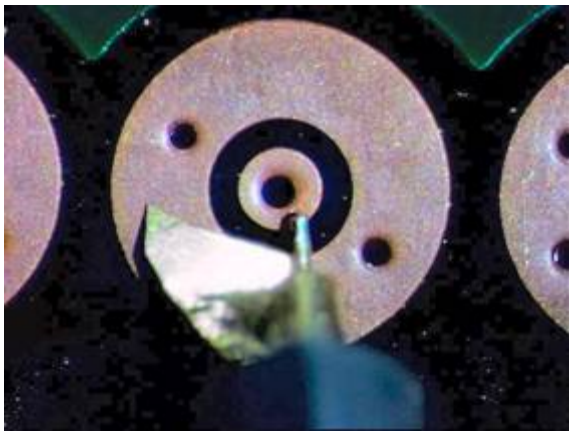
- used special ~40um foil on layer 3 and standard 1oz foil on layer 6

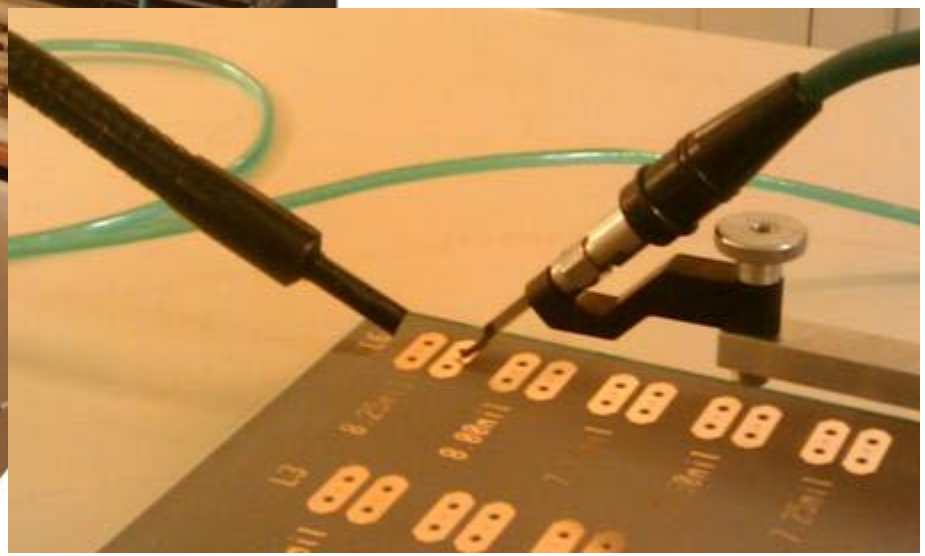
measurement system

- Agilent 8510B vector network analyzer
- Agilent 8515A S-parameter test set
- Agilent 8340B synthesized sweeper
- Agilent 85052B calibration kit
- Rosenberger Microcoax Utiflex cables
- Quater Research XYZ500MIS probe positioner
- GGB Industries 40A-SG-1000-DS Picoprobe®
- GGB Industries CS-11 calibration substrate

probing detail







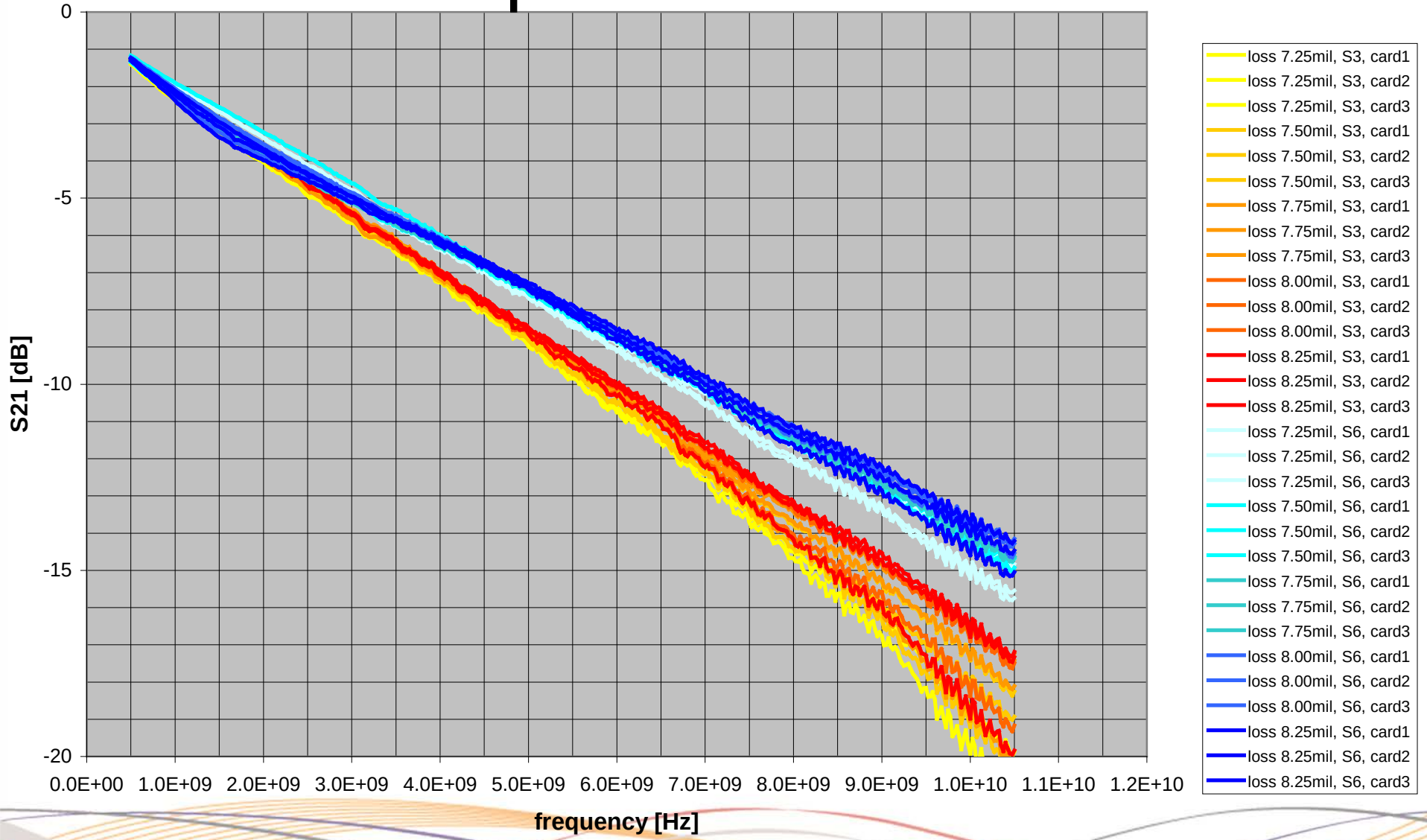
measurement procedure

- full two port calibration of VNA
  - warm up of 2h
  - calibration with CS-11 calibration substrate at the tip of the Picoprobes
- measurement of S-parameters
  - probing with Picoprobes
  - programmed measurement / measurement controlled via PC
  - transfer S-parameters PC hard disc drive
- all further data processing in statistic software
  - charts of various parameters
  - ANOVA evaluation to find the ‘vital few’ parameters

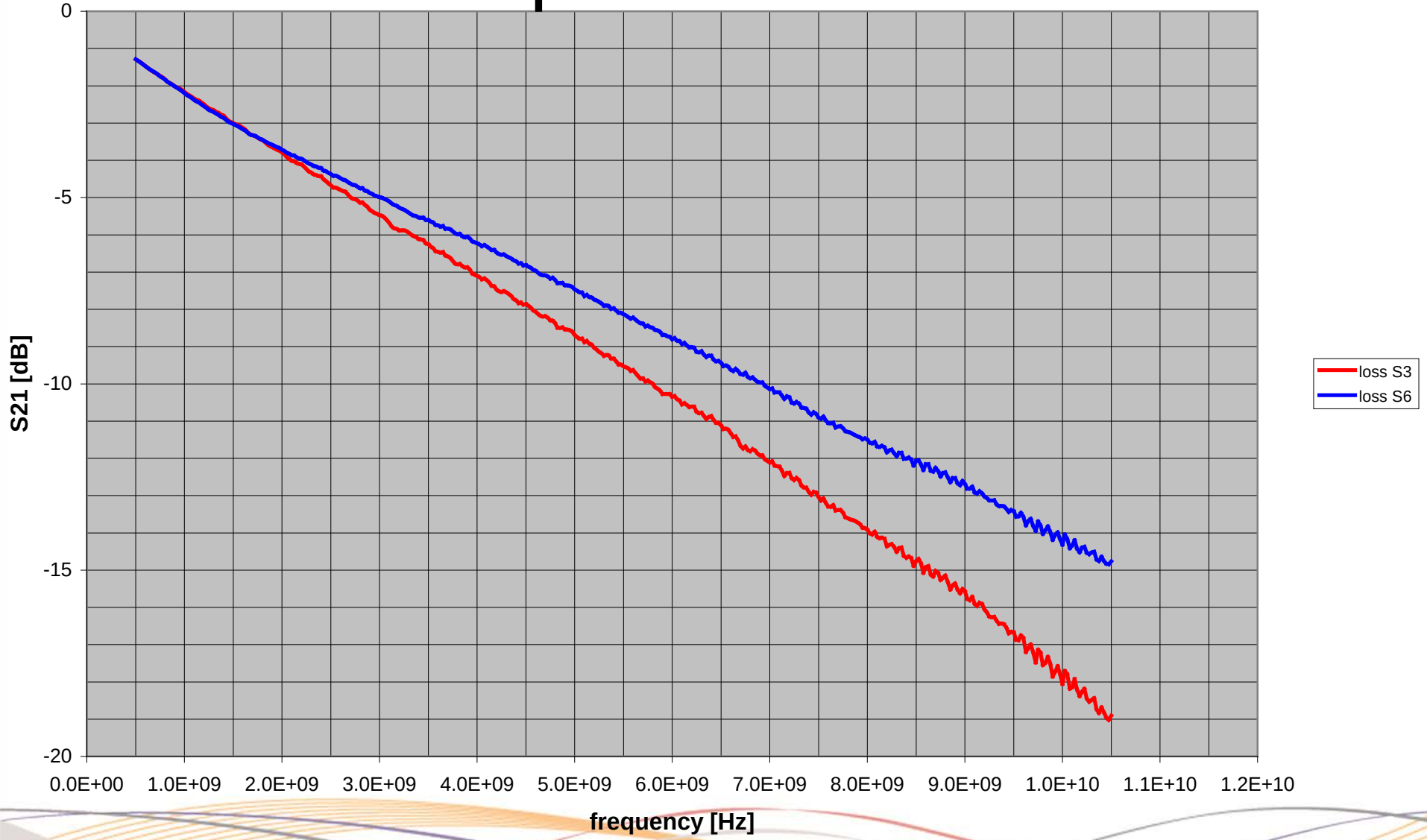
overview tested oxide replacements / foil types

- MacDermid Multibond 100 (primary site) + RTF foil
- MacDermid Multibond 100 (alternative site) + RTF foil
- MacDermid Multibond LE + RTF foil
- MacDermid Multibond HP + RTF foil
- no oxide replacement + RTF foil
- reduced black oxide + RTF foil
- Enthone Alpha Prep + RTF foil
- OMG Cobra Bond + RTF foil
- MecEtch Bond CZ-8100-R/M + RTF foil
- Atotech Secure HFz + RTF foil
- MacDermid Multibond 100 (primary site) + VLP foil
- MacDermid Multibond 100 (primary site) + ultra low profile foil

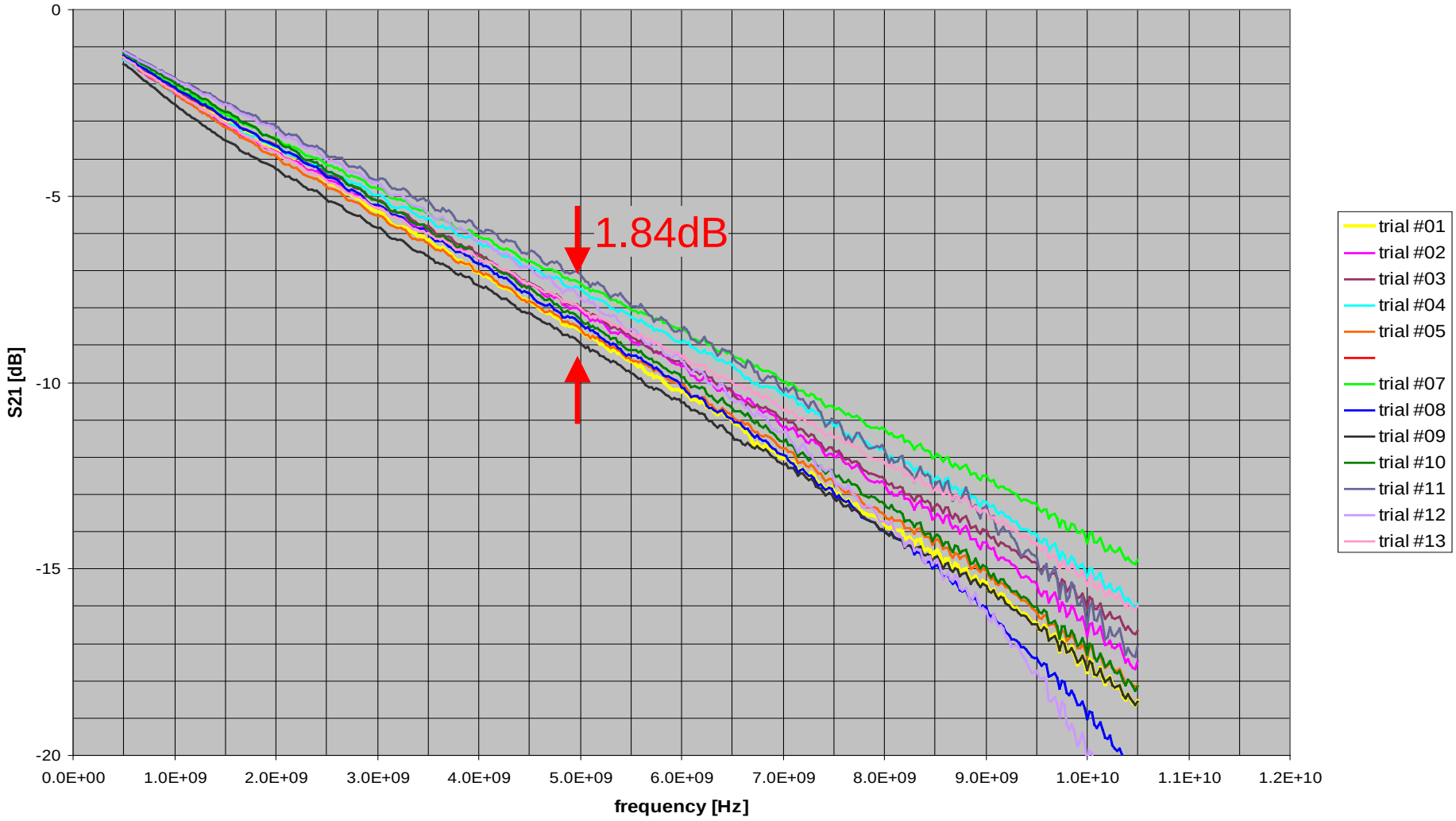
example of S21 curves



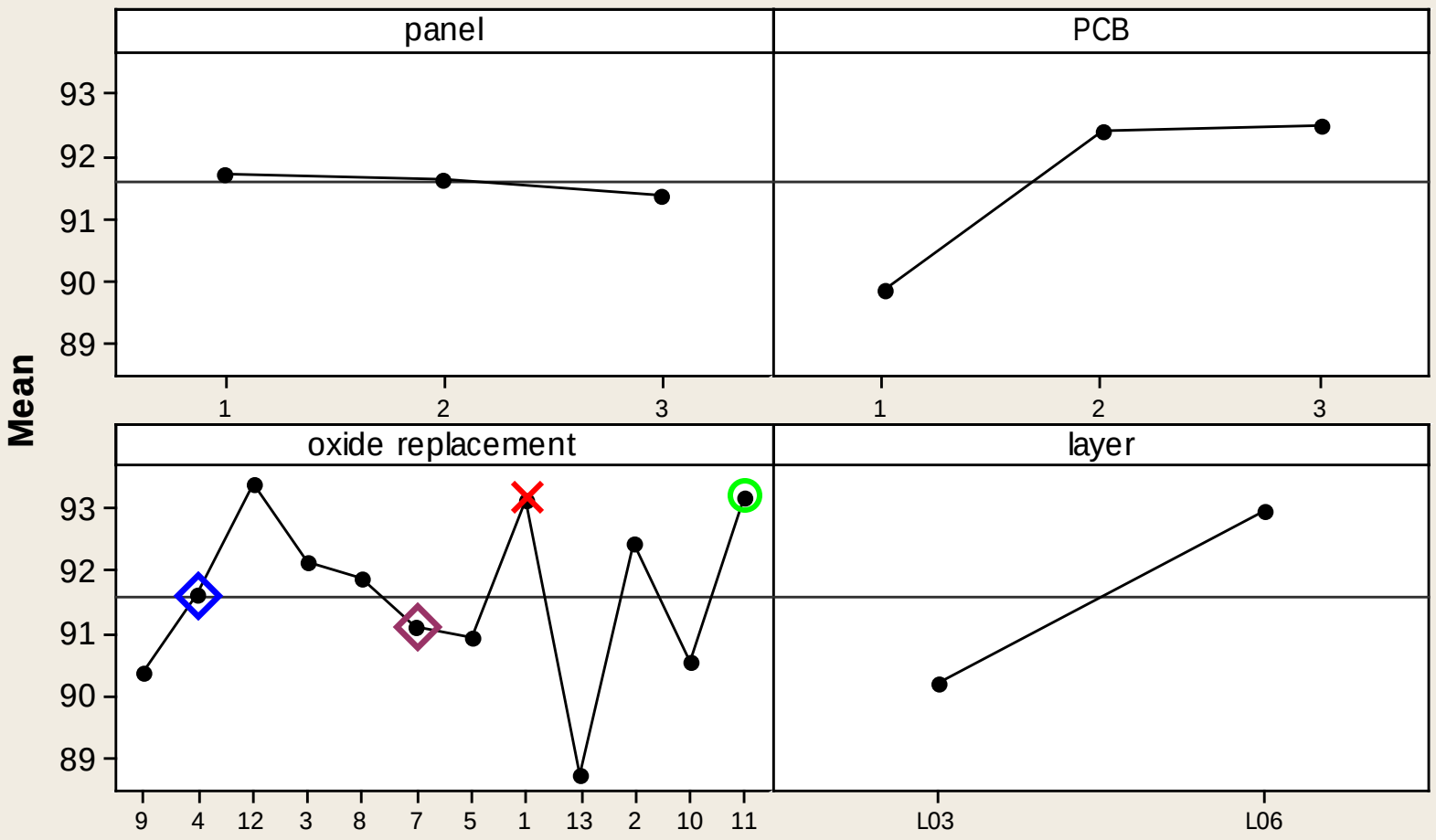
comparison S3 /S6



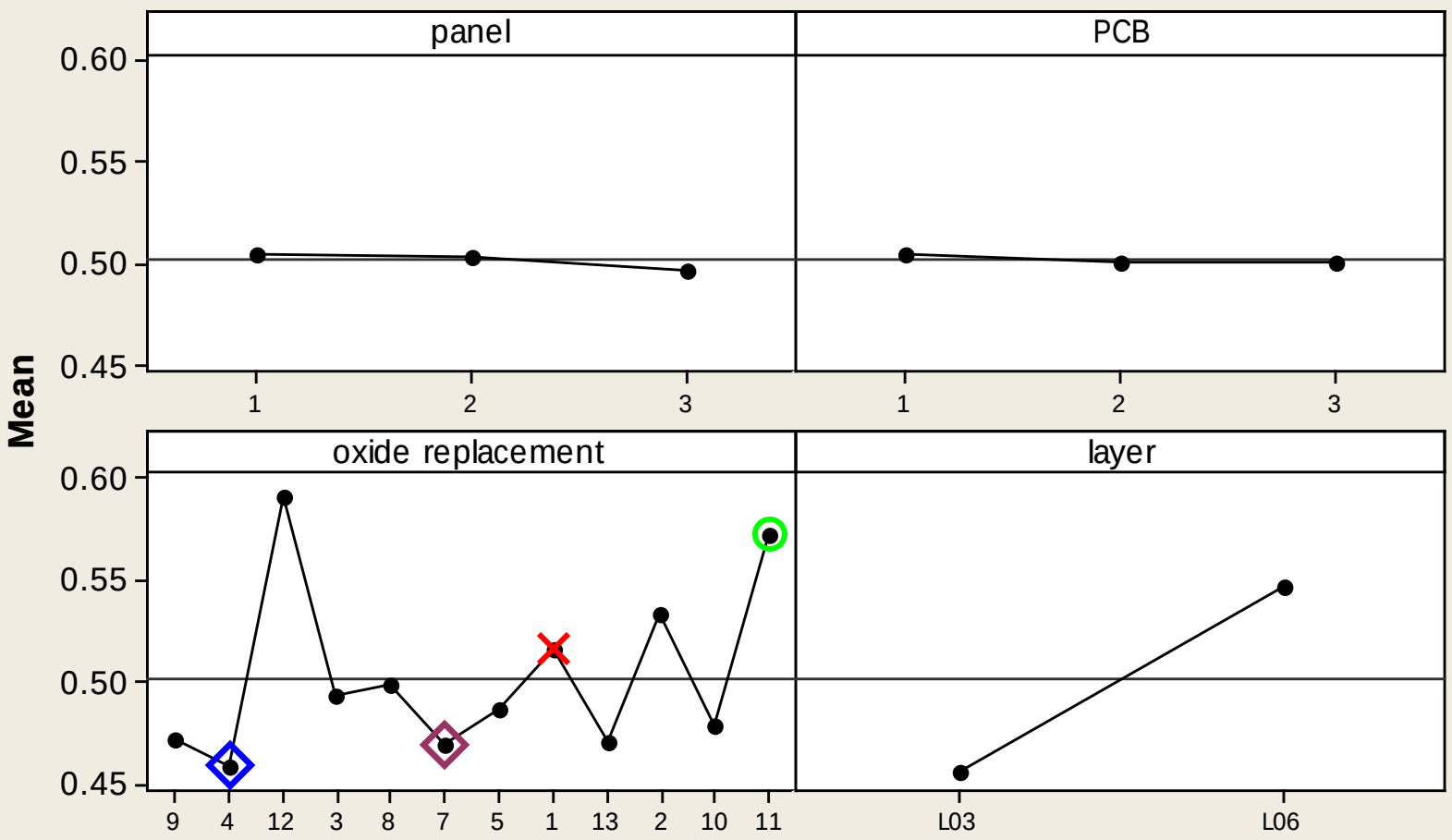
S21 delta @ 5 GHz



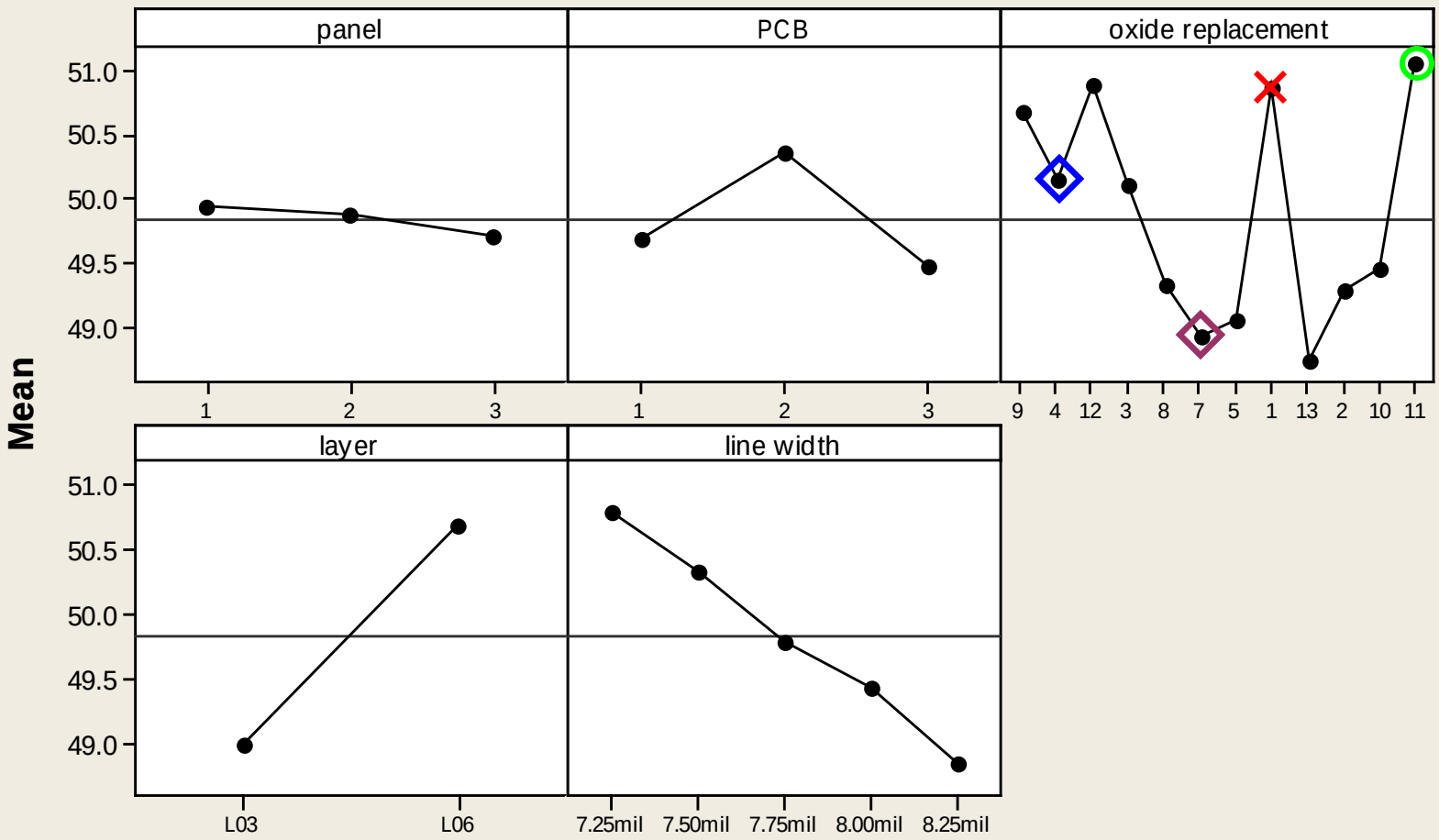
impedance (edge coupon)



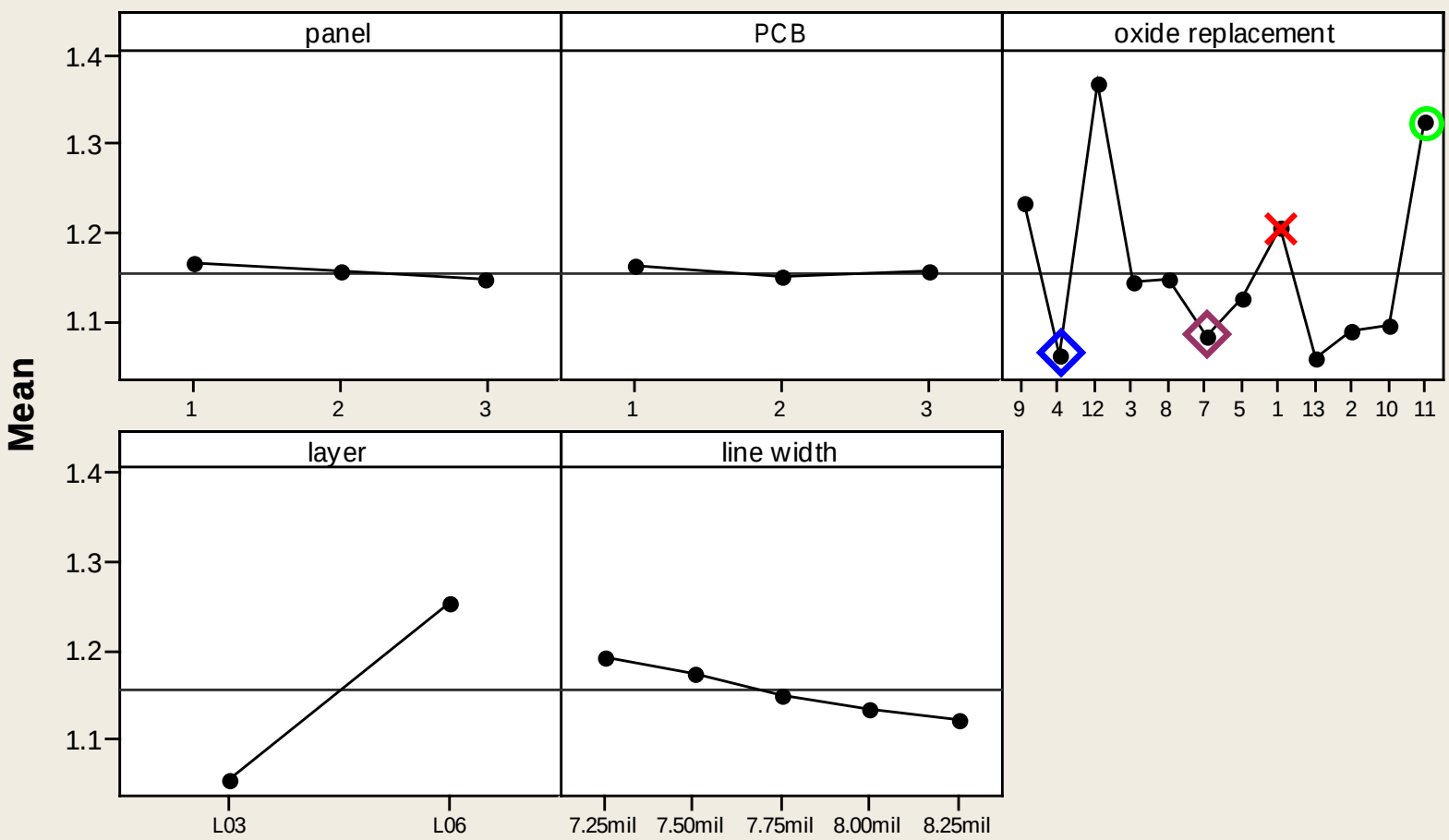
DC line resistance (edge coupon)



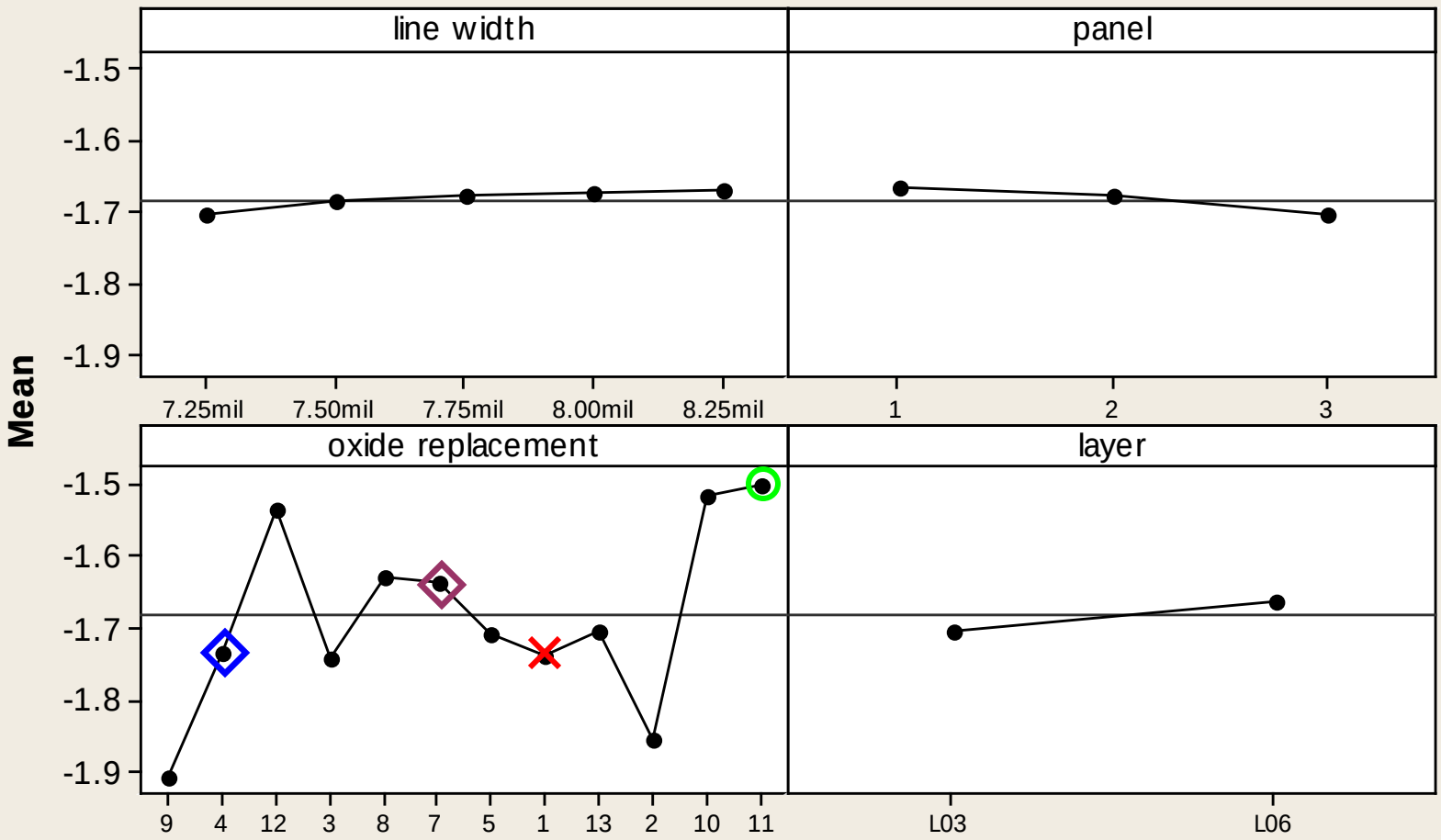
impedance (loss coupon)



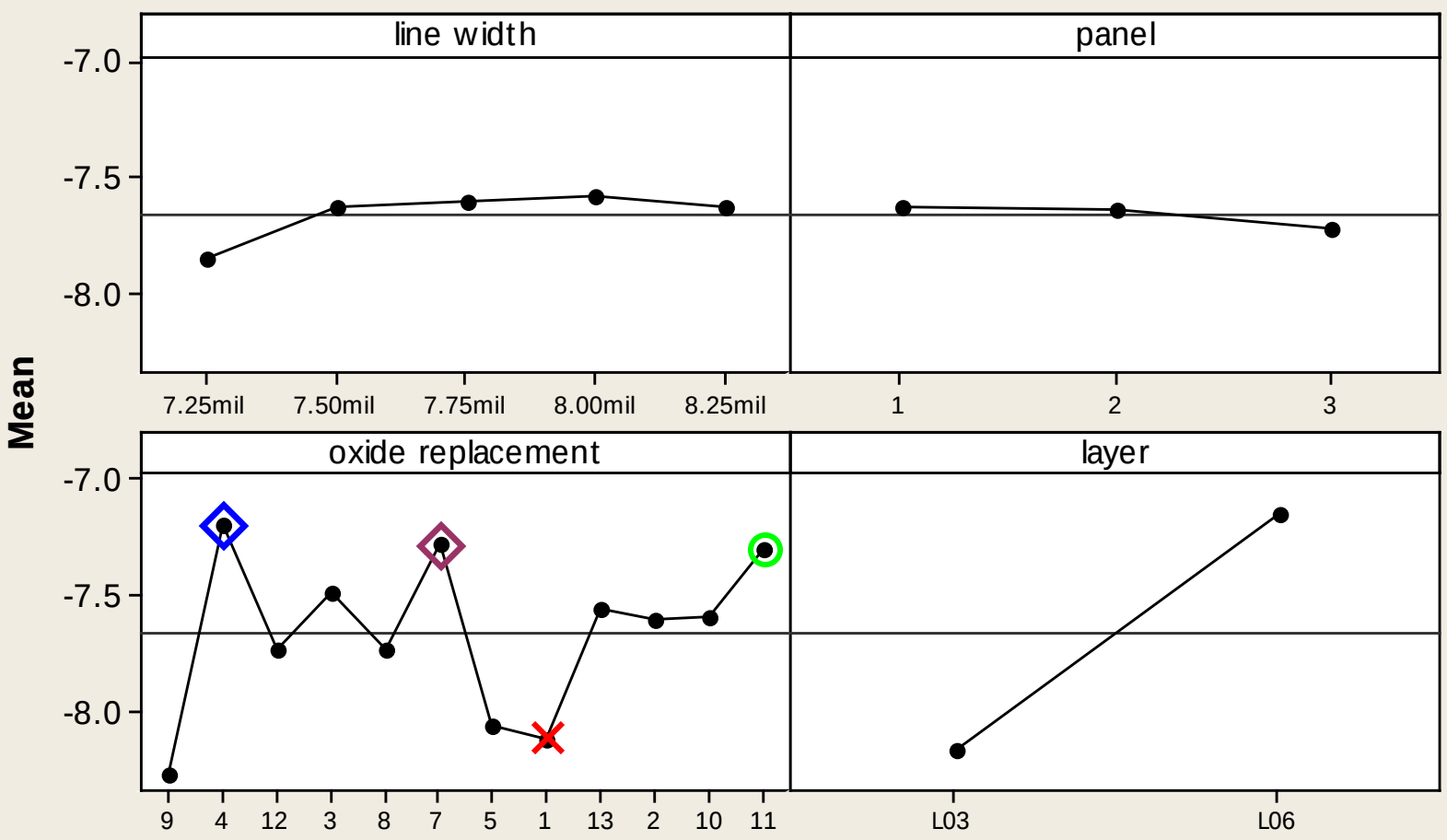
DC line resistance (loss coupon)



insertion loss at 0.75GHz



insertion loss at 5GHz



Anova numerical results: insertion loss @ 0.75GHz

- Analysis of Variance for S21 @ 0.75GHz, using Adjusted SS for Tests

Source	DF	Seq SS	Adj SS	Adj MS	F	P
line width	4	0.05282	0.05282	0.01321	1.86	0.117
panel	2	0.08512	0.08512	0.04256	5.99	0.003
oxide replacement	11	5.28071	5.28071	0.48006	67.55	0.000
layer	1	0.15498	0.15498	0.15498	21.81	0.000
Error	341	2.42352	2.42352	0.00711		
Total	359	7.99715				

- S = 0.0843036 R-Sq = 69.70% R-Sq(adj) = 68.10%

- line width is accounting for less than 1% → non significant factor
- panel is accounting for ~1% → non significant factor
- layer is accounting for ~2% → small factor
- oxide replacement is accounting for 66% of the variation → main influencing factor

Anova numerical results: insertion loss @ 5GHz

- Analysis of Variance for S21 @ 5GHz, using Adjusted SS for Tests

Source	DF	Seq SS	Adj SS	Adj MS	F	P
line width	4	3.2201	3.2201	0.8050	6.02	0.000
panel	2	0.6133	0.6133	0.3067	2.29	0.103
oxide replacement	11	38.6102	38.6102	3.5100	26.23	0.000
layer	1	92.5717	92.5717	92.5717	691.77	0.000
Error	341	45.6319	45.6319	0.1338		
Total	359	180.6473				

- S = 0.365811 R-Sq = 74.74% R-Sq(adj) = 73.41%

- line width is accounting for ~2% → small factor
- panel is accounting for less than 0.5% → non significant factor
- layer is accounting for ~51% → main influencing factor
- oxide replacement is accounting for ~21% of the variation → main influencing factor

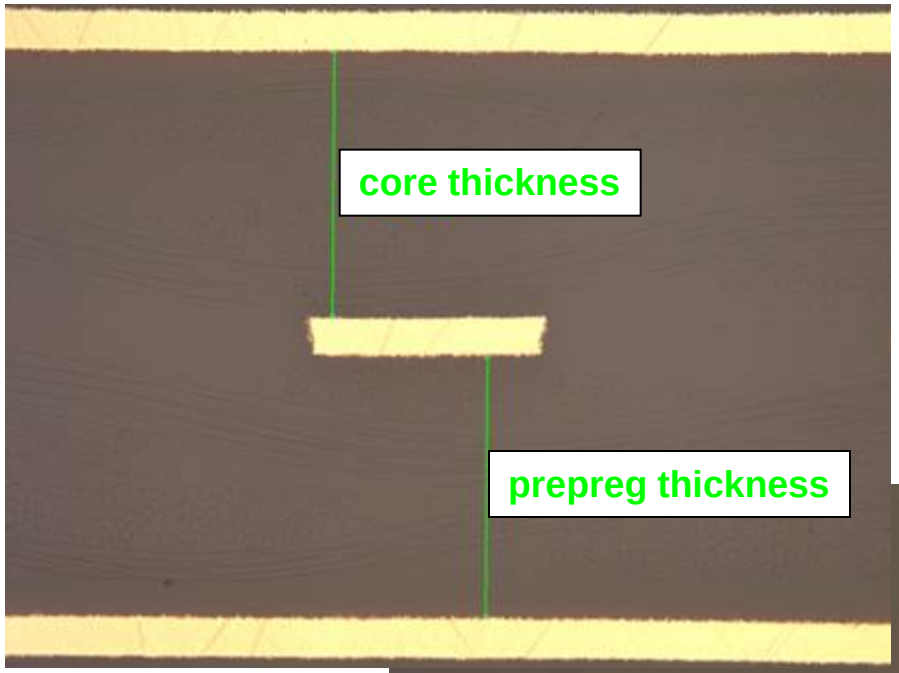
summary / electrical results

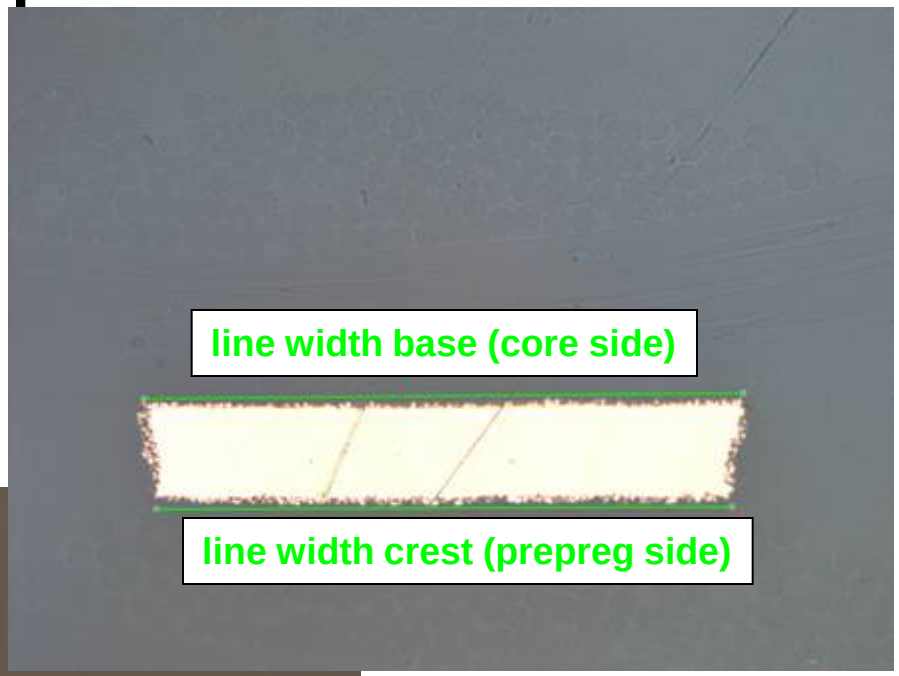
- the most promising (loss wise) oxide replacements / Cu foil types are:
  - RTF + low etch oxide replacement
  - RTF + non-etch adhesion promoter (NEAP)
  - VLP + standard oxide replacement
- all combinations above are showing a differential impedance of around 90ohms for the 1.14oz copper and 92..94ohms for 1oz (90ohm is target)
- all combinations above are showing a Rdc value of around 0.41..0.44ohms for the 1.14oz copper and between 0.51 and 0.59ohms for the 1oz (target value is below 0.6ohms)

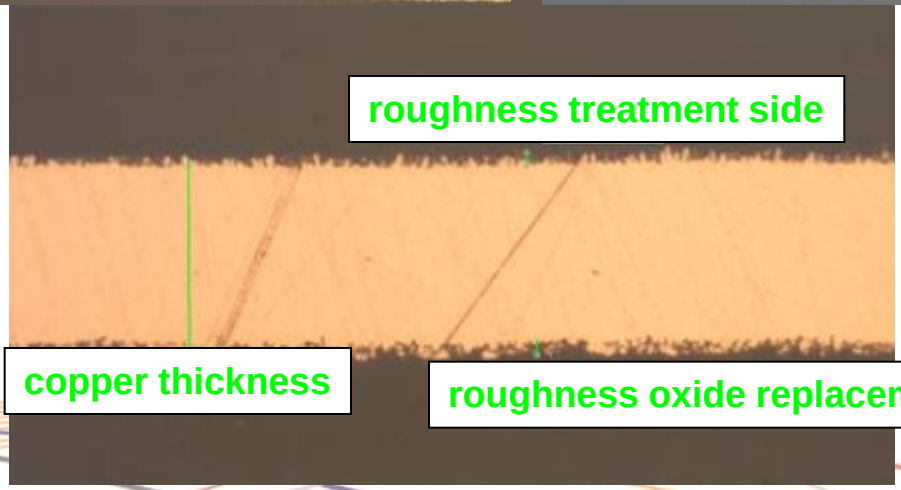
summary / electrical results (cont'd)

Oxide replacement	S21 @ 5GHz 1.14oz copper	S21 @ 5GHz 1oz copper
RTF + standard OR	8.74dB [ref]	7.48dB [1.26dB]
RTF + NEAP	7.61dB [1.13dB]	6.78dB [1.96dB]
RTF + low etch OR	7.55dB [1.19dB]	7.00dB [1.74dB]
VLP + standard OR	- - -	7.29dB [1.45dB]

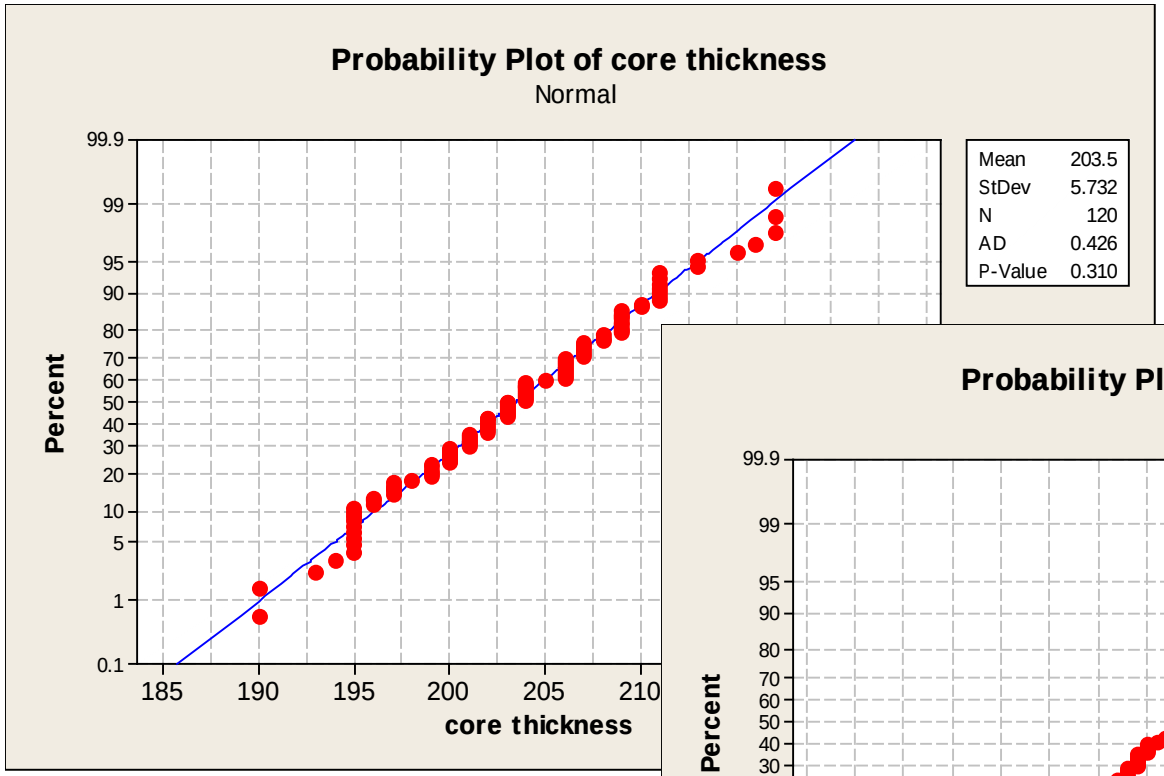
definition of parameters

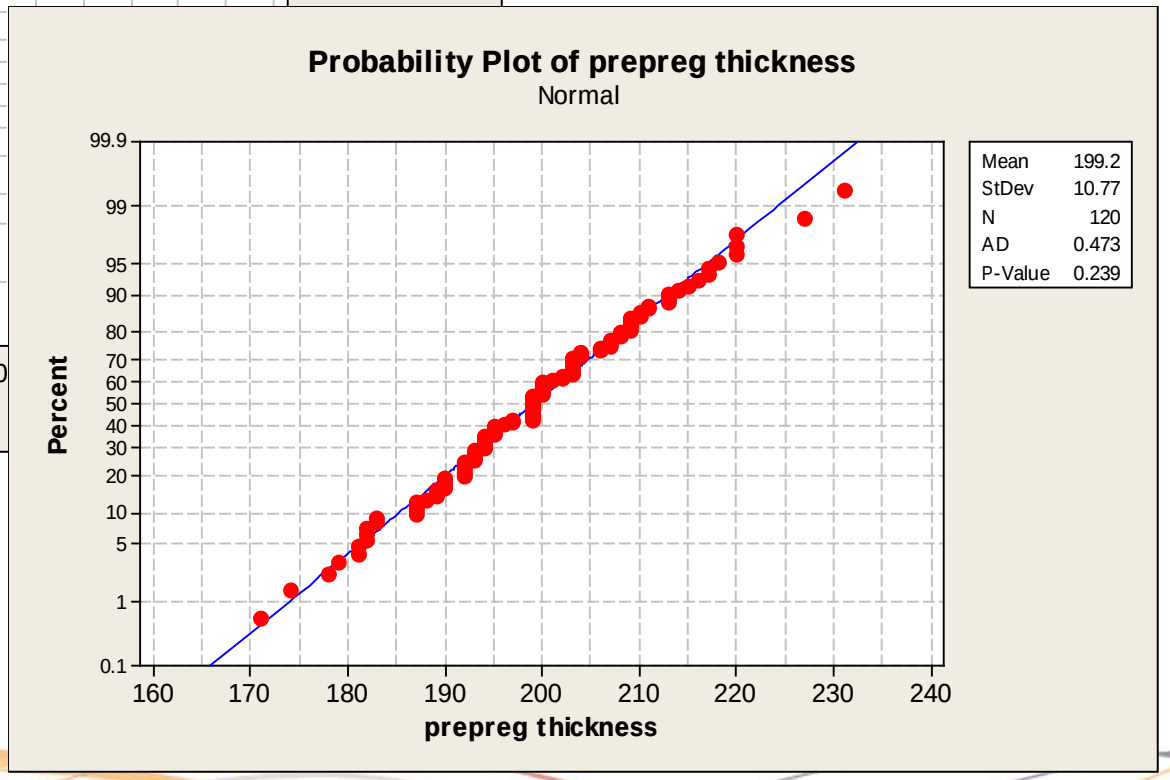






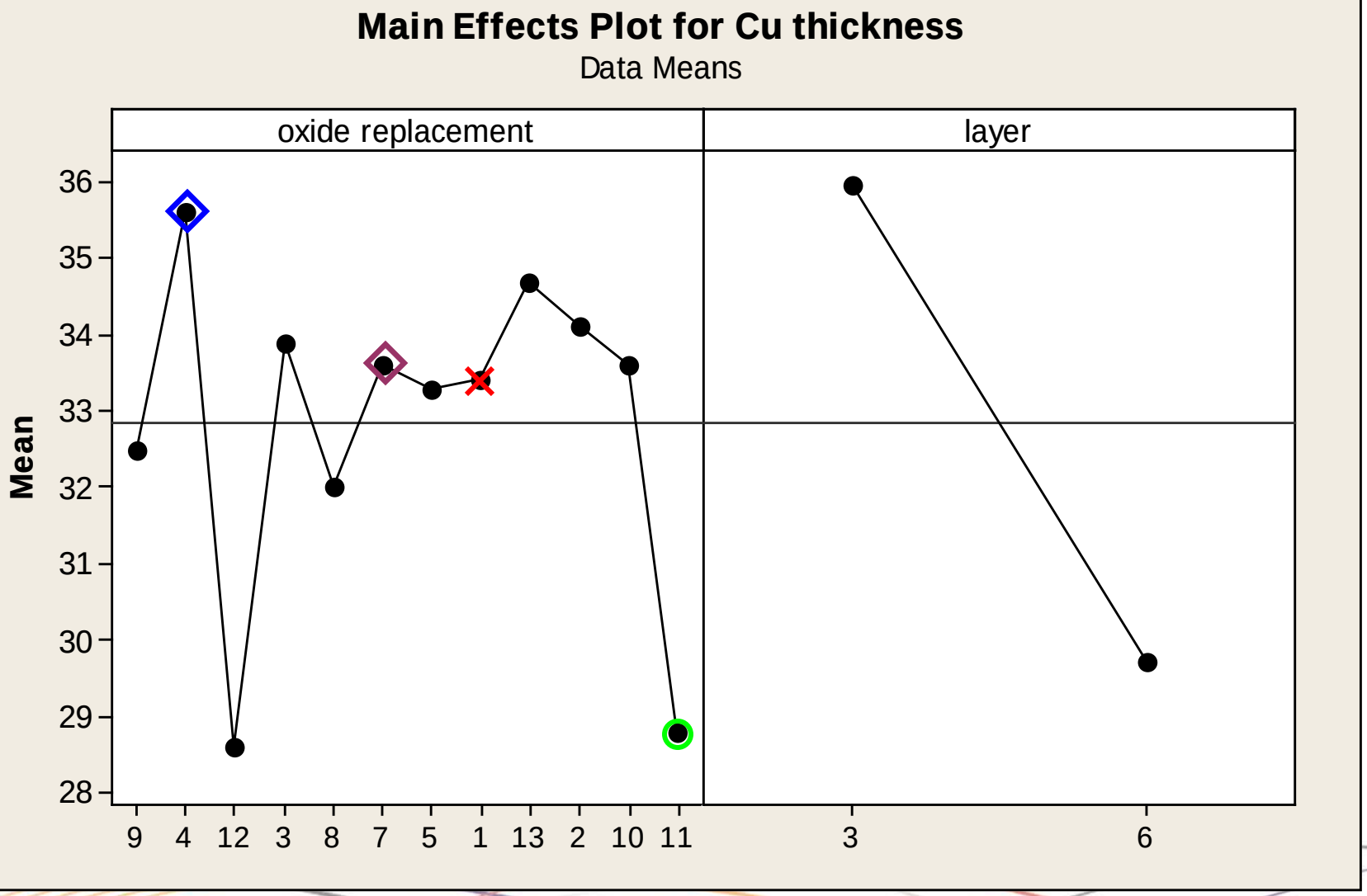
core and prepreg thickness



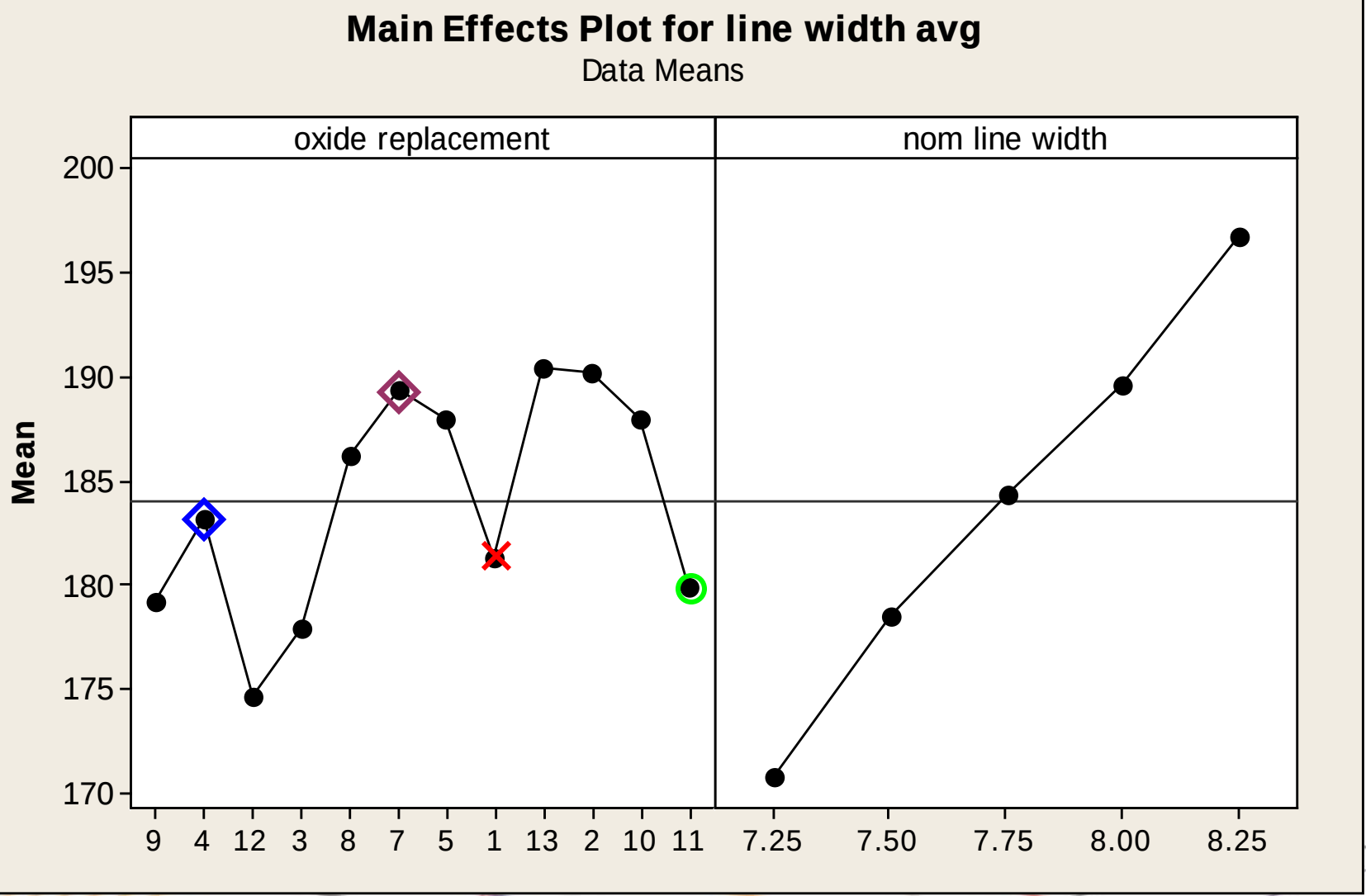


- dielectric thicknesses are normal distributed

copper thickness



line width


Main Effects Plot for line width avg
Data Means
oxide replacement
nom line width
Mean
200
195
190
185
180
175
170
9 4 12 3 8 7 5 1 13 2 10 11
7.25 7.50 7.75 8.00 8.25

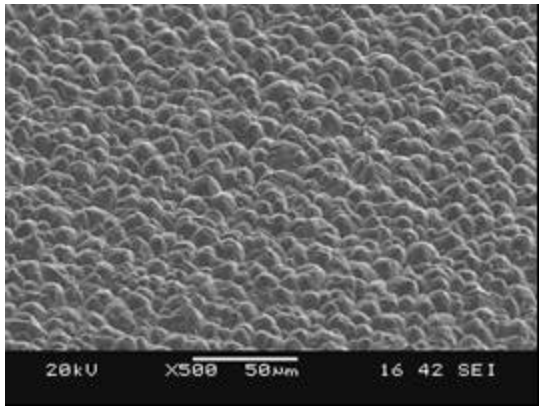
copper surface ‘as received’

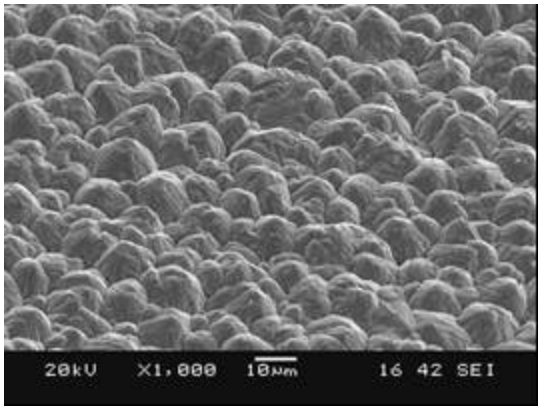
magnification 500x:

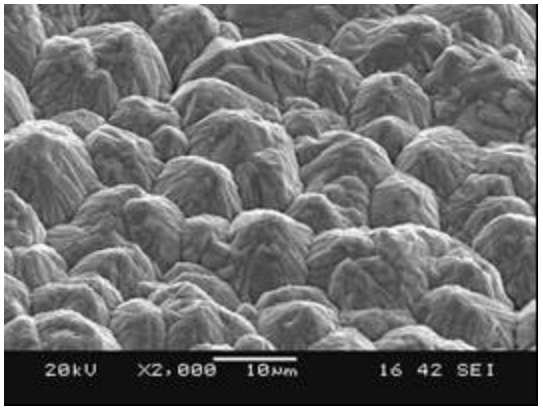
magnification 1000x:

magnification 2000x:

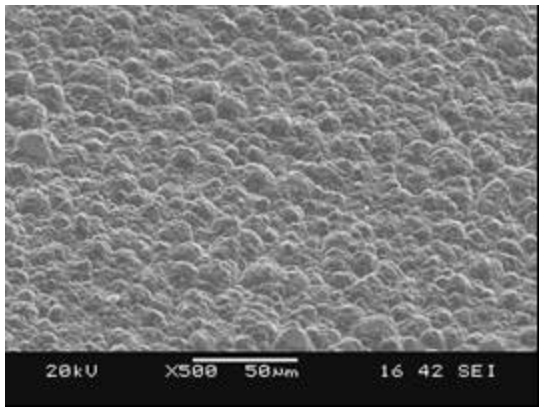
L03 / 1.14oz / 40um:

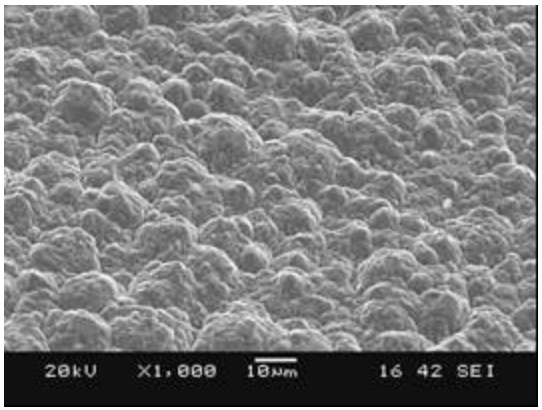


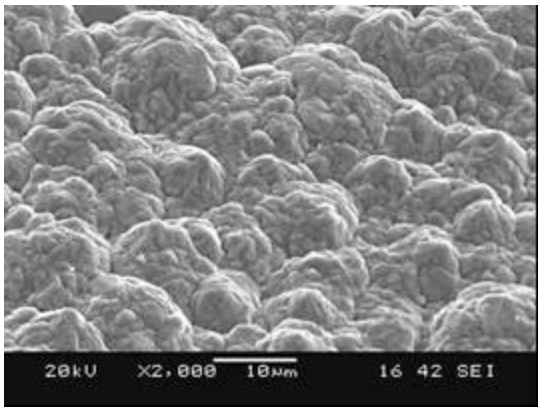




L06 / 1oz / 35um:







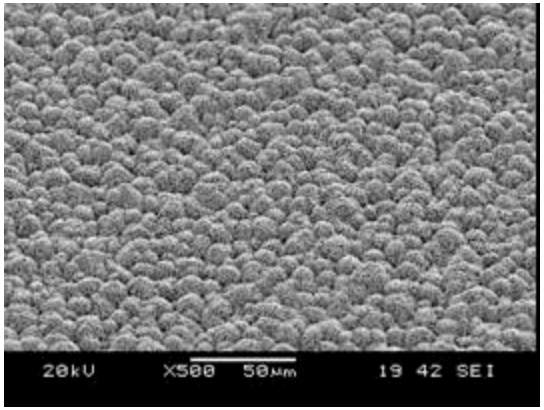
copper surface after IL process

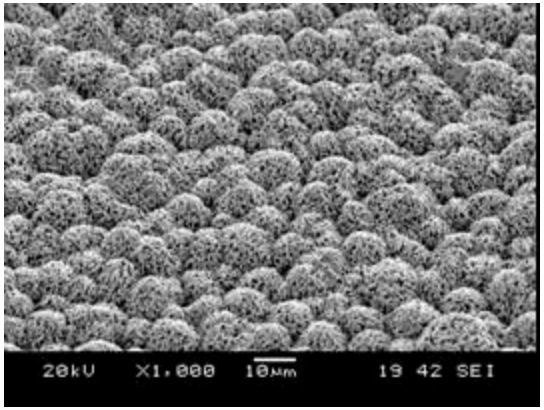
magnification 500x:

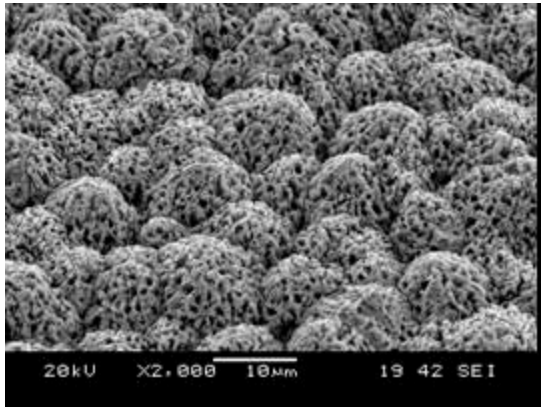
magnification 1000x:

magnification 2000x:

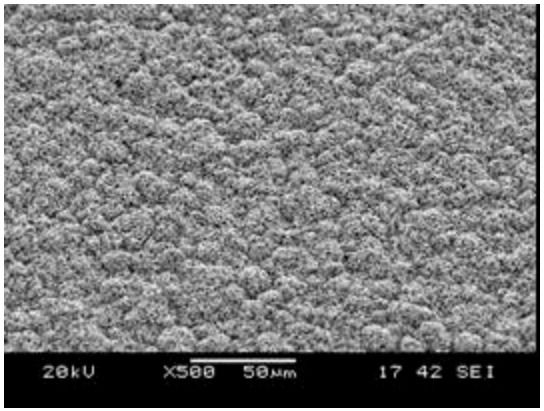
L03 / 1.14oz / 40um:

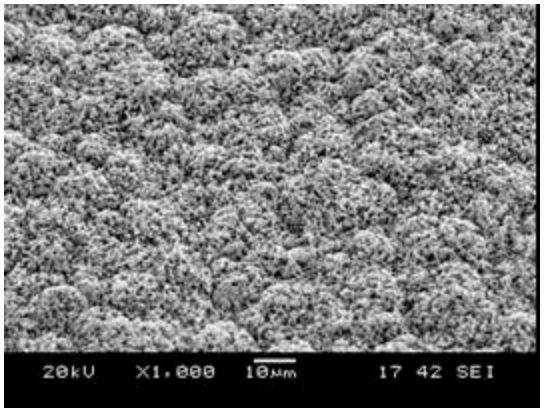


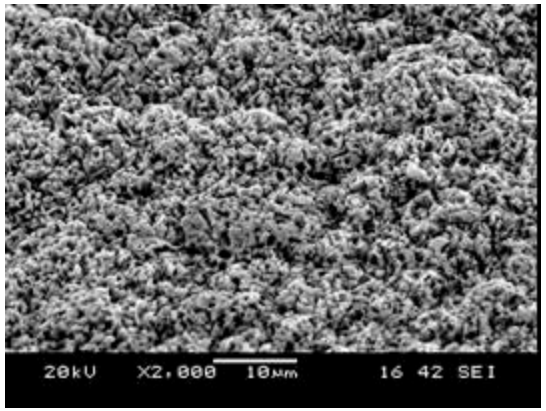




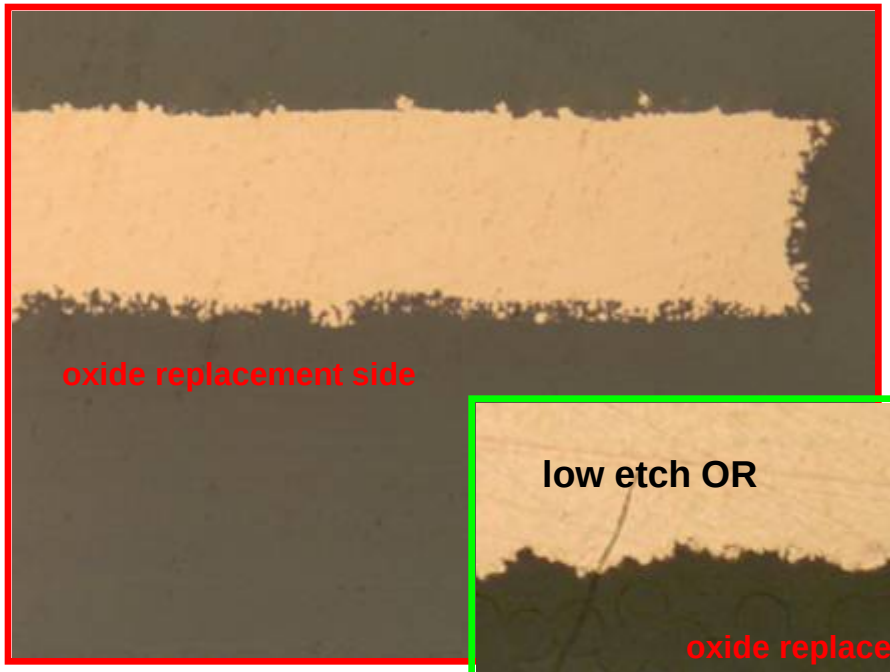
L06 / 1oz / 35um:

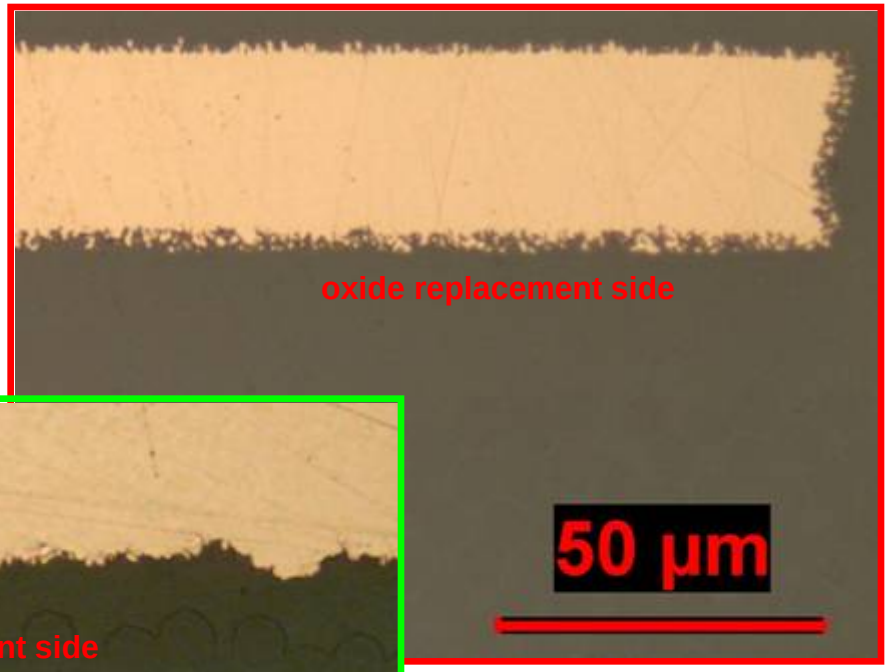


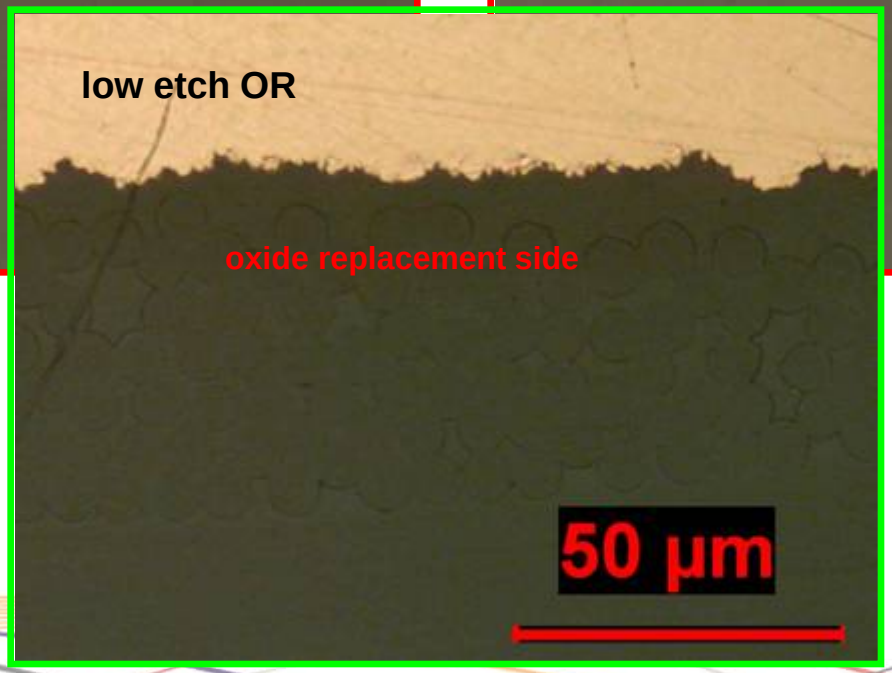




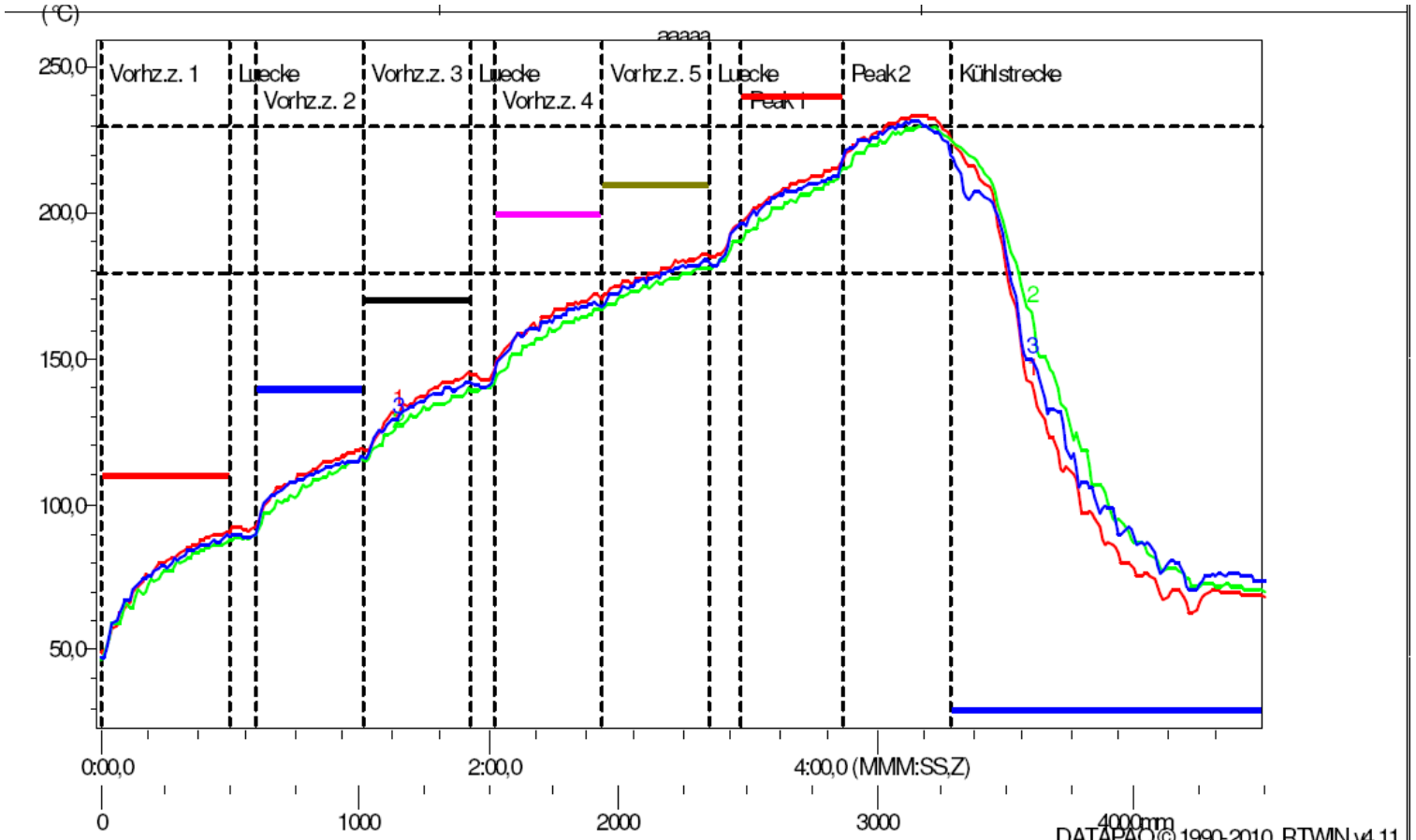
copper roughness – extreme oxide replacement attack







reflow profile (10x @ 230 deg C)



	Zone	Vorhz.z	Luecke	Vorhz.z	Vorhz.z	Luecke	Vorhz.z	Vorhz.z	Luecke	Peak 1	Peak 2	Kühlstrecke
Geschwindigkeit	Oben	110	0	140	170	0	200	210	0	240	265	30
750,0 (mm/min)	Unten	0	0	0	0	0	0	0	0	240	265	0

summary / thermal stress testing

- solder float tests
  - sample 13 shows delaminating issues already after 3 cycles solder float test
  - sample 2 shows after 6 cycles solder float test delaminating issues
- reflow simulation testing
  - visible delamination on sample 13 already after first cycle
  - cross sections after the reflow show only on sample 13 delaminating issues

acknowledgements

- Mohamed Kilouli for performing the thermal stress testing
- Dr. Sylvia Ehrler for many helpful inputs regarding material and copper foils
- Multek B2F, B3 and B5 for processing samples over alternative oxide replacement chemistries
- Circuit Foil Luxembourg for providing copper foil samples
- Isola Germany for providing special cores
- Atotech for processing samples over Secure HFz and reduced Black Oxide
- Enthone for processing samples over Alpha Prep
- OMG for processing samples over Cobra Bond

Thank You