Failure Mechanisms in Embedded Planar Capacitors during High Temperature Operating Life (HTOL) Testing

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Abstract
High temperature operating life (HTOL) testing was performed on embedded planar capacitors (with epoxy- $BaTiO_3$ composite dielectric) by subjecting these devices to highly accelerated temperature and voltage aging conditions. The objective of HTOL testing was to precipitate avalanche breakdown failures as a result of defects in the composite dielectric. These defects include porosity, voids, and agglomeration of $BaTiO_3$ in the epoxy matrix and are introduced during the manufacturing process. Since these tests were conducted under highly accelerated conditions, the failure mechanisms observed may not occur under the normal operating conditions of this device. However, the results of HTOL can be used in qualification of embedded planar capacitors and to further improve manufacturing processes to reduce the number of these defects.

During HTOL testing, the failure modes observed were a gradual decrease in the capacitance and a sharp decrease in the value of insulation resistance. The sharp decrease in the value of insulation resistance after some time was expected to be governed by the avalanche breakdown (ABD) of the dielectric. The ABD failures were modeled using the Prokopowicz model. The effect of the area of the capacitor and dielectric thickness on the time-to-failure as a result of ABD was also investigated.

A novel failure analysis technique was developed that can be used to locate the failure site of avalanche breakdown and understand the failure mechanism in this material. This technique can also be applied to some other dielectric materials as well. It was also observed that before ABD failures the dielectric material started to show signs of degradation. These degradations were detectable using AC measurements (measurement of dissipation factor) but were not observed in DC measurements (measurement of insulation resistance).

1 Introduction

Embedded planar capacitors (Fig. 1) are thin laminates embedded inside a multilayered printed wiring board (PWB) which serve both as a power/ground plane and as a parallel plate capacitor. These laminates extend throughout the PWB, reducing the need for discrete surface mount capacitors adjacent to a switching device (integrated circuit). A reduction in the number of surface mount capacitors [1], leading to miniaturization of the PWB, and improved electrical properties (such as reduced electromagnetic interference and simultaneous switching noise) [2] are the main advantages of using embedded planar capacitors. The reason for a decrease in the number of surface mount capacitors is a low value of parasitic inductance [3] of embedded planar capacitors due to elimination of leads and traces. With a decrease in the number of surface mount capacitors the number of solder joints will decrease, which is expected to increase the reliability of the PWB provided that the reliability of the embedded planar capacitor is comparable to or better than that of the traditional PWB.

The laminate consists of a thin dielectric material sandwiched between copper sheets. The dielectric material is generally a composite of polymer and ceramic. Pure polymers such as epoxy or polyimide are used in some applications but are not preferred due to a low value of the dielectric constant. Pure ceramic such as $BaTiO_3$ (as used in multilayer ceramic capacitors) is not used since the processing temperature of ceramics is high (~1000^{o}C) as compared to the regular PWB manufacturing processes (~250^{o}C). In order to overcome these difficulties, a composite of polymer and ceramic is used as the dielectric material. This composite combines the low temperature processability of polymers along with the high dielectric constant of ceramics [4]. With an increase in the ceramic loading the dielectric constant of the composite increases and various models have been proposed to model this behavior [5]-[9].

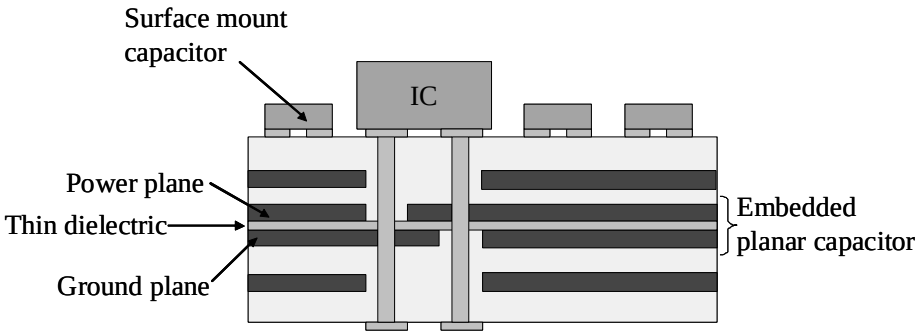

Fig. 1. Embedded planar capacitor

The polymer-ceramic composite that is widely used is an epoxy-$BaTiO_3$ composite. $BaTiO_3$ is used since its dielectric constant can be as high as 15000 in the crystalline phase [10]. The dielectric constant of $BaTiO_3$ is size dependent (in the crystalline phase) and exhibits the highest value when the particle size is close to 140 nm [11] and goes to a minimum when the particle size is close to 60 nm [12]. The dielectric constant of $BaTiO_3$ depends on the processing conditions, nature of dopants, and the frequency and temperature of measurements [13]. For epoxy-$BaTiO_3$ composites it has been observed that an increase in $BaTiO_3$ loading (for unimodally distributed particles) beyond 55-60% decreases the capacitance [14]. The decrease in capacitance is due to the presence of voids and pores in the composite when the theoretical maximum packing density is exceeded. Typically the maximum loading of $BaTiO_3$ is lower than 50% by volume since high filler loading can also result in poor adhesion to the metal electrodes [15]. This limits the maximum dielectric constant of the composite to close to 30 in commercially available dielectrics [16].

Embedded capacitors have many advantages but there has been an increasing focus on the reliability of these devices since failure of an embedded capacitor can lead to PWB failure. Embedded capacitors are not reworkable, and hence the entire PWB would have to be changed if these capacitors fail. The failure modes can be defined as a change in the electrical parameters such as capacitance, dissipation factor, or insulation resistance beyond permissible limits (which can be specified depending on the application of these capacitors). Further a drift in the electrical parameters of an embedded planar capacitor can affect the performance of the circuit where these capacitors are used. Some of the failure modes and mechanisms of embedded planar capacitors have been summarized in literature [17].

2 Avalanche breakdown due to defects in the dielectric

Since the dielectric constant of $BaTiO_3$ is size dependent, nanoparticles of $BaTiO_3$ are used which have a high dielectric constant. In suspension the ceramic nanoparticles are affected by mutual attraction due to van der Waals forces and form agglomerates [17]. One of the challenges in manufacturing these capacitors is to disperse the nanoparticles uniformly in the polymer matrix. Proper dispersion of these nanoparticles in the polymer matrix is essential to prevent any voids or agglomerates in the dielectric. A dispersant in a solvent medium is used that prevents the nanoparticles from agglomerating. [19]. After mixing the various components in the required quantities and following the process steps as shown in Fig. 2, the embedded capacitor paste (ECP) is formed. This ECP is then coated onto a substrate and heated to evaporate the solvent and cure the polymer [20].

The dielectric constant of $BaTiO_3$ is very high as compared to the dielectric constant of epoxy. When a composite dielectric is made by mixing a material of high dielectric constant (such as $BaTiO_3$) with a material of low dielectric constant (such as epoxy), the electric field is not uniform throughout the material [21]. The electric field is higher in the material of lower dielectric constant as compared to the material of higher dielectric constant. The electric field can be further disturbed by non-uniform dispersion of ceramic nanoparticles and defects in the dielectric such as voids or agglomeration of ceramic nanoparticles. Defects in the dielectric such as voids have the highest magnitude of electric field.

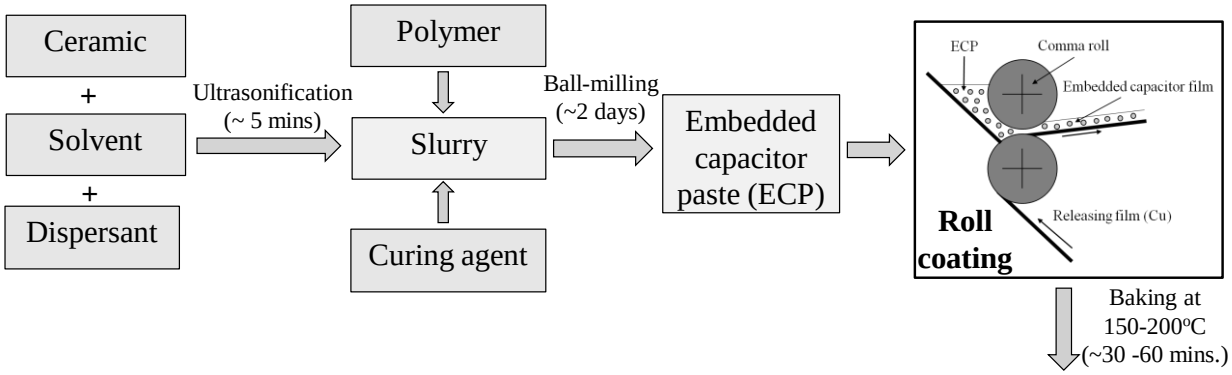

Fig. 2. Manufacturing of embedded capacitors

Defects introduced into the dielectric during the manufacturing processes can act as the site for the initiation of avalanche breakdown (ABD) [22]. During avalanche breakdown (ABD), there is a sudden increase in the value of leakage current. The stresses that increase the probability of ABD are temperature and voltage. A standard industrially acceptable test to precipitate these defects is the "hi-pot" test [23]. The hi-pot test is a go/no-go test in which a potential of up to 500 V is applied across the embedded capacitor laminate. Another technique that can be used to precipitate these defects is conducting a high temperature operating life (HTOL) test. During an HTOL test the embedded capacitor laminates are subjected to elevated temperature and voltage aging conditions [24]. If the temperature and voltage test conditions are much higher than the rated operating conditions, such that they exceed transition values associated with changes in the material or its behavior, the failure mechanisms observed during testing may not take place during normal operation due to highly accelerated stress conditions. However, the results of highly accelerated HTOL tests can nevertheless be used in qualification of embedded planar capacitors, to select among competing products, or to further improve the manufacturing processes to reduce the number of defects.

HTOL tests are used extensively in multilayer ceramic capacitors (MLCCs) with pure ceramic dielectric (such as $BaTiO_3$) to precipitate failure at defects in the dielectric. An empirical model of time-to-failure as a result of an increase in the leakage current (avalanche breakdown or thermal runaway) during HTOL was proposed by Prokopowicz and Vaskas, and can be represented as [25]:

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\left(\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \quad (1)$$

where t is the time-to-failure, V is the voltage, n is the voltage exponent, E_a is the activation energy, k is the Boltzmann constant, T is the temperature, and the subscripts *1* and *2* refer to the stress conditions. There exists a lot of published work on the computation of Prokopowicz model constants for pure $BaTiO_3$ dielectric used in MLCCs [26]-[30].

HTOL tests in embedded planar capacitors are not very common and the values of the Prokopowicz constants for a composite dielectric (epoxy and $BaTiO_3$) are not reported in the literature. In this work, HTOL tests are performed at multiple stress levels to investigate the effect of temperature, voltage, area of the capacitor, and dielectric thickness. Finally, the values of constants of the Prokopowicz equation are also computed.

3 Test vehicle and experimental setup

The test vehicle was a 4-layer PWB (shown in Fig. 3) in which layer 1 and 4 were the signal layers, and the planar capacitor laminate formed layer 2 (power plane) and layer 3 (ground plane). The power plane was etched at various locations to form discrete capacitors and the ground plane was common for all capacitors, as shown in Fig. 4. Two types of square capacitors, of area 0.026 in^2 (group A) and 0.19 in^2 (group B), are investigated in this work. There were 80 small capacitors (group A) and 6 large capacitors (group B) in the test vehicle. There were two different test vehicles, one with a laminate of dielectric thickness 8 μm and the other with a laminate of dielectric thickness 14 μm. The dielectric was a composite of $BaTiO_3$ of mean diameter equal to 0.25 μm loaded 45% by volume in bisphenol-epoxy. The dielectric constant and the dissipation factor of this composite was 16 and 0.05 respectively at 1 KHz.

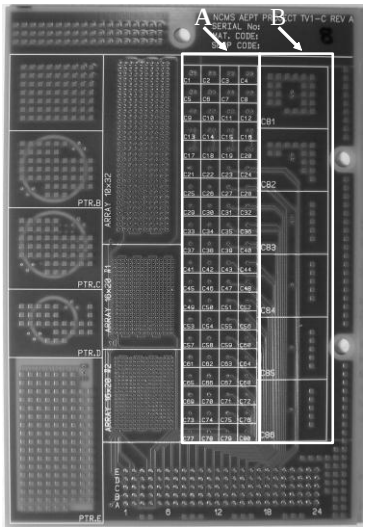

Fig. 3. Test Vehicle

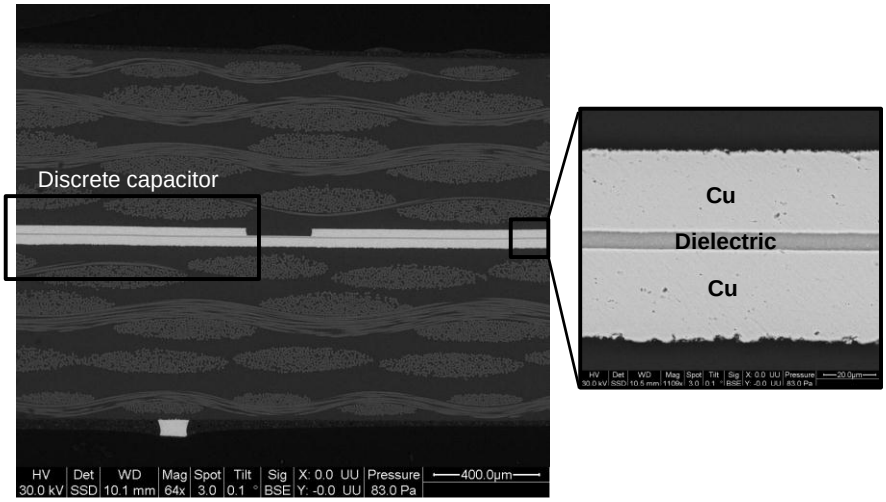

Fig. 4. Cross sectional view of the printed circuit board

An experimental setup was designed for stressing and monitoring the embedded capacitors in the HTOL test. In this work, three parameters, capacitance, dissipation factor, and insulation resistance were measured in situ once per hour. The capacitance and dissipation factor were measured using an Agilent 4263B LCR meter at 100 KHz. Insulation resistance was measured by an Agilent 4339B high resistance meter by applying a bias of 10 V. The switching of individual capacitor channels for measurements was performed by an Agilent 34980A switching/measuring unit. In order to limit the current in a capacitor channel in case of a dielectric failure, a 1.1 MΩ resistor was added in series with each capacitor. The failure criteria selected were a 20% decrease in capacitance, an increase in dissipation factor by a factor of 2, or a drop in insulation resistance below 10 MΩ. The boards were preconditioned at 105^{o}C for 48 hrs to remove any trace of moisture before the start of the experiments. Measurements were performed on 33 out of the 80 small capacitors and 4 out of the 6 large capacitors on the board.

4 Stress levels and design of experiments for HTOL tests

The temperature at all stress levels was below 130^{o}C which was the maximum operating temperature of the test board. The voltage was selected such that it was significantly lower than the breakdown voltage (dielectric withstanding voltage) of the dielectric at the test temperature. The breakdown voltage (V_{BD}) was measured for 10 small capacitors (8 µm dielectric thickness) at 85^{o}C and 125^{o}C and is shown in Fig. 5. Breakdown is expected to occur in the polymer matrix due to a large difference in the dielectric constant of epoxy and $BaTiO_3$, leading to a high electric field in the polymer matrix. It was observed that the value of V_{BD} decreased with an increase in the temperature. The reduction in the V_{BD} with temperature can be explained by an increase in the free volume of the polymer matrix [31]. According to this theory, as the temperature is increased the free volume of the polymer increases which increases the mean free path of the charge carrier. The charge

carriers are accelerated over a larger distance under the same electric field leading to a higher energy and hence the breakdown electric field reduces.

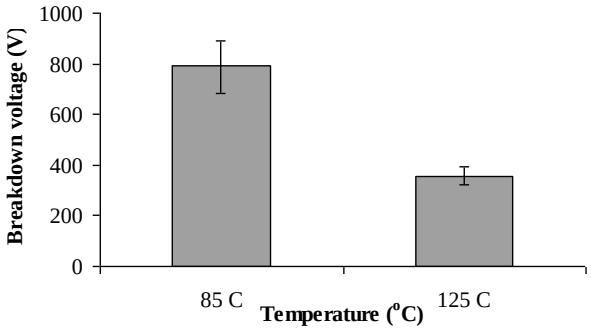

Fig. 5. Breakdown voltage (V_{BD}) of small capacitors (8 μm dielectric thickness)

The design of experiment (DoE) to investigate the effect of temperature, voltage, area, and dielectric thickness on the time-to-failure is shown in Table 1. The effect of each of these parameters was investigated by changing one parameter and keeping the other parameters constant. Altogether four failure terminated HTOL tests were conducted and their results are discussed in the following sections.

Table 1. Design of experiments for HTOL testing

Parameters	Parameter that was varied		Parameters that were constant			
	Level 1	Level 2	T	V	A	t
Temperature (T)	125°C	115°C	NA	285V	0.026 in^2	8 μm
Voltage (V)	285 V	225 V	125°C	NA	0.026 in^2	8 μm
Area (A)	0.026 in^2	0.19 in^2	125°C	285V	NA	8 μm
Dielectric thickness (t)	8 μm	14 μm	125°C	285V	0.026 in^2	NA

5 Observations of HTOL test

The failure modes observed at all the stress levels were a gradual decrease in capacitance and a sudden decrease in the value of insulation resistance implying avalanche breakdown (ABD). The capacitance was observed to degrade logarithmically and was discussed elsewhere [32]. Only failures as a result of ABD are discussed here since these failures occurred much before the capacitance failures. A plot of unreliability versus time-to-failure of ABD failures and capacitance failures is shown in Fig. 6. This analysis was performed using a Weibull 3 parameter distribution and the parameters of the distribution were found for ABD failures (β=1.0, η=218, γ=0.1) and capacitance failures (β=1.1, η=287, γ=305), where β is the shape parameter, η is the characteristic life, and γ is the location parameter.

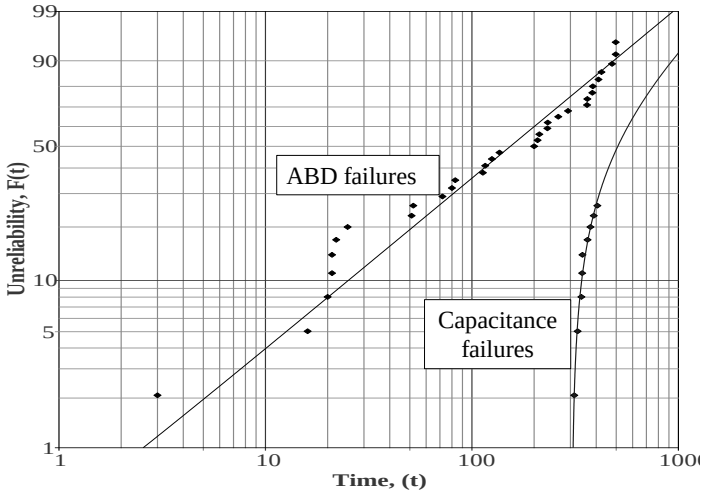

Fig. 6. Unreliability versus time-to-failure for various failure modes

At the time of a sudden decrease in the value of insulation resistance (IR) there was a sudden increase in the value of dissipation factor (DF). These observations indicate that the IR failures and DF failures were closely related and were governed by the same failure mechanism, avalanche breakdown. The behavior of IR and DF for one capacitor (small capacitor, tested at 125°C and 285V, with 8 μm dielectric thickness) is shown in Fig. 7. A closer examination of the data revealed that in some cases ABD failures did not result in a sharp increase in the value of DF and the capacitor did not fail according to the DF failure criterion. A representative plot of this behavior is shown in Fig. 8 (small capacitor, tested at 125°C and 285V, with 8 μm dielectric thickness).

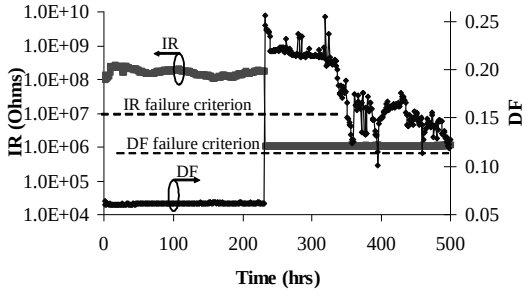

Fig. 7. Failure by both IR and DF failure criterion

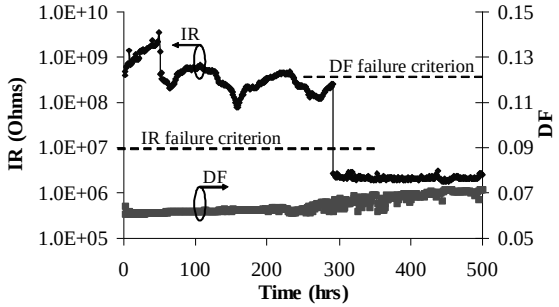

Fig. 8. Failure by only IR failure criterion

5.1 Effect of temperature

To investigate the effect of temperature, the data at 125°C, 285V and 115°C, 285V were compared (for small capacitors with 8 μm dielectric thickness). Statistical analysis was performed using Weibull statistics on the time-to-failure data of small capacitors (which had a significant sample size).

It was observed that failures were bimodal (followed two different distributions) so a mixed Weibull distribution with two populations was used. The two distributions as labeled as Type I and Type II in Fig. 9.

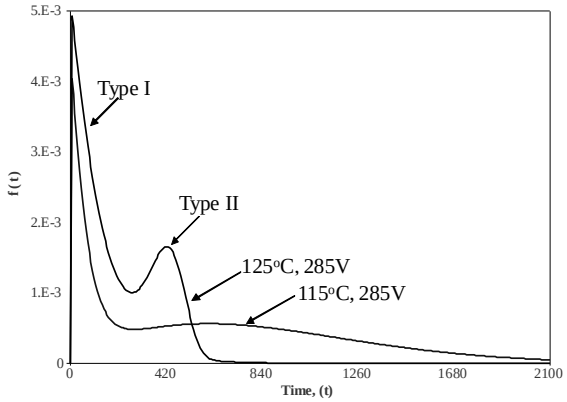

Fig. 9. Effect of temperature - probability distribution function (pdf) plot

The unreliability versus time-to failure plot at these two stress conditions is shown in Fig. 10. The values of parameters of the distribution, β, η, and P, (the proportion of failures associated with each of the two populations) were calculated and are given in Table 2. It was observed that the value of β for Type I distribution was close to 1 implying that these failures were random in nature. Further it was observed that a decrease in temperature by 10°C, decreased the MTTF for Type I failures (from 130 hrs to 63 hrs). Due to this behavior time-to-failure data of Type I failures are not used to calculate the Prokopowicz constants. The value of β for Type II failures was greater than 1 implying that these failures were actually the result of a wearout degradation mechanism. The value of activation energy (E_a) of the Prokopowicz model was computed for Type II failures and was found to be 0.99 eV.

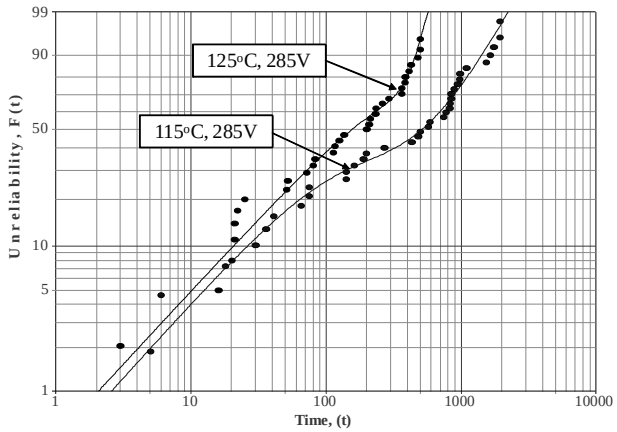

Fig. 10. Effect of temperature - unreliability versus time-to-failure plot

Table 2. Effect of temperature - statistical analysis of failures

Aging condition	Test duration (hrs)	Failed	Survived		MTTF (hrs)	β	η	P
125°C and 285V	500	32	1	Type I	130	1.0	130	0.7
				Type II	413	6.0	444	0.3
115°C and 285V	2000	36	0	Type I	63	1.1	65	0.3
				Type II	871	1.8	979	0.7

5.2 Effect of voltage

To investigate the effect of voltage, the data at 125°C, 285V and 125°C, 225V were compared (for small capacitors with 8 μm dielectric thickness). Statistical analysis was only performed on the time-to-failure data of small capacitors which had a significant sample size. The time-to-failure was observed to follow two different distributions at this new stress level also (125°C, 225V) as shown in Fig. 11.

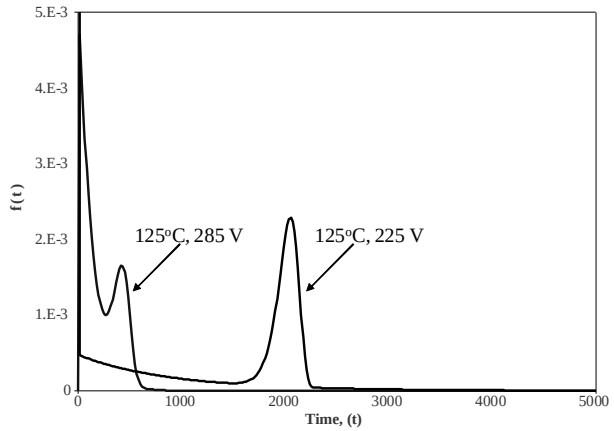

Fig. 11. Effect of voltage - probability distribution function (pdf) plot

The unreliability versus time-to failure plot at these two stress levels is shown in Fig. 12.The values of parameters of the distribution such as β, η, and P were calculated and are given in Table 3. The value of β for Type I failures was close to 1 implying that these failures were random in nature. The value of the voltage exponent (n) of the Prokopowicz model was computed for Type II failures and was found to be 6.7.

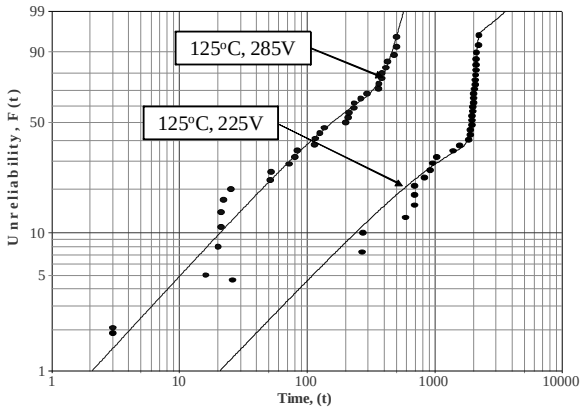

Fig. 12. Effect of voltage - unreliability versus time-to-failure plot

Table 3. Effect of voltage - statistical analysis of failures

Aging condition	Test duration (hrs)	Failed	Survived		MTTF (hrs)	β	η	P
125°C and 285V	500	32	1	Type I	130	1.0	130	0.7
				Type II	413	6.0	444	0.3
125°C and 225V	2300	35	1	Type I	935	1.0	935	0.4
				Type II	1996	22.0	2058	0.6

5.3 Effect of Area

All large capacitors were found to fail as a result of ABD within 10 hrs (well below the time-to-failure of small capacitors) at all stress levels.

Statistical analysis was not performed on the time-to-failure data of large capacitors due to their small sample size. The electric field experienced by the dielectric of both groups (A and B) was the same, so a smaller time-to-failure of large capacitors can be explained by an increase in the number of defects in the dielectric. The reason for avalanche breakdown (which is the failure mode in the current case) has been attributed to defects in the dielectric [22]. With an increase in the area of the capacitor, the number of defects in the dielectric per unit volume should increase, which might have led to the shorter time-to-failure for large capacitors. It implies that the Prokopowicz equation should also include a term for area to compensate for this. However an area scaling factor cannot be developed in the current experiments due to insufficient data.

5.4 Effect of dielectric thickness

To investigate the effect of dielectric thickness, the data on embedded capacitors with 8 μm and 14 μm dielectric thickness were compared at 125°C, 285V. Statistical analysis was only performed on the time-to-failure data of small capacitors which had a significant sample size. It was observed that with an increase in the dielectric thickness, type I (random) failures disappeared. The time-to-failure of embedded capacitors with 14 μm dielectric thickness was observed to follow a Weibull 2 parameter distribution. The unreliability versus time-to failure plot for both dielectric thicknesses is shown in Fig. 13. The values of parameters of the distribution were calculated and are given in Table 4.

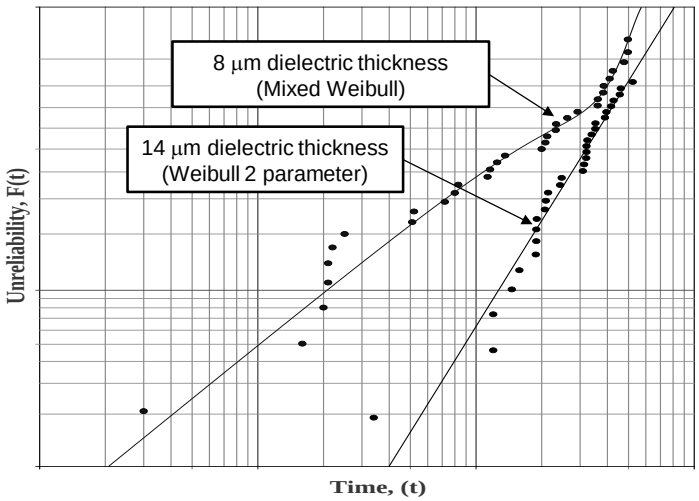

Fig. 13. Effect of dielectric thickness - unreliability versus time-to-failure plot

Table 4. Effect of dielectric thickness - statistical analysis of failures

Aging condition	Test duration (hrs)	Failed	Survived		MTTF (hrs)	β	η	P
125°C and 285V (t = 8 μm)	500	32	1	Type I	130	1.0	130	0.7
				Type II	413	6.0	444	0.3
125°C and 285V (t = 14 μm)	526	36	6		341	2.0	383	

6 Failure analysis

Failure analysis is needed to locate the failure site and understand the failure mechanism. The challenge in performing failure analysis was to locate the failure site, which was at an unknown location in the capacitor dielectric. Use of non-destructive techniques such as thermal imaging and SQUID (Superconducting Quantum Interference Device) microscopy may possibly locate the failure site which can be analyzed after cross sectioning. However in this paper a novel failure analysis technique is presented to understand the mechanism of these failures. To illustrate this technique failures were induced in a healthy capacitor at a predetermined failure site. Since the failure site was already known, use of non-destructive techniques to locate the failure site was eliminated. It has already been shown that the value of breakdown voltage in this material is temperature dependant. This particular property of breakdown voltage in this material was utilized in this failure analysis technique.

The procedure involved removing a healthy capacitor from the PWB. Electrical wires were connected to both planes of the capacitor and the capacitor was potted in epoxy. The potted sample was ground from one direction to expose both planes of the capacitor. Finally the sample was polished and etched in $FeCl_3$ solution to make sure that the spacing between the Cu planes was uniform throughout the surface and also to remove any Cu debris from the dielectric. Defects created during the grinding operation are not desirable. The objective of fine polishing and etching was to eliminate defects created during grinding. The process steps of sample preparation are shown in Fig. 14.

Once the sample was prepared, this technique was first applied to analyze the failure site of breakdown voltage (dielectric withstanding voltage). The polished surface of the sample was heated to 125°C and the voltage between the capacitor plates was ramped from zero to the point of dielectric breakdown. Since the polished surface of the sample was at the highest temperature (125°C), breakdown took place close to the polished surface. Fig. 15 shows the site of dielectric breakdown that was achieved using the technique described above. Energy dispersive spectroscopy (EDS) showed that the failure site (dark in color) was hollow and the Cu plates melted and moved towards each other. The sequence of events that led to this failure is under investigation

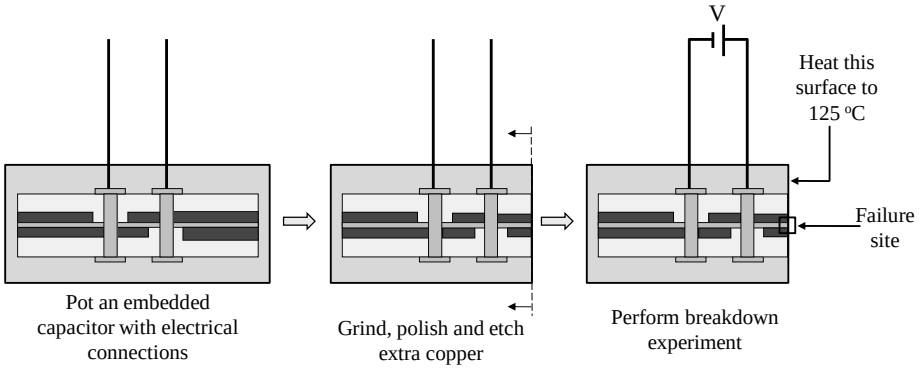

Fig. 14. Sample preparation steps

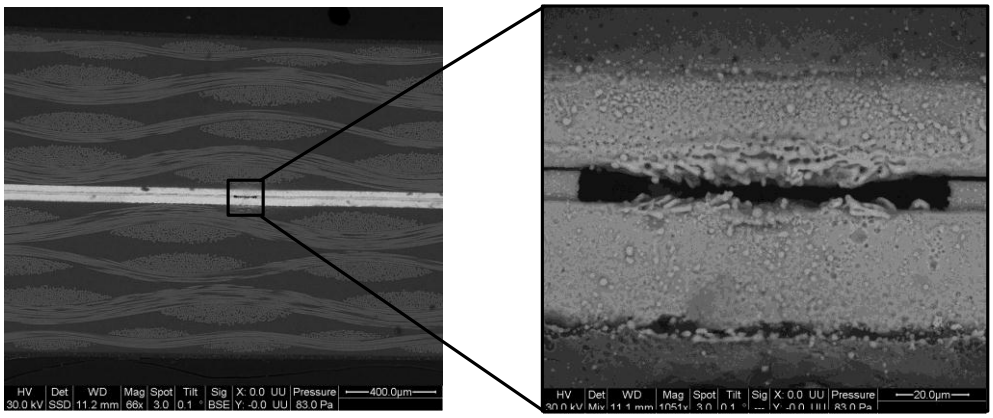

Fig. 15. Site of dielectric breakdown

The application of this technique to the breakdown samples demonstrates the potential usefulness of the approach. In the current work failures were created by ramping the voltage from zero until the point of dielectric breakdown. However during HTOL testing failures occur after some time at a constant temperature and voltage. The mechanism of failure in the above two cases appears to be different. In the future, similar samples will be prepared and a constant temperature and voltage (125^{o}C and 285V) will be applied under similar conditions until ABD of the dielectric is observed. These failures will be more representative of failures taking place during the HTOL test. Analysis of the failure site will be useful in understanding the ABD taking place during the HTOL test.

7 Detection of degradation in the dielectric material

Failures during HTOL testing took place after the stress was applied for some extent of time, depending on the stress level, which implies that the dielectric degrades with time under these conditions. It is expected that the degradation level in the dielectric increases with time and finally the degradation level reaches a threshold when the capacitor dielectric fails by ABD. The exact nature of this degradation mechanism is not clear. It might be possible that this degradation takes place due to Maxwell's stress in the dielectric [33]. Whatever might be the cause of this degradation, it is clear from Fig. 7 and Fig. 8 that insulation resistance is not able to capture these degradations. The value of insulation resistance was almost constant before a sudden drop at failure.

After conducting some preliminary analysis on the dissipation factor data, it was observed that the values of dissipation factor started to fluctuate before ABD failure as shown in Fig. 16. No such fluctuations were observed in the insulation resistance data and this may be because insulation resistance is a DC measurement and dissipation factor is an AC measurement (measured at 100 KHz). Insulation resistance only takes into account the DC leakage current in the dielectric. However dissipation factor takes into account both the DC leakage current and the polarization losses in the dielectric. This might be the reason that dissipation factor is able to show indications of dielectric degradation whereas insulation resistance is not. The fluctuations in the dissipation factor data were not found in all the capacitors and the reason for this is currently under investigation.

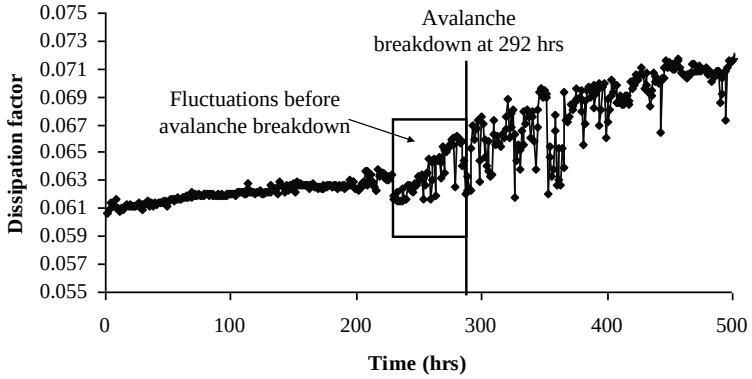

Fig. 16. Fluctuations in dissipation factor before avalanche breakdown

8 Future work

Future research will involve conducting HTOL experiments at two additional stress levels and calculation of the values of the constants of the Prokopowicz model with better confidence. For failure analysis, a sample will be prepared according to the new method described in this paper, and failures that are more representative of failures occurring during the HTOL test will be reproduced and analyzed.

9 Conclusions

High temperature operating life (HTOL) testing was conducted on embedded planar capacitors with epoxy-$BaTiO_3$ composite dielectric. The time-to-failure as a result of avalanche breakdown was modeled using the Prokopowicz model. The constants of the Prokopowicz model, n and E_a were found to be 6.3 and 0.99 eV respectively (for a composite with 45% loading of $BaTiO_3$ by volume in epoxy). This model can be used for the qualification of embedded planar capacitor laminates to precipitate defects resulting from the manufacturing process. Further a novel failure analysis technique was developed that can be used to locate the site of avalanche breakdown without the use of techniques such as thermal imaging or SQUID microscopy.

10 Acknowledgement

The authors would like to express their gratitude to the over 50 companies that support the Center for Advanced Life Cycle Engineering (CALCE) consortium and have sponsored this research.

11 References:

[1] M. Alam, M. H. Azarian, M. Osterman, and M. Pecht, "Effectiveness of Embedded Capacitors in Reducing the Number of Surface Mount Capacitors for Decoupling Applications," *Circuit World*, Vol. 36, Issue 1, 2010.

[2] A. Madou and L. Martens, "Electrical Behavior of Decoupling Capacitors Embedded in Multilayered PCBs," *IEEE Transactions on Electromagnetic Compatibility*, pp. 549-556, Vol. 43, No. 4, 2001.

[3] R. Ulrich and L. Schaper, *Integrated Passive Component Technology*, Wiley- IEEE Press, 2003.

[4] S. Bhattacharya and R. Tummala, "Next generation Integral Passives: Materials, Processes, and Integration of Resistors and Capacitors on PWB Substrates," *Journal of Material Science: Materials in Electronics*, pp. 253-268, Vol. 11, No. 3, 2000.

[5] D. Yoon, J. Zhang, and B. Lee, "Dielectric Constant and Mixing Model of $BaTiO_3$ Composite Thick Films," *Materials Research Bulletin*, pp. 765-772, Vol. 38, 2003.

[6] K. Jang and K. Paik, "Screen Printable Epoxy/$BaTiO_3$ Embedded Capacitor Pastes with High Dielectric Constant for Organic Substrate Applications," *Journal of Applied Polymer Science*, pp. 798-807, Vol. 110, 2008.

[7] Y. Rao, J. Qu, T. Marinis, and C. Wong, "A Precise Numerical Prediction of Effective Dielectric Constant for Polymer-Ceramic Composite based on Effective-Medium Theory," *IEEE Transactions on Components and Packaging Technologies*, pp. 680-683, Vol. 23, No. 4, 2000.

[8] J. Xu, S. Bhattacharya, K. Moon, J. Lu, B. Englert, and C. Wong, "Large-Area processable High K Nanocomposite-Based Embedded Capacitors," *Electronic Components and Technology Conference*, pp. 1520-1532, San Diego, CA, 2006.

[9] N. Jayasundere and B. Smith, "Dielectric Constant of Binary Piezo-electric 0-3 Composites," *Journal of Applied Physics*, pp. 2462-2466, Vol. 73, 1993.

[10] S. Swartz, "Topics in Electronic Ceramics," *IEEE Transactions on Electrical Insulation*, pp. 935-987, Vol. 25, No. 5, 1990.

[11] S. Wada, T. Hoshina, H. Yasuno, M. Nam, H. Kakemoto, T. Tsurumi, and M. Yashima, "Size Dependence of Dielectric Properties for nm-Sized Barium Titanate Crystallites and Its Origin," *Journal of Korean Physical Society*, pp. 303-307, Vol. 46, No. 1, 2005.

[12] M. Leonard and A. Safari, "Crystallite and Grain Size effects in $BaTiO_3$," *International Conference on Ferroelectric Applications*, pp. 1003-1005, Vol. 2, 1996.

[13] Y. Chiang, D. Birnie II, and W. Kingery, *Physical Ceramics-Principles for Ceramic Science and Engineering*, John Wiley and Sons, 1997.

[14] K. Paik, J. Hyun, S. Lee, and K. Jang, "Epoxy/$BaTiO_3$ ($SrTiO_3$) Composite Films and Pastes for High Dielectric Constant and Low Tolerance Embedded Capacitors in Organic Substrates," *Electronics System Integration Technology Conference*, pp. 794-801, Vol. 2, Dresden, Germany, 2006.

[15] R. Ulrich, "Matching Embedded Capacitor Dielectrics to Applications," *Circuit World*, pp. 20-24, Vol. 30, Issue 1, 2003.

[16] X. Jianwen, S. Kyoung, P. Pramanik, S. Bhattacharya, and C. Wong, "Optimization of Epoxy-Barium Titanate Nanocomposites for High Performance Embedded Capacitor Components," *IEEE Transactions on Components and Packaging Technologies*, pp. 248-253, Vol. 30, No. 2, 2007.

[17] M. Alam, M. H. Azarian, M. Osterman, and M. Pecht, "Reliability of Embedded Planar Capacitors under Temperature and Voltage Stress," *Capacitor and Resistor Technology Symposium*, Jacksonville, FL, 2009.

[18] H. Windlass, P. Raj, D. Balaraman, S. Bhattacharya, and R. Tummala, "Colloidal Processing of Polymeric Ceramic Nanocomposite Integral Capacitors," *IEEE Transactions on Electronics Packaging Manufacturing*, pp. 100-105, Vol. 26, No. 2, 2003.

[19] L. Chu, K. Prakash, M. Tsai, and I. Lin, "Dispersion of Nano-Sized $BaTiO_3$ Powders in Nonaqueous Suspension with Phosphate Ester and their Applications for MLCC," *Journal of European Ceramic Society*, pp. 1205-1212, Vol. 28, 2008.

[20] S. Ogitani, S. Allen, and P. Kohl, "Factors Influencing the Permittivity of Polymer/Ceramic Composites for Embedded Capacitors," *IEEE Transactions on Advanced Packaging*, pp. 313-322, Vol. 23, No. 2, 2000.

[21] S. Simamoto, Y. Sakata, J. Kojima, N. Kume, and Y. Tsujimoto, "Lacquered Polymer-Ceramic Composite Dielectric Film for Capacitors," *IEEE International Symposium on Electrical Insulation*, pp. 140-143, Baltimore, MD, 1992.

[22] B. Rawal and N. Chan, "Conduction and Failure Mechanisms in Barium Titanate Based Ceramics under Highly Accelerated Conditions," *AVX Technical Report*, Myrtle Beach, SC.

[23] J. Andresakis, T. Yamamoto, and N. Biunno, "New Non-Reinforced Substrates for use as Embedded Capacitors," *Circuit World*, pp. 36-41, Vol. 30, Issue 1, 2003.

[24] M. Alam, M. H. Azarian, M. Osterman, and M. Pecht, "Effect of Environmental Stress and Bias Conditions on Reliability of Embedded Planar Capacitors," *IPC APEX EXPO*, Las Vegas, NV, 2010.

[25] T Prokopowicz and A Vaskas, "Research and Development, Intrinsic Reliability, Subminiature Ceramic Capacitors," Final Report, ECOM-90705-F, pp. 175, NTIS AD-864068, 1969.

[26] W. Minford, "Accelerated Life Testing and Reliability of High K Multilayer Ceramic Capacitors," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, pp. 297-300, Vol. CHMT-5, No. 3, 1982.

[27] I. Yoo, L. Burton, and F. Stephenson, "Electrical Conduction Mechanisms of Barium-Titanate-Based Thick-Film Capacitors," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, pp. 274-282, Vol. CHMT-10, No. 2, 1987.

[28] J. Paulsen and E. Reed, "Highly Accelerated Life Testing of Base-Metal-Electrode Ceramic Chip Capacitors," *Microelectronics Reliability*, pp. 815-520, Vol. 42, 2002.

[29] G Maher, T Prokopowicz, and V Bheemineni, "High Volumetric Capacitance Low Fired X7R MLC Capacitor," *Electronics Components and Technology Conference*, pp. 280-284, Orlando, FL, 1993.

[30] M Randall, A Gaurav, D Skamser, and J Beeson, "Lifetime Modeling of Sub 2 Micron Dielectric Thickness BME MLCC," *Capacitor and Resistor Technology Symposium*, Scottsdale, AZ, 2003.

[31] M. Roy, J. Nelson, R. MacCrone, L. Schadler, C. Reed, R. Keefe, and W. Zenger, "Polymer Nanocomposite Dielectrics-The Role of the Interface," *IEEE Transactions on Dielectrics and Electrical Insulation*, pp. 629-643, Vol. 12, No. 4, 2005.

[32] M. Alam, M. H. Azarian, M. Osterman, and M. Pecht, "Prognostics of Embedded Planar Capacitors under Temperature and Voltage Aging," *ASME Conference on Smart Materials, Adaptive Structures and Intelligent Systems*, Philadelphia, PA, 2010.

[33] R. Bartnikas and R. Eichhorn, *Engineering Dielectrics-Volume II A*, ASTM Special Technical Publication, Philadelphia, PA, 1983.

Failure Mechanisms in Embedded Planar Capacitors during High Temperature Operating Life (HTOL) Testing

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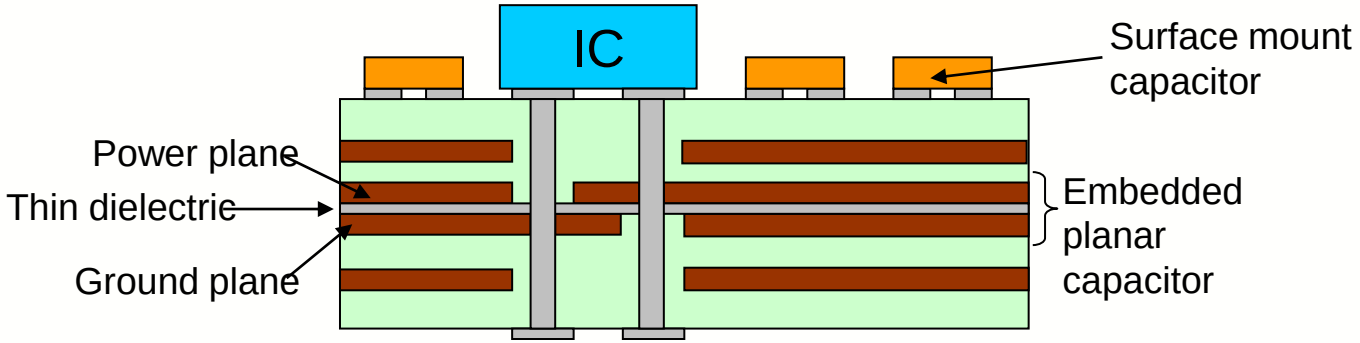
Embedded Planar Capacitors

- Thin laminate embedded inside a PWB that functions both as:
  - Power/ground plane
  - Parallel plate capacitor
- Used in decoupling operations and leads to:
  - Reduction in the number of surface mount capacitors[1]
  - Improved electrical performance[2](such as reduced EMI)



Embedded planar capacitors can lead to PWB miniaturization

[1]M. Alam, M. Azarian, M. Osterman, and M. Pecht, "Effectiveness of Embedded Capacitors in Reducing the Number of Surface Mount Capacitors for Decoupling Applications," Circuit World, Vol. 36, Issue 1, 2010.

[2]A. Madou and L. Martens, "Electrical Behavior of Decoupling Capacitors Embedded in Multilayered PCBs", IEEE Transactions on Electromagnetic Compatibility, pp. 549-556, Vol. 43, No. 4, 2001.

Dielectric Material

- Polymer-ceramic composites[1] are widely used.

Polymer
Pros: Low processing temp. (~200°C)
Cons: Low dielectric constant (~3-5)

+

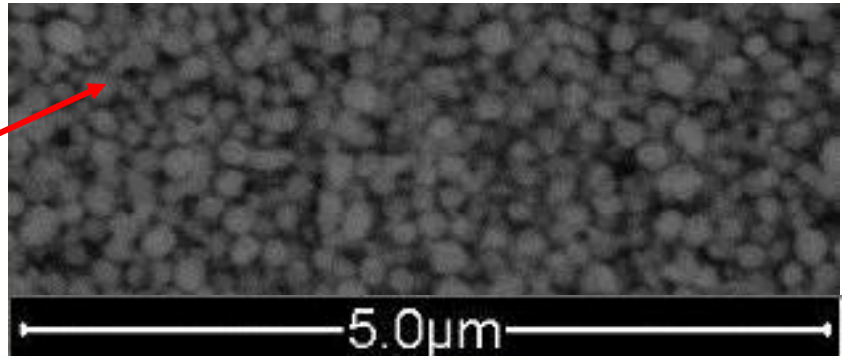
Ceramic
Pros: High dielectric constant (~1000)
Cons: High processing temp. (~1000°C)

⇨

Composite
Moderately high dielectric constant (~50)
Low processing temp. (~200°C)

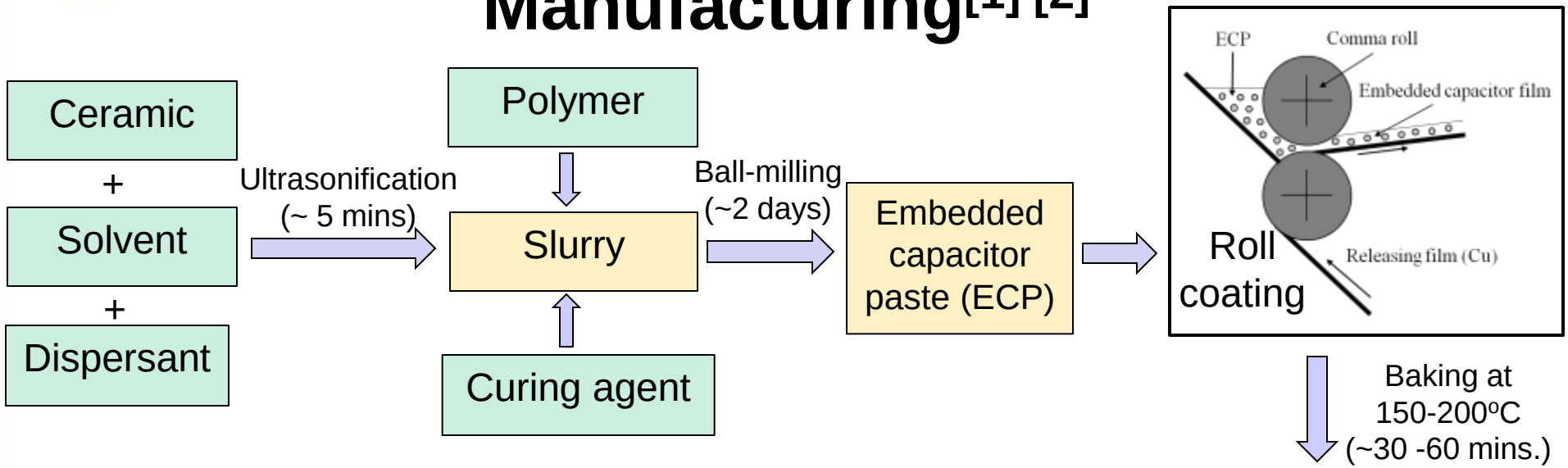
- The material investigated in this work is an epoxy-$BaTiO_3$ composite.

$BaTiO_3$ particles
(diameter ~ 0.1 μm)



[1]K. Jang and K. Paik, "Screen Printable Epoxy/$BaTiO_3$ Embedded Capacitor Pastes with High Dielectric Constant for Organic Substrate Applications," Journal of Applied Polymer Science, pp. 798-807, Vol. 110, 2008.

Manufacturing[1] [2]



- Dispersant: is added to prevent agglomeration of ceramic nanoparticles due to Vander Walls force.
- Ultrasonification and ball milling: are performed to break down agglomerates of ceramic nanoparticles.

Non uniform dispersion of ceramic nanoparticles can lead to defects in the dielectric such as voids, porosity and agglomeration of ceramic particles

[1]S. Ogitani, S. Allen, and P. Kohl, "Factors Influencing the Permittivity of Polymer/Ceramic Composites for Embedded Capacitors", IEEE Transactions on Advanced Packaging, pp. 313-322, Vol. 23, No. 2, 2000.

[2]L. Chu, K. Prakash, M. Tsai, and I. Lin, "Dispersion of Nano-Sized $BaTiO_3$ Powders in Nonaqueous Suspension with Phosphate Ester and their Applications for MLCC", Journal of European Ceramic Society, pp. 1205-1212, Vol. 28, 2008.

Avalanche Breakdown due to Defects in the Dielectric

- Defects have a high value of local electric field and can lead to avalanche breakdown (ABD)[1] of the dielectric.
- To precipitate these defects, embedded capacitor manufacturer's typically conduct a "hi-pot"[2] test:
  - a potential of up to 500 V is applied across the embedded planar capacitor
  - go/no-go test

A time-to-failure (TTF) model for these defects related failures has not been developed for embedded capacitors

$$TTF_{ABD} = f(T, V)$$

Effect of dielectric thickness and area of the capacitor on TTF_{ABD} ???

[1]B. Rawal and N. Chan, "Conduction and Failure Mechanisms in Barium Titanate Based Ceramics under Highly Accelerated Conditions," AVX Technical Report, Myrtle Beach, SC.

[2]J. Andresakis, T. Yamamoto, and N. Biunno, "New Non-Reinforced Substrates for use as Embedded Capacitors", Circuit World, pp. 36-41, Vol. 30, Issue 1, 2003.

Prokopowicz Model

(Used in High Temperature Operating Life Testing of MLCCs)

Used in multilayer ceramic capacitors (MLCCs) with ceramic dielectric:

- to precipitate defect related failures
- Oxygen vacancy migration related failures

$$\frac{MTTF_1}{MTTF_2} = \left(\frac{V_2}{V_1}\right)^n \exp\left(\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

n and E_a for pure $BaTiO_3$ is available in literature [1]

Can this model used in embedded capacitors with composite dielectric?

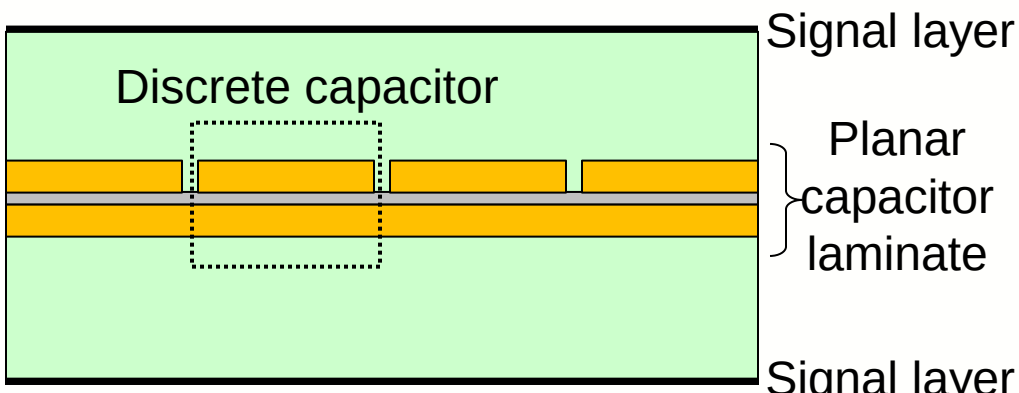
What are the values of n and E_a for an epoxy-$BaTiO_3$ composite?

where MTTF is the mean-time-to-failure as a result of ABD, V is the voltage, n is the voltage exponent, E_a is the activation energy, k is the Boltzmann constant, T is the temperature, and the subscripts *1* and *2* refer to the two aging conditions.

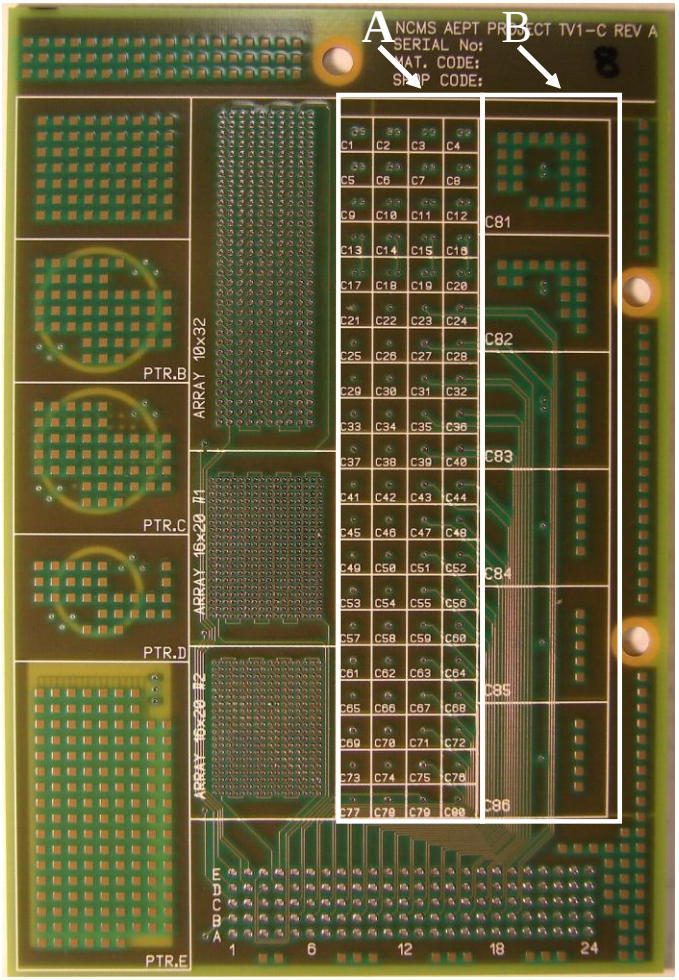
[1] J. Paulsen and E. Reed, "Highly Accelerated Life Testing of Base-Metal-Electrode Ceramic Chip Capacitors," Microelectronics Reliability, pp. 815-520, Vol. 42, 2002.

Test Vehicle

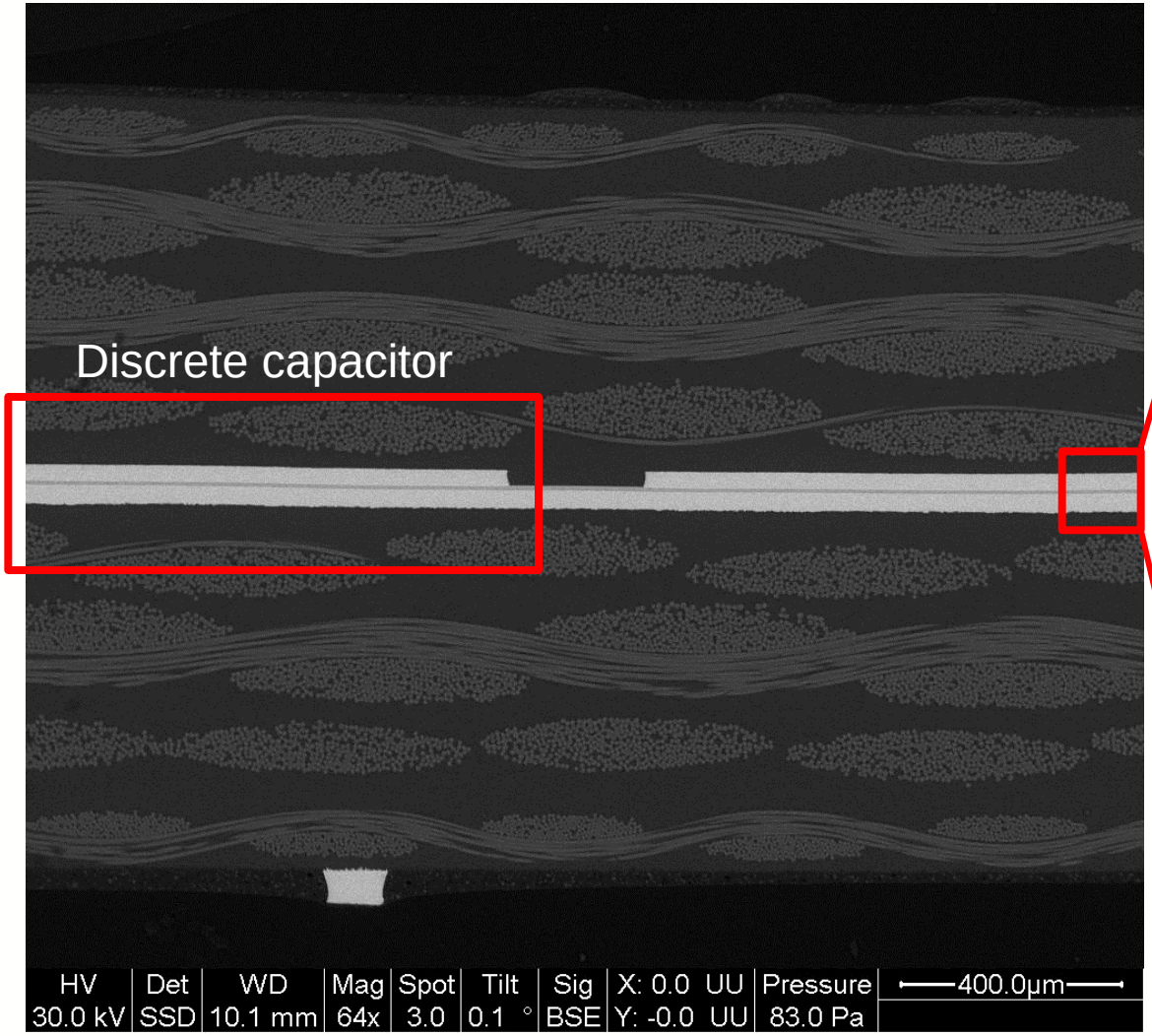
- Four layered PWB:

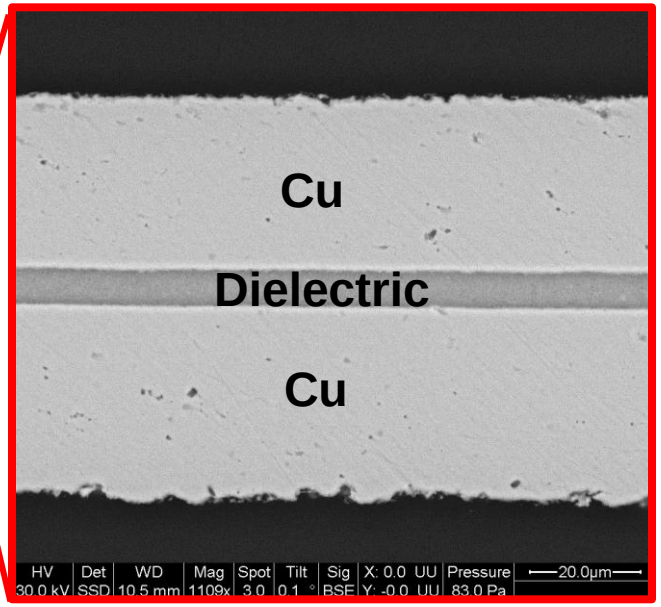


- Two types of PWBs:
  - 8 μm dielectric thickness
  - 14 μm dielectric thickness
- Two types of capacitors :
  - Small (Group A): ≈ 400 pF and 80 capacitors/test vehicle
  - Large (Group B): ≈ 5 nF and 6 capacitors/test vehicle.



Sectional View of the PWB





Dielectric was a composite of epoxy and $BaTiO_3$ (loaded 45% by vol.), whose dielectric constant was 16 at 1 KHz

DoE for HTOL Testing

- High temperature operating life (HTOL) experiments were designed to investigate the effect of:
  - Temperature (T)
  - Voltage (V)
  - Area (A)
  - Dielectric thickness (t)
- Altogether 4 failure terminated HTOL tests were conducted

Factors	**Levels**		Values of parameters that were kept constant			
	1	**2**	T	V	A	t
Temperature	**125°C**	**115°C**	NA	285V	0.026 in^2	8 mm
Voltage	**285 V**	**225 V**	125°C	NA	0.026 in^2	8 mm
Area	**0.026 in^2**	**0.19 in^2**	125°C	285V	NA	8 mm
Dielectric thickness	**8 mm**	**14 mm**	125°C	285V	0.026 in^2	NA

Measured Parameters and Failure Criterion

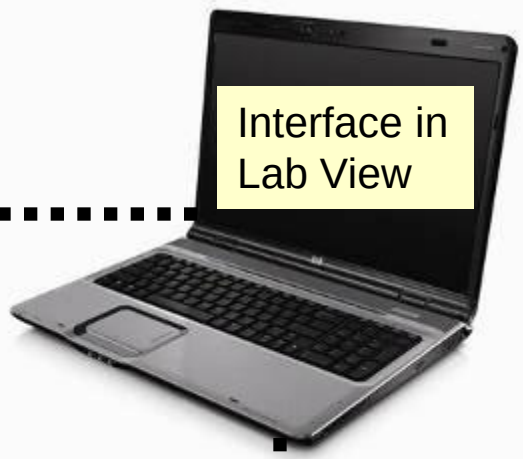
- 33 out of 80 small capacitors and 4 out of 6 large capacitors were selected.
- Measured parameters:
  The following parameters of each capacitor were measured once every hour:
  - Capacitance (*C*) at 100 kHz
  - Dissipation factor (*DF*) at 100 kHz
  - Insulation resistance (*IR*) at 10 V.
- Failure Criterion:

  The failure criteria selected were:
  - 20% decrease in capacitance (*C*)
  - increase in dissipation factor (*DF*) by a factor of 2
  - drop in insulation resistance (*IR*) to 10 MΩ.

Experimental Setup

LCR Meter
(for capacitance and dissipation factor measurements)

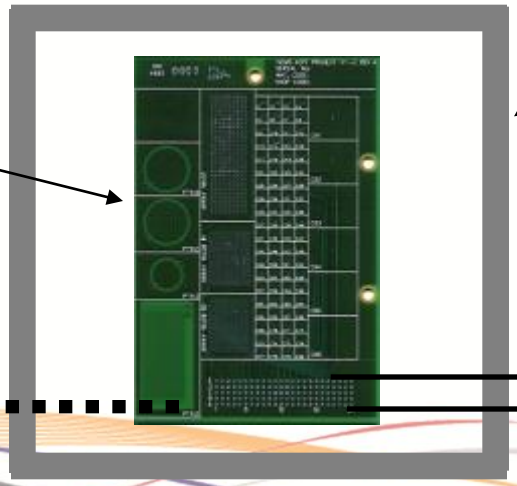
Multiplexer
(for switching of individual channels)



High Resistance Meter
(for insulation resistance measurements)

Thermal chamber

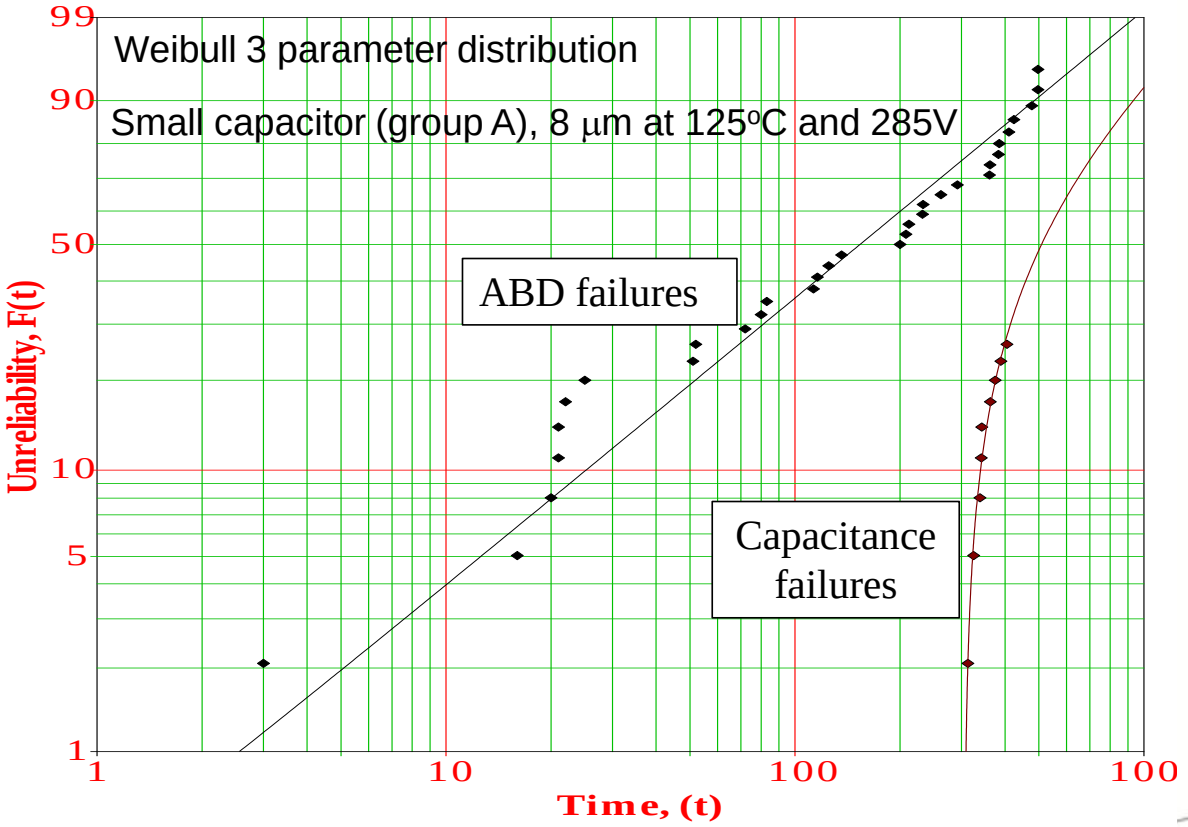
Test vehicle



Power Supply

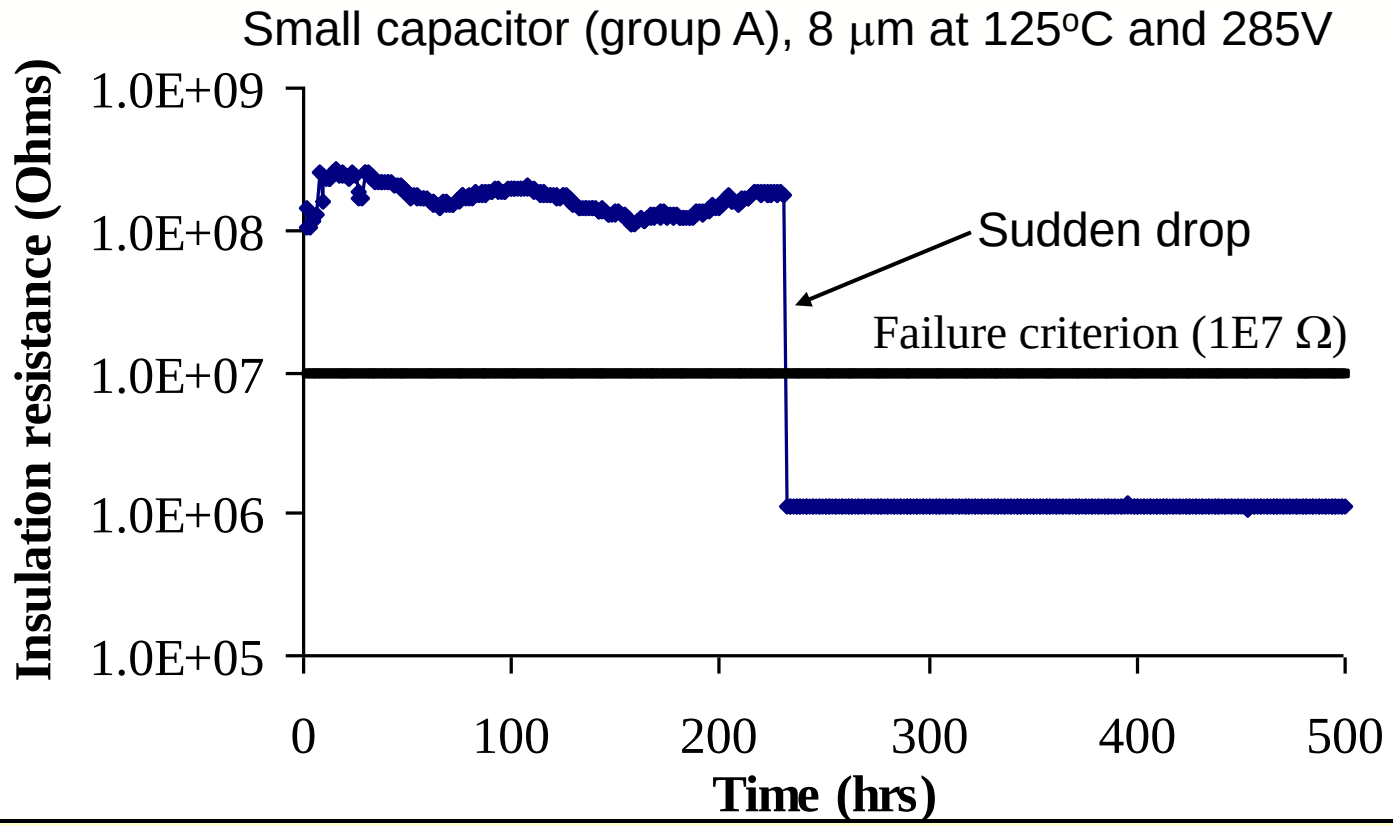
Failure Modes during HTOL Testing

- The failure modes observed were a:
  - Gradual decrease in capacitance
  - Sharp drop in insulation resistance implying ABD



The focus of this study is only avalanche breakdown (ABD) failures

Typical Plot of Insulation Resistance

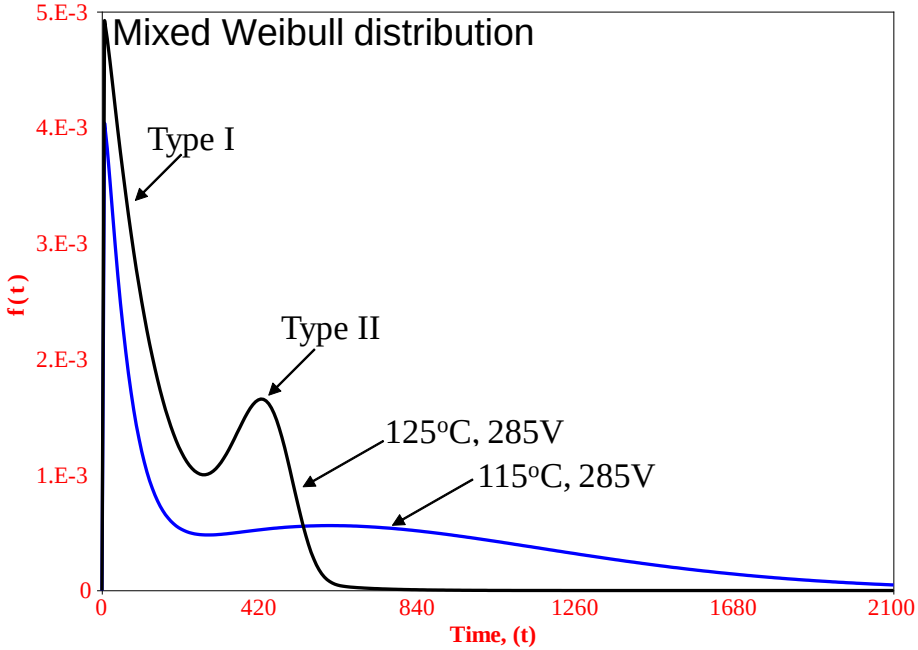


Since HTOL experiments were conducted under highly accelerated conditions, this failure mode may not take place under normal operating conditions

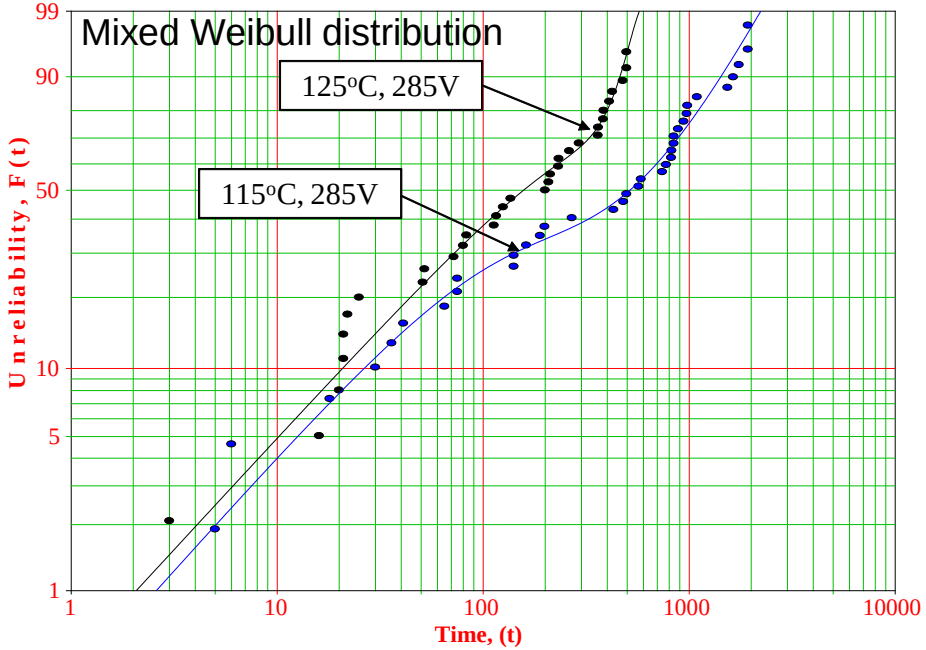
Effect of Temperature (115°C→125°C)

(285V, Small capacitors, 8 μm dielectric thickness)

Probability distribution function



Unreliability vs. time-to-failure



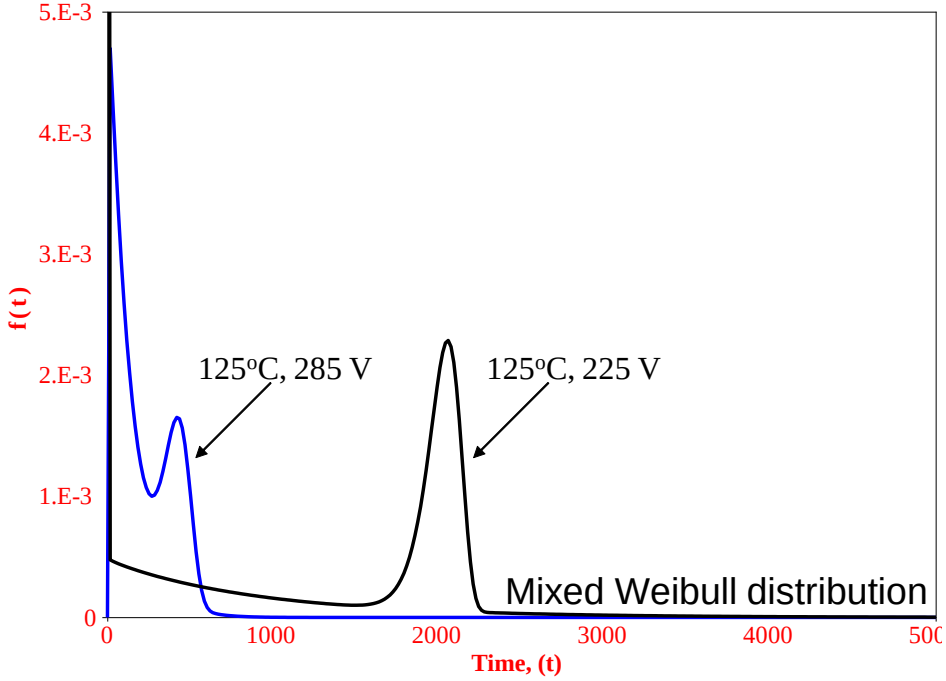
Aging condition	Test duration (hrs)	Failed	Survived		MTTF (hrs)	β	η	P
125°C and 285V	500	32	1	Type I	130	1.0	130	0.7
				Type II	413	6.0	444	0.3
115°C and 285V	2000	36	0	Type I	63	1.1	65	0.3
				Type II	871	1.8	979	0.7

Type I failures seems to be random in nature since the value of β is close to 1

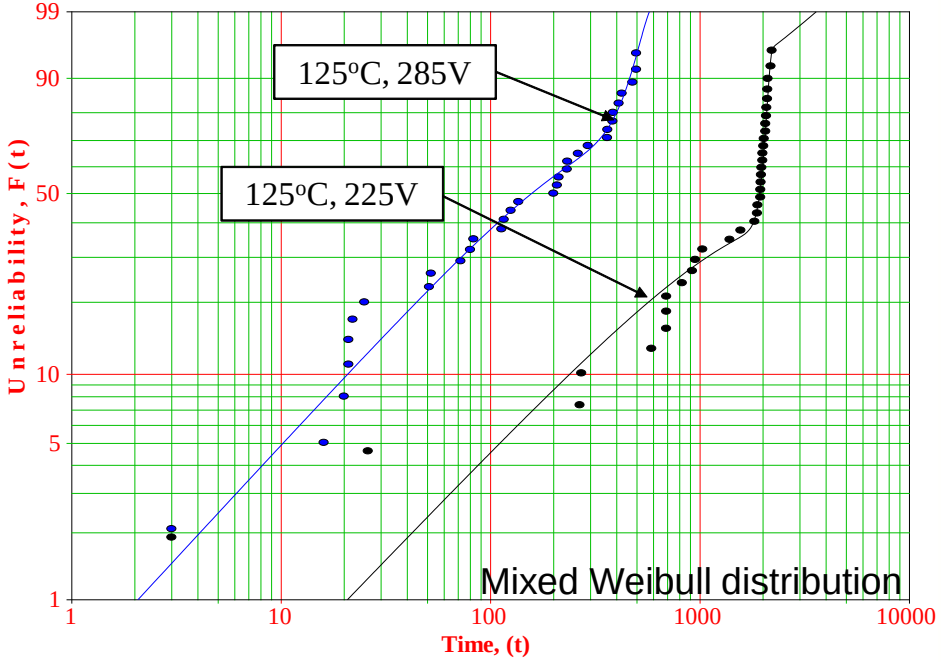
Effect of Voltage (225V→285V)

(125°C, Small capacitors, 8 μm dielectric thickness)

Probability distribution function



Unreliability vs. time-to-failure



Aging condition	Test duration (hrs)	Failed	Survived		MTTF (hrs)	β	η	P
125°C and **285V**	500	32	1	Type I	130	1.0	130	0.7
				Type II	413	6.0	444	0.3
125°C and **225V**	2300	35	1	Type I	935	1.0	935	0.4
				Type II	1996	22.0	2058	0.6

Constants of the Prokopowicz Model

- The constants of the Prokopowicz model were found:
  - E_a = 0.99 eV
  - n = 6.7
- The values of these constants (*n* and E_a)
  - depend only the material properties
  - does not depend on configuration
    - size of the capacitor
    - dielectric thickness.
- **The model can be used for any configuration of embedded capacitor (with the same material).**

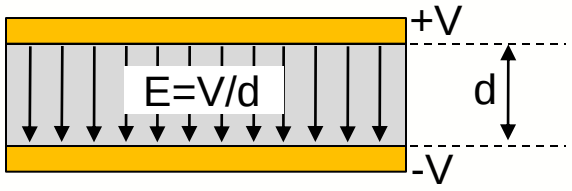
$$\left(\frac{t_1}{t_2}\right)_{Configuration\ A} = \left(\frac{t_1}{t_2}\right)_{Configuration\ B} = \text{.....} \left(\frac{t_1}{t_2}\right)_{Configuration\ n} = \left(\frac{V_2}{V_1}\right)^{6.7} \exp\left(\frac{0.99\,eV}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where t is the dielectric thickness and A is the area of the capacitor.

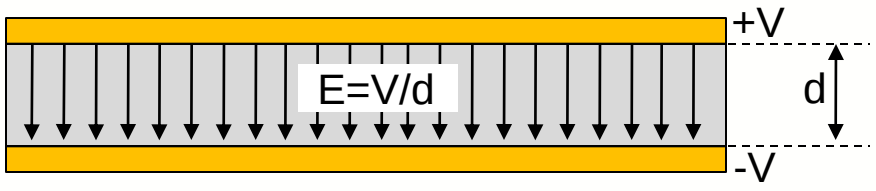
Effect of Area (0.026 in^2→0.19 in^2)

(125°C, 285 V, 8 μm dielectric thickness)

- All large capacitors failed within 10 hrs.
- Electric field experienced by the dielectric of small and large capacitor is same.



Group A



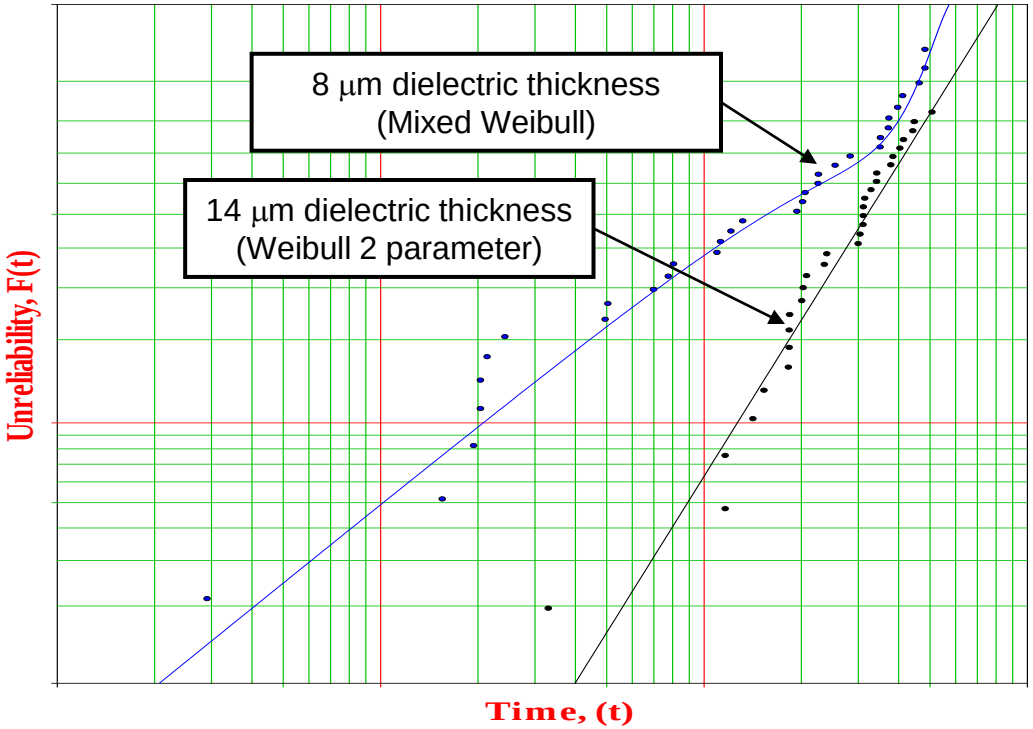
Group B

- A shorter time-to-failure of large capacitors implies that these failures are defect driven, whose probability increases with capacitor area.

Effect of Dielectric Thickness (8 μm → 14 μm)

(125°C, 285 V, small capacitors)

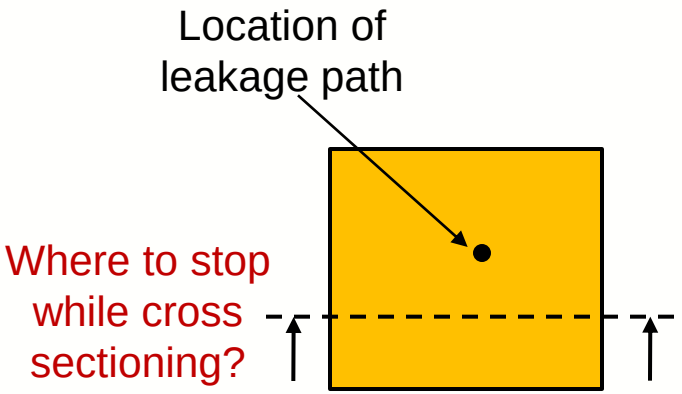
With an increase in the dielectric thickness, Type I failures disappeared.

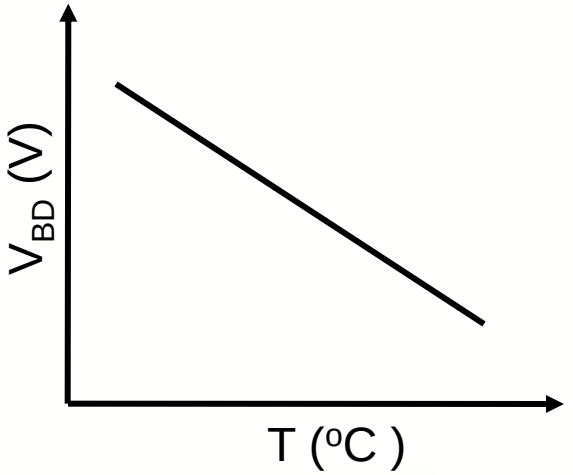


Aging condition	Test duration (hrs)	Failed	Survived		MTTF (hrs)	β	η	P
125°C and 285V **(8 μm)**	500	32	1	Type I	130	1.0	130	0.7
				Type II	413	6.0	444	0.3
125°C and 285V **(14 μm)**	526	30	6		341	2.0	383	

Failure Analysis

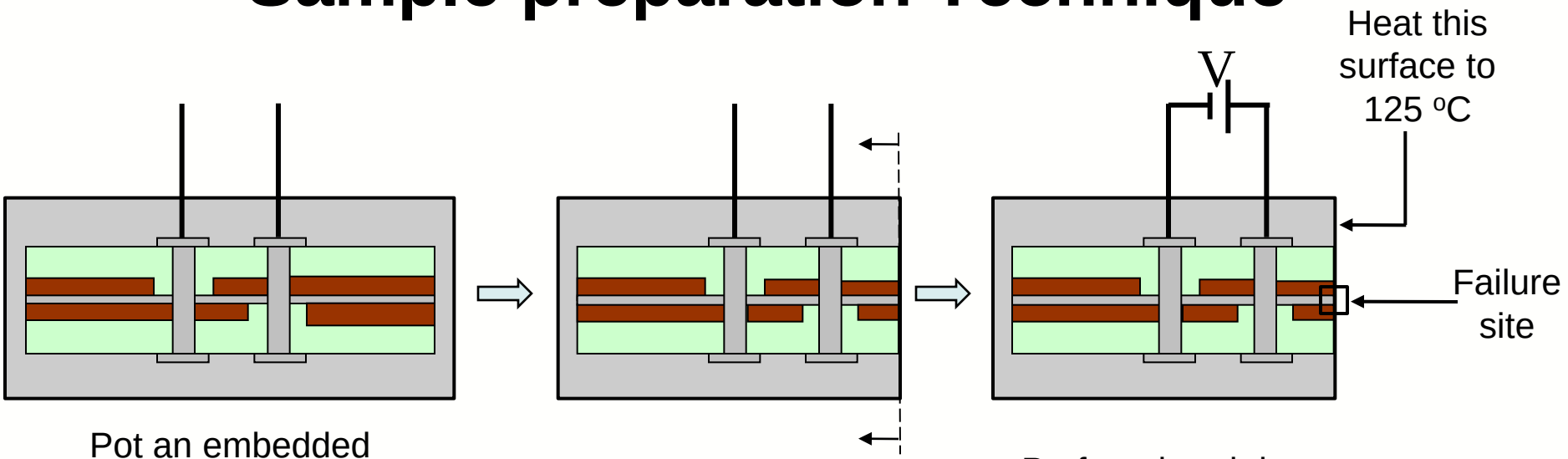
- Isolate a leakage path (~10^5 Ω) in a 4 layered PWB.
- Use of non-destructive techniques such as thermal imaging and SQUID (Superconducting Quantum Interference Device) microscopy can possibly be used to locate the failure site.
- However in this work a new technique was used to located the failure site:
  - similar failures were reproduced in a healthy capacitor at a predetermined failure site
  - The temperature dependent breakdown voltage (V_{BD}) property of this material was utilized[1].





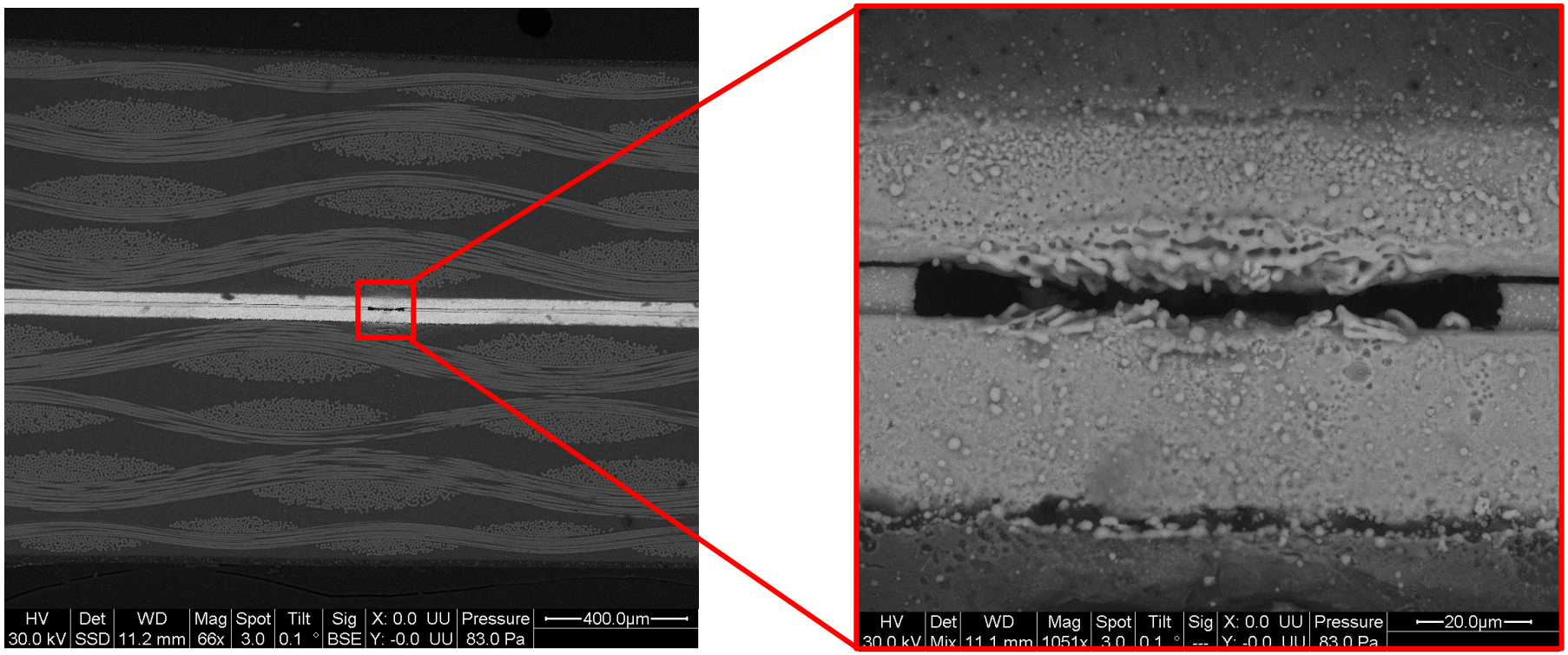
[1] M. Alam, M. H. Azarian, M. Osterman, and M. Pecht, "Reliability of Embedded Planar Capacitors under Temperature and Voltage Stress", *Capacitor and Resistor Technology Symposium*, Jacksonville, FL, 2009.

Sample preparation Technique



- The objective of fine polishing and etching was to reduce the number of defects created during grinding.
- The polished surface of the sample was heated to 125°C and the voltage between the capacitor plates was ramped from zero until the point of dielectric breakdown (V_{BD}).

Site of Dielectric Breakdown



- The failure site (dark in color) was hollow and the Cu plates melted and moved towards each other.
- The sequence of events that led to this failure is under investigation.

Conclusions And Future Work

Conclusions:

- HTOL experiments were used to model (using Prokopowicz equation) the time-to-failure as a result of avalanche breakdown in embedded capacitors.
- The model can be used for the qualification of embedded capacitors to precipitate defects resulting from the manufacturing process.
- A new failure analysis technique was developed that can be used to locate the site of avalanche breakdown in the dielectric.

Future Work:

- Conduct HTOL experiments at two additional stress levels to evaluate the values of constants of the Prokopowicz model with better confidence.
- Failures that are more representative of failures occurring during HTOL test will be reproduced and analyzed.