Industrial PCB Development using Embedded Passive & Active Discrete Chips Focused on Process and DfR

M. Brizoux, A. Grivon, W. C. Maia Filho, E. Monier-Vinard
Thales Corporate Services
Meudon-la-Forêt, France

J. Stahr, M. Morianz
AT&S
Leoben, Austria

Abstract
For several years, 3D-integration approaches have been explored to keep pace with the continuous trends towards electronics miniaturization and densification. Numerous technologies issued from various chip-, package- or board-level concepts can now be used and combined to achieve highly integrated "smart" systems. PCB embedding of passive and active devices is one of these advanced options with a strong potential : it enables a dramatic functionality increase while maintaining key PCB attributes of component and interconnects carrier. The presented paper will discuss some aspects of the PCB embedding technology developed in the frame of the HERMES project (High density integration by Embedding chips for Reduced size Modules and Electronic Systems). This European funded FP7 3 years research program targets to establish an industrial platform capable of producing PCBs with 2 layers of embedded components including large die sizes. The embedded PCBs manufactured will then be populated with external SMD components on both sides to constitute complex high-end integrated modules able to withstand conventional repair operations and ensuring a high reliability level. The work carried out will support the design and manufacturing of the various HERMES functional demonstrators for security, automotive and power module applications.

Key words : HDI (High-Density Interconnects), 3D packaging, PCB embedding, reliability, torsion

Introduction

The electronics industry is continuously following the trends towards increased density and complexity, searching for new interconnection and packaging solutions. Recently, several competitive packaging approaches have entered the evaluation and qualification stages to achieve 3D technologies [1] [2]. Chip embedding using advanced PCB processes and state-of-the-art PCB materials show very good potential to realize cost effective packages. This technology offers a new interconnect solution without wire bonding with improved thermal and electrical performance and the capability of die stacking.
Two main applications have been identified for chip embedding which fit in a good way to the capabilities of the technology : modules where several chips and passive components are embedded and silicon packages. Especially for silicon packages the stacking of the dies with the embedding method is an interesting feature requested from many semiconductor companies. In the HERMES project stacking of two dies will be driven to industrial level and up to four dies on development level.
The HERMES consortium focus on building a supply chain and industrialize the technology including reliability assessments on test vehicles. Fully functional demonstrators defined by the end users will be manufactured for process verification and product validation. Reliability is a key aspect for the embedding technology driven by the quality requirements of the automotive, semiconductor and security&communication industry. Test concepts will be developed for each application , because a test solution is fundamental to industrialize the embedding technology. Supply chain management starting at the silicon house followed by the back-end services to prepare the die for embedding followed by chip embedding, testing and ending at the OEM or silicon house is another big topic for the HERMES consortium.
This paper will focus on the activities carried out to characterize the thermal and thermo-mechanical behavior of embedded circuit boards. Electrical aspects such as cross talk, power integrity and control impedance which are also key considerations for the high-density HERMES technology will be addressed on in a future dedicated paper. The integration of dies and discrete passive chips inside a PCB build-up significantly impacts board stiffness and mechanical properties which in turn will affect solder joint reliability. In HERMES, an extensive work is conducted to understand these effects in the aim of establishing DfR (Design for Reliability) rules and optimize future embedded designs. The approach considered relies on FEA modeling supported by an experimental validation and in-depth physical property measurements. The modeling work targets to determine the stress and strain distribution within embedded structures including the incidence of critical variables such as die size and position in the stack-up. Simulation results will be calibrated through high-accuracy strain measurements under torsion using internal embedded gages in conjunction with conventional external 3-axis rosettes. The DfR rules resulting from this study will complement the other aspects investigated in the HERMES project (namely thermal and signal integrity performances) in order to produce highly functional and reliable modules using embedded PCB technology.

PCB embedding technology fundamentals

The constant need of consumer and telecom electronics for miniaturization drives the development of IC semi-conductor technologies for decades. For electronic components, this translates into a continuous evolution towards increased functionality in smaller form factor and finer pitch packages. To accommodate these always denser components, PCB technologies are also following a similar trends resulting in shrinking features as highlighted on figure 1. In this evolution, microvias have played a crucial role and have been a key enabling technology by significantly raising the achievable interconnect density level. Microvia is now a well established and mature technology commonly used in high-complexity and high-reliability designs. The next densification step is PCB embedding which relies on copper filled microvias to form the electrical connections to the embedded components. This 3D packaging technology has a strong potential to meet the needs of a large spectrum of applications (see figure 1 which compares the domains covered by various 3D technologies).

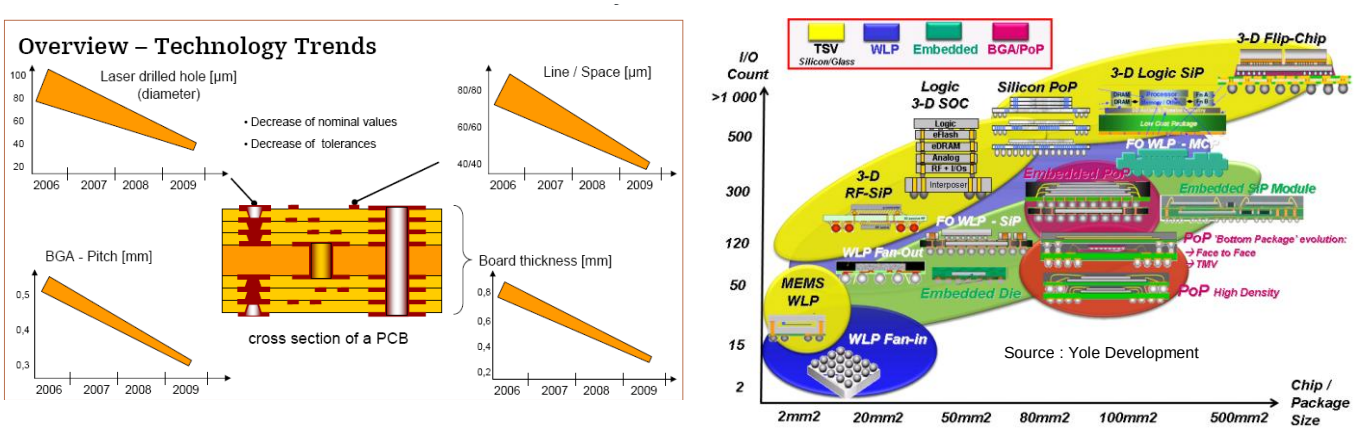


Figure 1 – PCB technology trends (left) and 3D packaging roadmap (right).

Compared to the widespread solder or wire bonding, filled microvias constitute a thermally and mechanically stable interconnect with improved thermal and electrical performances. This provides unique advantages for the PCB embedding technology.

Embedding technology process flows

Two basic process flows may be used to embed passive and active chips within a PCB : face-up and face-down. These 2 variants differentiate in the way of interconnecting the component with the outside world and use different materials and processes. An overview of the 2 approaches is given in figure 2.

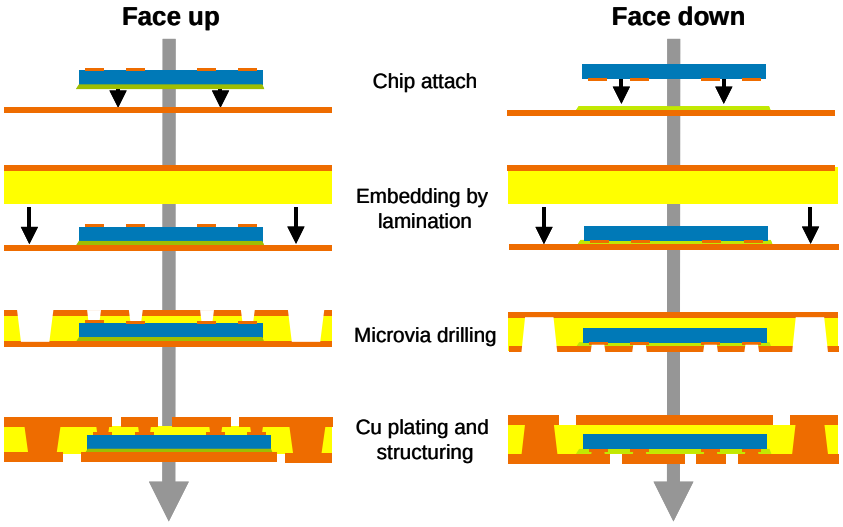


Figure 2 – PCB embedding process flows : face-up (left) and face-down (right).

In a face-up process, the component is placed on a carrier material and the contact pads of the component can be seen after assembly. This approach offers some very good thermal properties and is well suited for power component embedding. Processing limitations are encountered when trying to embed components with variable thicknesses. After embedding, the

dielectric thickness between the component surface and the outer copper surface is not constant, which challenges the subsequent microvia laser drilling and copper plating especially when via filling is needed.
In a face-down process, the component is assembled with the component image to the carrier material. Normally, a screen printed electrically non-conductive adhesive polymer is used to fix the component on the carrier. This method offers several advantages: a good thickness control of the dielectric material between the component and the carrier and very good registration accuracy at the assembly process. The reason for the improved registration capability comes from the fact that the camera of the assembly machine can see the image of the component and therefore can registrate to it before assembly is done. In the face up technology the camera registrates to the contour of the component.
Using the face-down technology, several components with different thicknesses can be embedded in a FR-4 core. The prepregs used for embedding are cut out to create cavities around components. The prepregs with the openings are stacked to the height of the component and topped with a prepreg without openings. The embedding with different thickness is easy to do by opening the dielectric material to the individual height of the component which can typically vary from 100 to 350 µm.
The constituted embedded cores can then be used as standard innerlayer cores and included in a PCB multilayer construction. External SMD components can then be assembled on both sides of the embedded PCB to constitute very high-density modules/assemblies (see figure 3).

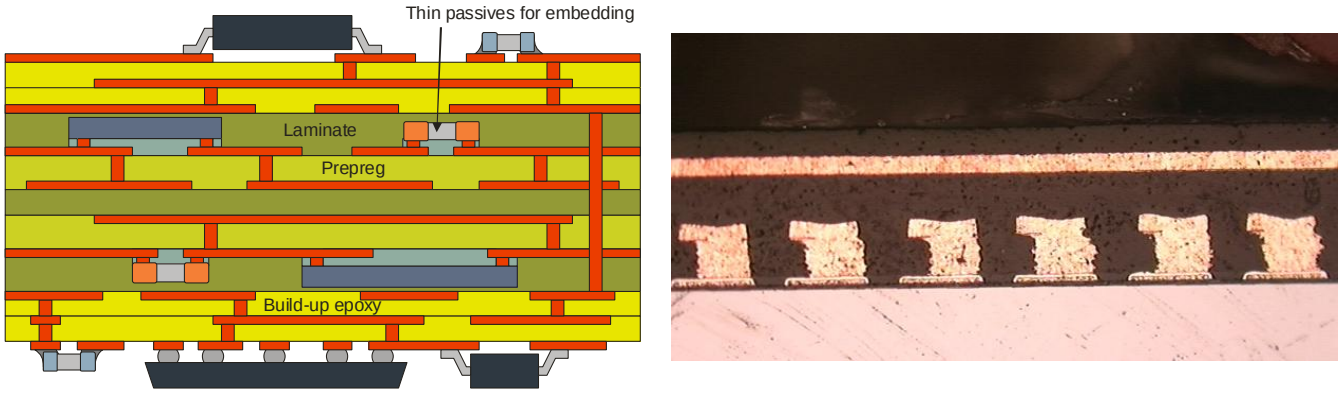


Figure 3 – Example of embedded PCBs with 2 embedded cores and external assembled components (left). Cross-sectional close-up view of an embedded chip (pad pitch : 100 µm, target land at chip : 65 µm diameter)

Embedding process prerequisites : silicon wafer and passive chips preparation treatments
Several preparation operations are needed to convert active dies into an embeddable form. First, the conventional Al die pads need to be coated with a Cu finish to interconnect them with laser drilled PCB microvias. A copper die pad metallization of 5µm thickness is typically used.
In most cases, the die connection pitch has also to be adapted to the PCB scale. The method used is to apply a redistribution layer (RDL) which enables to relocate the original die pads at an expanded pitch. The RDL involves the addition of a polyimide based dielectric material which can be found in around 70% of the WL-CSP packages. The RDL process is done at the wafer level and the interconnect pads are connected by micro via to the redistribution layer. The possible RDL ,options are shown on figure 4. On this layer the routing is done to distribute the I/O pads all over the chip area on a grid with a minimum pitch of 225µm. On this grid size one line can be routed through. The target design rules for industrialization will be 25 µm line and space and the pad size for the micro via interconnection has to be 150µm.

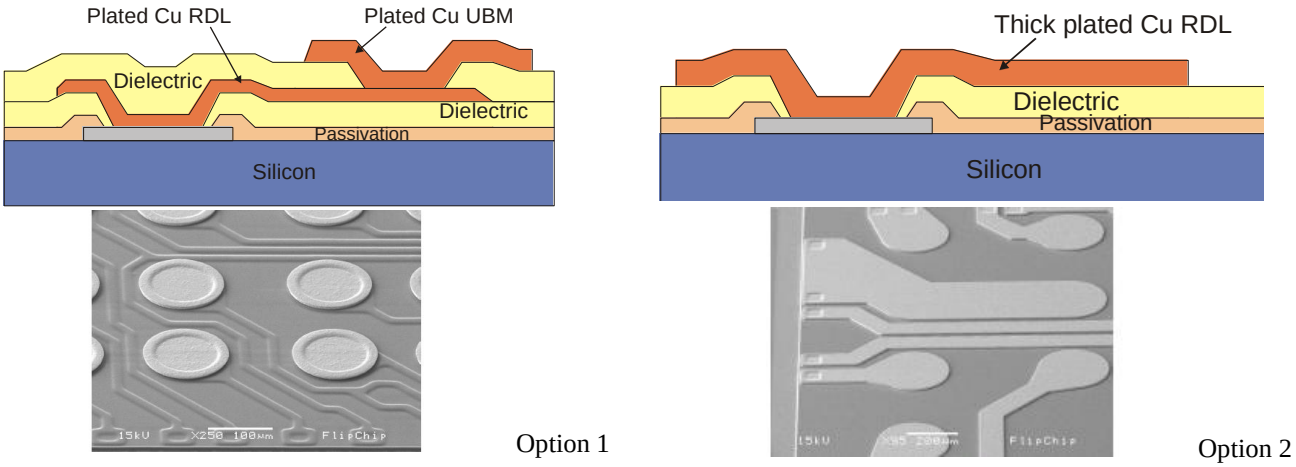


Figure 4 – RDL options.

Usually, the option 1 is preferred as it provides higher routing density through smaller line widths and capture pads on the redistribution layer and protects the RDL layer against handling issues. Option 2 is realized with fewer process steps and hence can be used as a cost-effective alternative for lower I/O count dies. Higher I/O count dies do not comply with this option because of increased registration issues. The minimum pitch manageable appears to be 100 µm when a single row of pads is connected in a layer.

The next step needed to prepare a die before PCB embedding is wafer thinning. Generally, a coarse grinding is done followed by a fine grinding process to release stresses from the wafer and prevent silicon micro cracks. Typically, a thickness in the range of 100 to 150µm covers most cases, but special applications such as power MOSFETs may call for 70µm to reduce the thermal resistance. 70µm is considered as the current minimum wafer thickness achievable on an industrial level.

Wafer dicing and taping are the last two operations that are needed to get a component that can be assembled with a high speed assembly machine. The taping process of thin silicon dies in a pocket tape can be done with remarkably good yields for small components, but becomes more challenging for die sizes larger than 8mm x 8mm..

All the required preparation steps from wafer Cu plating to taping can be handled by FCI (Flip-Chip International) which is an industrial back-end supplier supporting the HERMES project [3] (see figure 5).

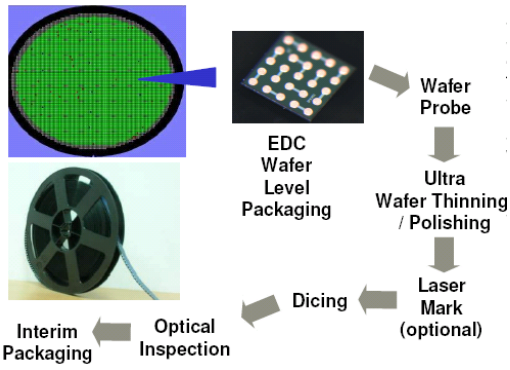


Figure 5 – Process flow of the required operations before embedding from wafer to packing.

Investments for production

Chip embedding in a PCB is a major breakthrough which dramatically increases the added-value of the PCB. To achieve high production yields and competitive costing, IC semiconductor practices and culture have to be introduced together with highly capable machines and processes. Clean room requirements and ESD compliance are some of the basic requirements that have been implemented in the industrialization unit at AT&S in the frame of the HERMES project. In addition, the site has been completely re-configured in order to ensure a damage free handling along the whole production line. The plant is no more a conventional PCB factory, but rather an embedded fab.

One of the basis in the embedding technology for discrete components is the assembly to a carrier material which can be an imaged FR-4 core or a copper foil. In the beginning of chip embedding, this task has been accomplished by accurate die bonders, but these equipment do not accept PCB standard large format panels like 18"x 24". Large panel capability is a key requirement to keep the costs down. Latest SMD placement machines can fulfill high-accuracy and high-speed assembly as well as handle large panels. One assembly head can run 20000 components per hour which can give a capacity of more than 80000 components an hour with a fully populated 4-head system. Looking at HERMES design rules, the assembly tolerance is set to +/- 10 µm. An example of high-speed assembly machine used for PCB embedding is shown on figure 6.

Figure 6 – SEAS SIPLACE X2 high-speed assembly machine

Chip embedding technology can be viewed as a high-density packaging technology – as a combination of a interconnect system and a package. In this area, advanced design rules of 25µm line and space are requested, with a projection down to 15µm. Among other technical objectives (refer to figure 7), HERMES targets the industrialization of a 25µm technology which is well beyond typical PCB manufacturing capabilities.

Objective	Target for production	Target for prototype
Die pitch	125 µm peripheral 250 µm area array	60 µm peripheral
Manufacturing panel size	24" x 18"	4"x4" - 18" x 12"
Line/space for fine line interconnect	25 µm ± 4 µm	15 µm ± 3 µm
Component placement speed	10.000 / hr	1.000 / hr
Chip placement accuracy	15 µm @ 3σ	7.5 µm @ 3σ
Thermal resistance for single chip power package	10 K/Watt @ 125°C junction temperature	5 K/Watt @ 150°C junction temperature
High frequency insertion loss for 1 connection to a chip pad	0.1 dB @ 10 GHz	0.1 dB @ 10 GHz
Multilevel stacking in production	2	4

Figure 7 – Overview of HERMES main technical objectives.

Achieving such very fine features on large panels require significant investments and new approaches. In HERMES, a semi-additive plating process based on an adaptive laser direct imaging (LDI) and ultra-thin 2µm copper foils has been implemented. Although LDI is already industrialized for some years, its usage in conjunction with a semi-additive process necessitated intensive development activities. In addition, microvia filling combined with a semi-additive patterning process brings additional challenges in fulfilling a good uniformity of the plated structures. In HERMES, this is overcome by a new single board plater machinery concept that targets a copper thickness tolerance of +/- 15% all over the panel.

Testability

PCB embedding deeply impacts the conventional supply chain and poses new testability challenges. Process control and high yields are the fundaments to ensure a good product quality, but functionality testing and good test coverage are mandatory requirements for complex assemblies. This is currently managed by upstream test strategies. Usually today, component functionality and performances are tested by component manufacturers. Some of these tests are very complex and performed at the wafer level at hot and cold temperatures. Other functional tests are done by the assembler on fully populated boards. Switching to an embedding process flow has a strong effect on testability because part of these tests have to be integrated at

the PCB level (see figure 8). This would mean to add new testing methodologies (like ICT, flying probe, boundary scan) and know-how at the PCB manufacturing stage.

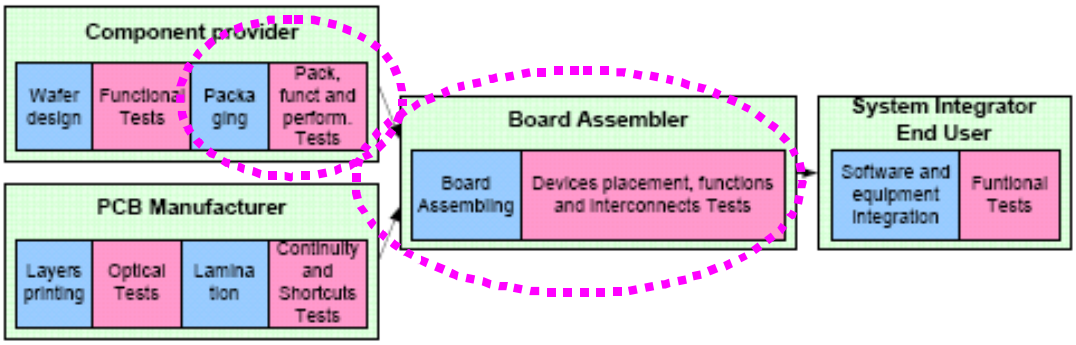


Figure 8 – Conventional test flow from wafer to SMT assembly.

For simple components or when all components are delivered from a single source, a model similar to the current one may be however used to manage the full functional testing. Modules with passive components (capacitors, resistors, diodes) only can also be accommodated by latest advanced PCB testers, but the whole testing concept for actives and passives is not implemented today.
HERMES drives the development of the test concept for the realized embedded application forward. The first step is the definition of test levels and the gates for testing. The first gate will be most probably after finishing the embedded core. In this stage, the embedded components can be contacted will all pins and a test with a good functional coverage could be done.
The development of the test concept will need time there are technical issues as well as a necessary transfer of know-how necessary. The management of the know-how transfer and distribution in this new supply chain will be the biggest challenge.

PCB embedding technology design rules
To support a full industrialization, the HERMES project puts a lot of efforts in defining design rules for PCB embedding technology. To accommodate the various needs of future applications, the following aspects will be thoroughly investigated:

- Thermal management
- Signal integrity for high frequency transmissions
- Thermo-mechanical behavior of embedded boards
- Reliability

In the following paragraphs, a partial overview of the thermal and thermo-mechanical activities is presented.

Thermal aspects
PCB embedding technology is a disruptive high-density technology which raises new significant thermal management challenges by concentrating heat in the PCB inner layers.

Thermally enhanced packages with bottom exposed die paddle (such as QFNs) induce increased temperatures near the board surface. The adoption of embedded chips in future designs will further increases the thermal constraints at the PCB heart and exacerbate the need of adequate design.

Considering the kind of dies to embed, the required thermal performances for the HERMES technology are very ambitious. As an example, for power module applications, the junction to ambient thermal resistance is expected to have to be limited to around 10K/W at 125°C junction temperature for reliability purpose. Assuming a free natural convection cooling mode at an ambient temperature of 85°C and a junction temperature to keep below 125°C, this implies that the maximum power dissipation allowed, using Fourier relationship ($P = \frac{\Delta T}{Rth}$), has to be close to 4W for a single embedded chip.

To address the specific concerns related to PCB embedding technology, a fully detailed thermal model has been built from a CFD simulation tool. An example of investigated construction is shown on the picture below.

The basic concept is to embed a thin chips, less than 150µm, into the laminated build-up layers of less than 600µm called the "Core layer", then integrated this one into a classic multilayer electronic board with SMD components on the external surfaces

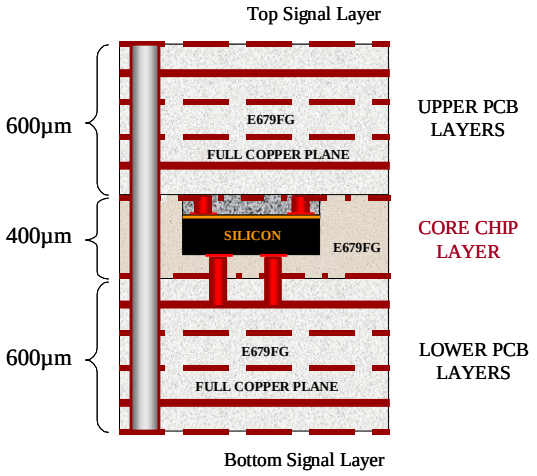
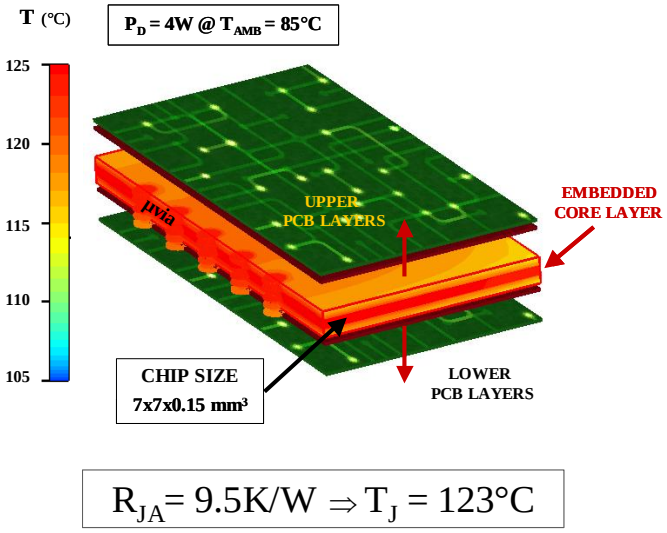


Figure 9 – Example of modelled embedded structure (12-layer board layout).

The first simulation results has highlighted that the thermal behaviour of an embedded chip is mainly depending of the full copper layers of the board. Several layer constitutions have been tested and show that an asymptotic performance value is quickly achieved with 4 full copper layers of 50µm thickness.

Early results also indicate that the cooling of a single large chip size, such as 10x10mm^2 is likely to be achieved as shown on figure 10.



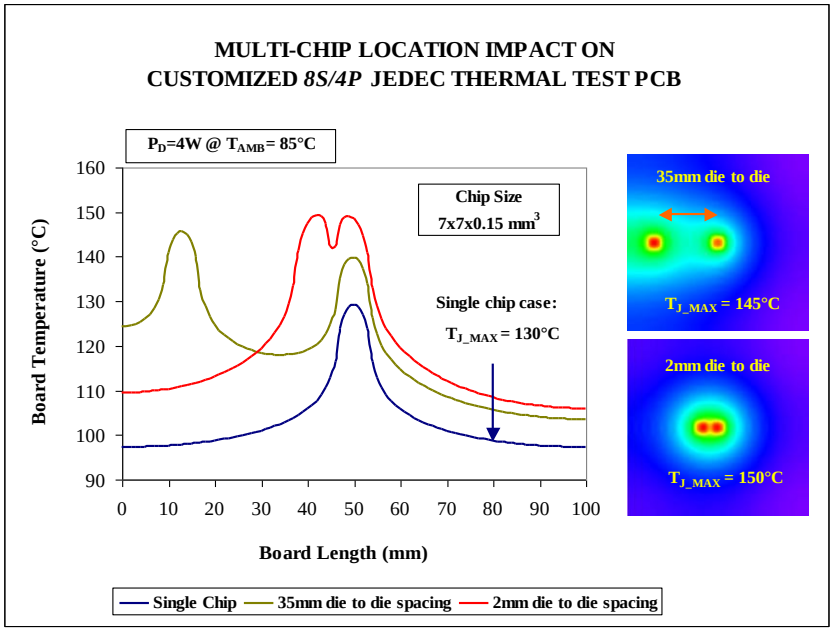
		CHIP AREA LAYERS LAYOUT				CHIP AREA THERMAL BEHAVIOUR			
Layer Number	Layer Name	Function	Material	Thick. µm	Copper coverage	Average Temp (K)	Chip heat exchange (W)	Heat cooling paths	
1	TOP	CONDUCTOR	COPPER	50	10%	108	0.05	1.1%	
2		DIELECTRIC	E679FG	75		108	0.06	0.0%	
3	INT2	CONDUCTOR	COPPER	50	100%	108	0.50	11.1%	
4		DIELECTRIC	E679FG	75		109	0.50	0.0%	
5	INT3	CONDUCTOR	COPPER	35	10%	109	0.54	1.1%	43%
6		DIELECTRIC	E679FG	75		110	0.54	0.1%	
7	INT4	CONDUCTOR	COPPER	35	10%	110	0.60	1.4%	
8		DIELECTRIC	E679FG	75		111	0.61	0.1%	
9	INT5	CONDUCTOR	COPPER	50	100%	111	1.74	28.3%	
10		DIELECTRIC	E679FG	75		113	1.75	0.3%	
11	INT6	CONDUCTOR	COPPER	35	0%	116	1.76	0.2%	
12		DIELECTRIC	GLUE	75		118	1.79	0.8%	
13		CONDUCTOR	CHIP COPPER	20	0%	120	1.80	0.3%	
14		CHIP	SI	150		123	4.00	3.2%	6%
15		CONDUCTOR	CHIP COPPER	20	0%	120	2.07	0.3%	
16		DIELECTRIC	E679FG	75		118	2.06	0.8%	
17	INT7	CONDUCTOR	COPPER	35	0%	116	2.03	0.2%	
18		DIELECTRIC	E679FG	75		114	2.02	0.3%	
19	INT8	CONDUCTOR	COPPER	50	100%	113	2.00	32.2%	
20		DIELECTRIC	E679FG	75		112	0.72	0.1%	
21	INT9	CONDUCTOR	COPPER	35	10%	112	0.71	1.7%	
22		DIELECTRIC	E679FG	75		111	0.65	0.1%	
23	INT12	CONDUCTOR	COPPER	35	10%	110	0.64	1.3%	50%
24		DIELECTRIC	E679FG	75		110	0.59	0.0%	
25	INT13	CONDUCTOR	COPPER	50	100%	109	0.59	13.2%	
26		DIELECTRIC	E679FG	75		109	0.06	0.0%	
27	BOT	CONDUCTOR	COPPER	50	10%	109	0.06	1.3%	
				1600					

Figure 10 – Embedded chip thermal behavior

For smaller chip sizes, temperature will exceed 125°C without a significant limitation of its power dissipation P_D <<4W.

In order to allow electronic designers to investigate the limits of the power dissipation, another analytical model has been defined to integrate the incidence of the chip location into the board, as well as the thermal interactions with other chips or SMD components.

In order to allow the electronic designer to quickly investigate the limits of the power dissipation, depending of the chip location into the board, as well as the chip thermal interactions with other chips or SMD components, an analytical model has been defined**.**



ANALYTIC APPROACH

This one is based on a symmetric board layout hypothesis and use the heat equation solution for a source on an orthotropic substrate

This approach offers the possibility to quickly define, at an early design stage, the most appropriate PCB layer arrangement and chip placement according to its dissipation for harsh environment, such as the cases describe in the figure 11

Figure 11 – Multi-chip thermal optimization with die-to-die spacing of 35mm and 2mm.

So the final project design validation, using the full detailed geometries of the chip and PCB layers will done only on few relevant cases.

Therefore, an experimental validation using standard JEDEC JESD51 methodologies will be also performed to improve the analytic model and get more accurate predictions of the thermal behaviour in the chip area.

This standard provides a set of guidelines to design thermal test board and to perform their experiment widely used by component manufacturers.

To demonstrate the HERMES thermal performance benefits, an analysis was leaded on a JEDEC “high conductivity” test board, called 2s2p.

The 2s2p is a 4” test board, Figure 12, which is formed by embedding two 35µm copper planes (2p) in the PCB, while the finish thickness is 1.60 mm.

The same approach will be used for embedded chips..

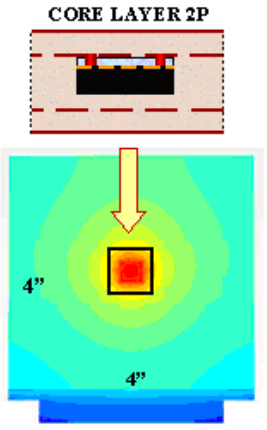


Figure 12. JEDEC “high conductivity” test board

For instance, the thermal resistance junction to ambient of an embedded chip of 10x10mm^2 in a 2s2p board is below to 15K/W which can be compared to a large thermal enhanced BGA package of 27x27mm^2 using an internal copper heat sink.
In summary, a definition of some design rules for the use of embedded chip has been established and a behavioral model allows to check a chip cooling at an early stage of the design.

Thermo-mechanical evaluation

A significant portion of the HERMES project is devoted to the mechanical and thermo-mechanical assessment of embedded PCBs. The final objectives are to define robust design rules ensuring a consistent reliability level for a variety of applications. To reach these goals, the following methodology has been adopted :

- Develop a generic strain distribution model
- Validate the model through an experimental test program
- Measure the reliability of embedded constructions using an optimized design

For a maximum model consistency, a special care has been brought to the experimental part by including detailed PCB material characterizations as well as extensive measurements on dedicated test vehicles. The methodology used (illustrated on figure 13) combines finite element analysis (FEA), strain gage measurements and torsion tests.

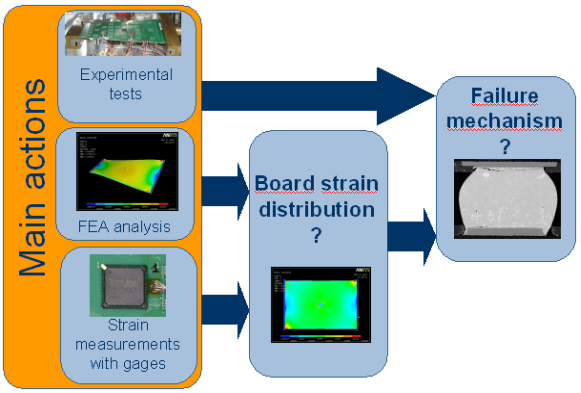


Figure 13 - Schematic view of the test program.

In this paper, an overview of the preliminary activities is presented, namely material characterizations performed for FEA and the feasibility of strain gages integration in the board.

PCB material physical property measurements

FEA simulations require basic mechanical properties like Young modulus, coefficient of thermal expansion and Poisson ratio. Data supplied by PCB base material thermo-mechanical properties supplied by laminate manufacturers are mostly useless, as measurements are performed on simple constructions which do not reflect modern multilayer PCBs. As an example, 8 plies of thick 7628 pre-pregs are often used to simulate a 1.6mm PCB, while multilayer boards found in high-end applications routinely comprise of a minimum of 16 plies with a variety of resin contents and thicknesses. Previous work has outlined the necessity of performing actual measurements on representative PCB build-ups to get consistent results as well as the strong incidence of the resin content on the board thermo-mechanical behavior [4].

Based on this essential background, a set of thermo-mechanical measurements has been performed using a comprehensive test program including 46 PCB constructions. The measurements have been done on 10mm x 100mm PCB samples without internal copper layer (see figure hereafter). Previous work has indeed evidenced that an homogeneous copper charge has very little influence on the elastic behavior of the board. For each considered PCB build-up, 10 samples have been manufactured to increase consistency and take possible result variability into account.

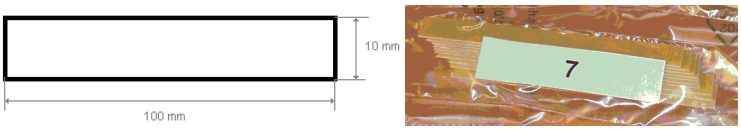


Figure 14 – Schema of the sample (left) and example of a package of samples #7 (right).

Test samples have been produced with 2 halogen-free epoxy base materials to characterize the following features :

1. Resin-content. Measurements have been carried out by Thermo-Gravimetric Analysis (TGA) using a Thermo-Microbalance with a resolution of 1µg under pure gas atmosphere from ambient temperature up to 800°C.
2. CTE (in-plane and in the Z-axis). This key characteristics is obtained by Thermo-Mechanical Analysis (TMA) and usually greatly differ from values supplied in base material datasheets.
3. Elastic modulus. It has been determined by Dynamic Mechanical Analysis (DMA) in the –60°C / +260°C temperature range at three different frequencies. For samples thinner than 200µm, traction tests have been used whereas bending tests have been applied on thicker samples. An example of test results is shown below. Two observations can be made : the drop of dynamic elastic modulus occurring at the material glass transition temperature (Tg) and the stability of the elastic modulus in frequency for temperatures below Tg.

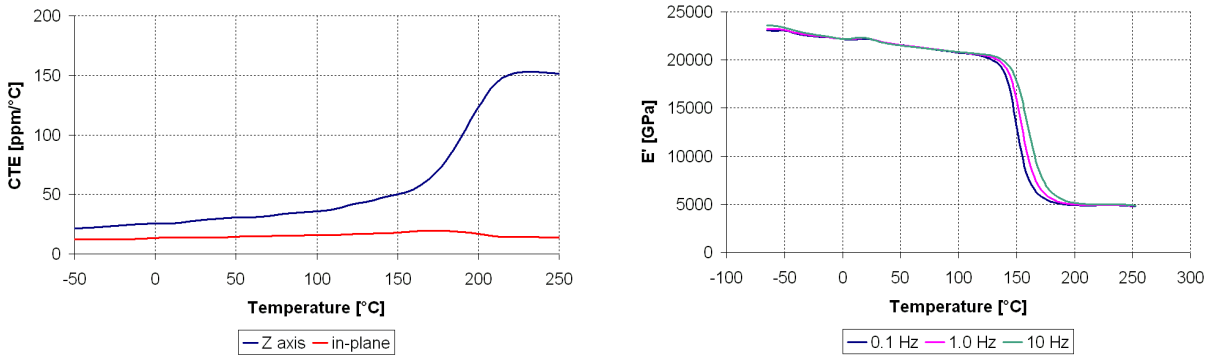


Figure 15 – Examples of experimental TMA (left) and DMA (right) curves.

PCB strain characterization

A comprehensive test program involving multiple stack-up configurations has been built to experimentally characterize the effects of embedded components on the mechanical behavior of the board. This program relies on dedicated test vehicle boards including embedded components and strain gages. The build-up constructions used are fully consistent with the ones used in the material characterization study. Due to the impossibility of assembling both silicon dies and strain gages on the same layer, 5 PCB constructions have been considered for this study (see figure 16).

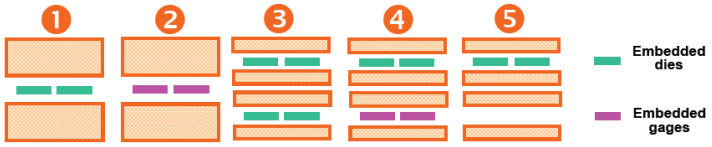


Figure 16 – Overview of the 5 types of embedded structures.

Additional strain gages bonded on the external PCB sides will be also used to cross-correlate the internal measurements and will enable to calibrate the finite element models.

On the embedded layers of the test vehicle boards, 3 types of dies and 4 types of passive chips will be assembled :

- Dies of 10 x 10 mm²; 5 x 5 mm² and 3 x 3 mm²
- Resistors and capacitors in 0201 and 0402 case sizes (R0201, R0402, C0201, C0402)

The silicon dies include daisy-chain circuits for electrical continuous monitoring during the tests to ensure the integrity of the interconnections in the embedded layer. The density of interconnections between the embedded silicon die and the board, which is critical for flip-chip assemblies, will be also evaluated using two die configurations : design 1 with a full matrix of interconnections; design 2 with interconnections only on the periphery of the die.

The test boards have been designed to comply with a torsion test methodology : dimensions have been set to 260 x 125 mm² and embedded components have been placed within the homogeneous strain area in the central zone. Figure 17 shows the embedded layer design and the embedded component distribution.

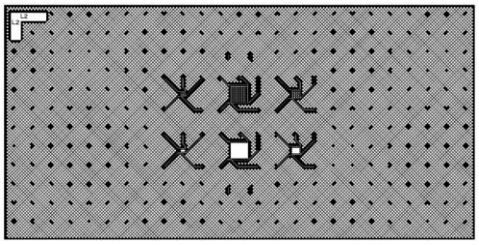


Figure 17 – Embedded layer lay-out.

Special development was done for strain measurements in the board using embedded strain gages. Firstly, an elementary component including the strain gage and the associated measurement circuit was defined. Figure 18 shows the schematic view of this elementary component and its cross-section analysis. The strain gage is a 3-axis rosette consisting of 3 strain gages with an active length of 1.6mm placed under three different orientations. Small sized gages have been selected to avoid

the effects of the strain gradient on measurements. The combination of the three measured values allows to calculate the total strain and its direction. Secondly, strategic points were defined on the test vehicle for strain characterization. The objective is to give sufficient data to correlate experimental results with simulations. In total, 7 strain gages will be embedded in each board.

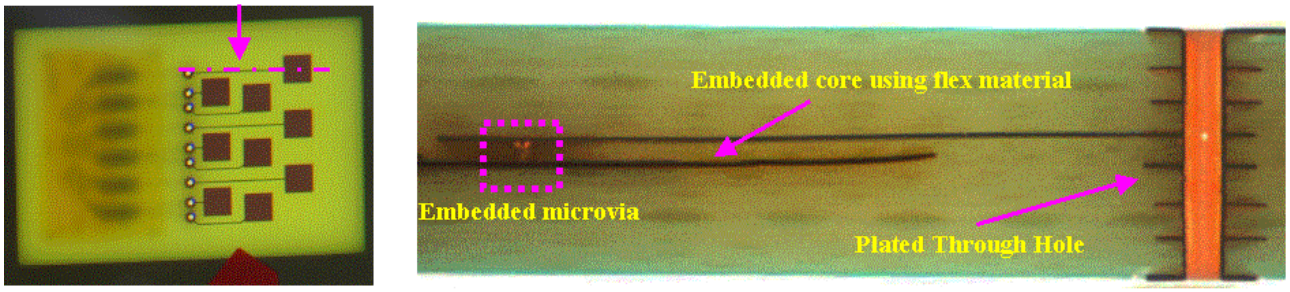


Figure 18 – Strain measurement circuit surface view (left) and cross-sectional view (right)

In a previous study, a methodology based on strain measurements under torsion testing has been developed to characterize the thermo-mechanical behavior of electronic assemblies. This methodology can be used to simulate thermo-cycling stresses and evaluate the reliability of solder joints. For embedding technology, it will enable to analyze the mechanical board response to different stresses. Varying the torsion angle will generate controlled deformations and in particular induce a sliding effect between the various PCB inner layers. Varying the dwell time will allow creep evaluations. In addition, the torsion test bench is equipped with a thermal chamber which brings the possibility to perform torsion tests under temperature, up to 125°C. This capability will be exploited to characterize the effect of the CTE mismatch of the different elements constitutive of an embedded board.

Embedded strain measurement validation

Before manufacturing the test vehicle boards, a preliminary test has been carried out to validate the embedding process for strain gages. A 3-axis rosette strain gage has been embedded in a PCB and its response to a torsion profile has been analyzed (see figure 19). This experiment enabled to validate the process, taking into account the following :

- The measured strain magnitude has been found consistent with previous studies using torsion test
- The creep observed when torsion is applied lies in the same order of magnitude as the one measured by strain gages assembled on the external sides of the board.
- A good reproducibility has been noted during several torsion cycles.
- Residual strain at the end of the cycle is normal and is related to torsion test bench backlash.

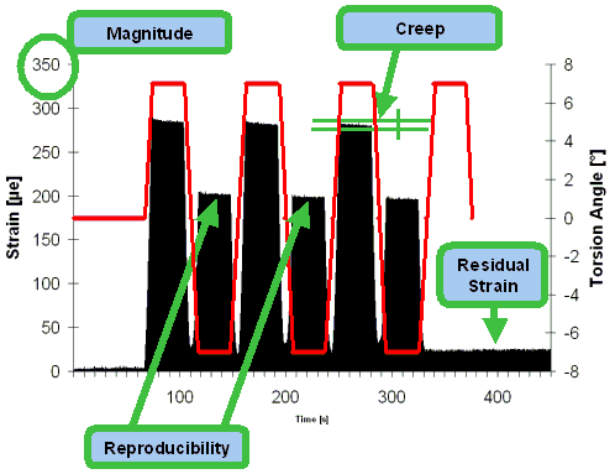


Figure 19 – Demonstration of strain measures using embedded strain gages

The possibility of measuring strain using embedded gages has been demonstrated, which will provide an accurate in-situ strain measurement inside a PCB build-up. The test vehicles needed for the thermo-mechanical characterization program are currently under manufacturing. It represents more than 200 boards, including 5 design variants and 28 build-up structures with silicon dies, passive chips and strain gage rosettes.

Conclusions

The chip embedding technology has already a long development story documented with patents from General Electric in the 80s. A lot of efforts have been done to bring the embedding technology to the market. With the increasing interest from several business branches, enough potential has been seen to create the Hermes consortium. This consortium forms a supply-chain to develop the chip embedding technology – starting with the bare wafer and ending in an embedded application. The clear target of the project is to bring the technology to industrialization. Beside the consortium, an early adopter group was founded to enlarge the footprint for the introduction of the technology. The members of the early adopters group benefit from the development results in the consortium to develop their applications for a later industrialization. The development of design rules their standardization and the development of EDA design tools for the embedding technology is another topic where the early adopters group will contribute with their input. Two important application areas can be seen – embedded packages for silicon dies and embedded modules with some dies and passive components. 3D packaging is offered by this technology either by assembling of components on the outer layers or by chip stacking.

After 1,5 years duration of the project, most of the processes for embedding are evaluated by test vehicles showing the embedding capability for dies up to 10 by 10 mm and ultra fine line technology down to 25 µm line and space. Functional demonstrators are in progress to show the full capability of the chip embedding technology .

Embedding active and passive components in a multilayer PCB with external packages assembled on both PCB sides is an extremely ambitious goal dictated by the needs of upcoming portable and AHP products. More than ever, robust design rules for reliability and manufacturing (DfR & DfM) are very critical and a paramount necessity in order to achieve high yields and technical performances. In this paper, the methodologies used to establish design rules in domains like thermo-mechanical fatigue and thermal management are highlighted. These methodologies are based on a large experimental part involving several dedicated test vehicles in conjunction with simulation.

The design rules will take into account base material properties and PCB architectures up to 3+ 8+3 layers with one and two layers of embedded components assembled according to a face-down process flow.

Signal integrity for high-speed digital transmissions is investigated under another on-going study which is not presented here.

Acknowledgments

The authors would like to express their thanks to the European Commission for their funding of the HERMES project (FP7-ICT-224611).

References

[1] Baik-Woo et al., "Technologies for convergent microelectronic systems", *Article CircuiTree*, January 2008.

[2] L. Boettcher et al., "Chip Embedding by Chip in Polymer Technology", *Proceedings of IMAPS Device Packaging Conference*, Scottsdale, USA, March 2008.

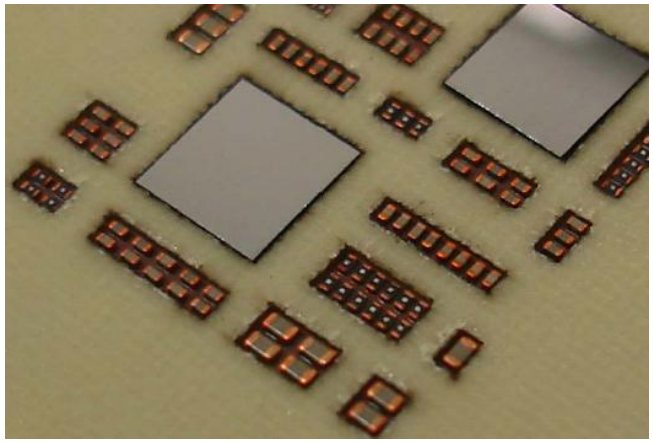
[3] T. Tessier et al., "Infrastructure Building for Embedded Die Printed Wiring Board Applications", *Proceedings of 5th International Wafer-Level Packaging Conference*, San Jose, USA, October 2008.

[4] W. C. Maia Filho et al., "Influence of build-up construction and resin-content on mechanical behavior of printed circuit boards", *Proceedings of 10th IEEE Eurosime, International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems*, Delft, Netherlands, April 2009.

Industrial PCB Development Using

Embedded Passive & Active Discrete Chips

Focused on Process and DfR



Outline

- Introduction
  - 3D Packaging context
- Chip embedding technology features
- Technology process flows
- Thermal and thermo-mechanical aspects
- Conclusions

Context – Electronics Industry Drivers

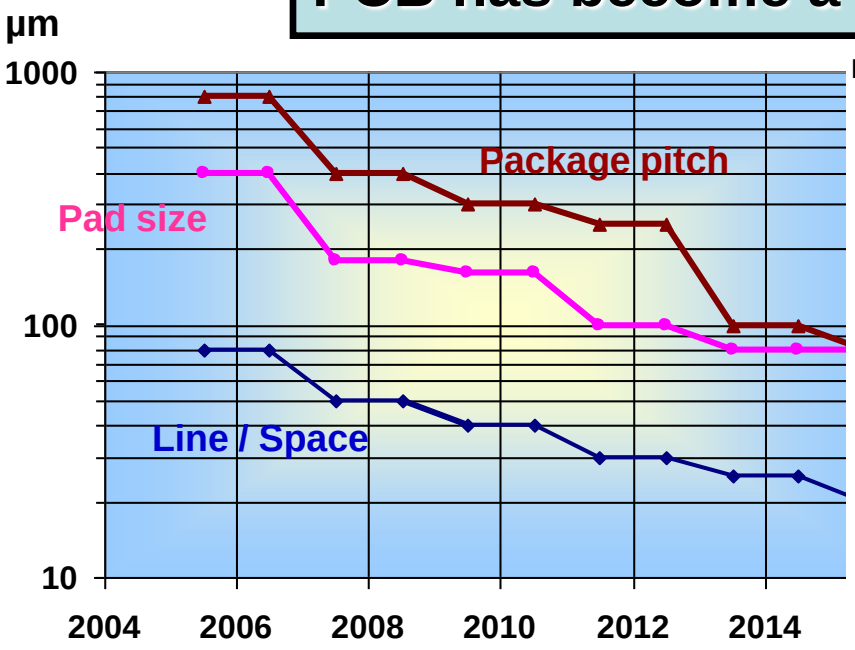
Mobility is the electronics driving force → Miniaturization

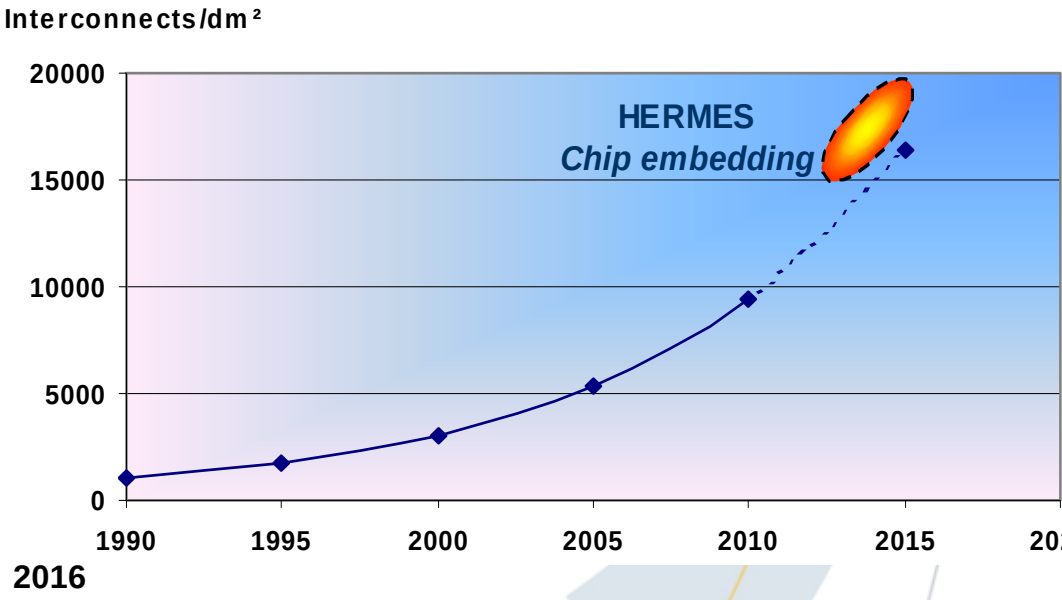
High volume / low cost → High yield

IC features	↘	28nm
IC pitch	↘	30µm
Package pitch	↘	0.4mm
Clock rates	↗	several GHz
Operating voltages	↘	<1V
Power density	↗	20-50W/cm²

- Signal/power integrity
- Routability
- Thermal management in still air
- IC/PCB pitch accommodation

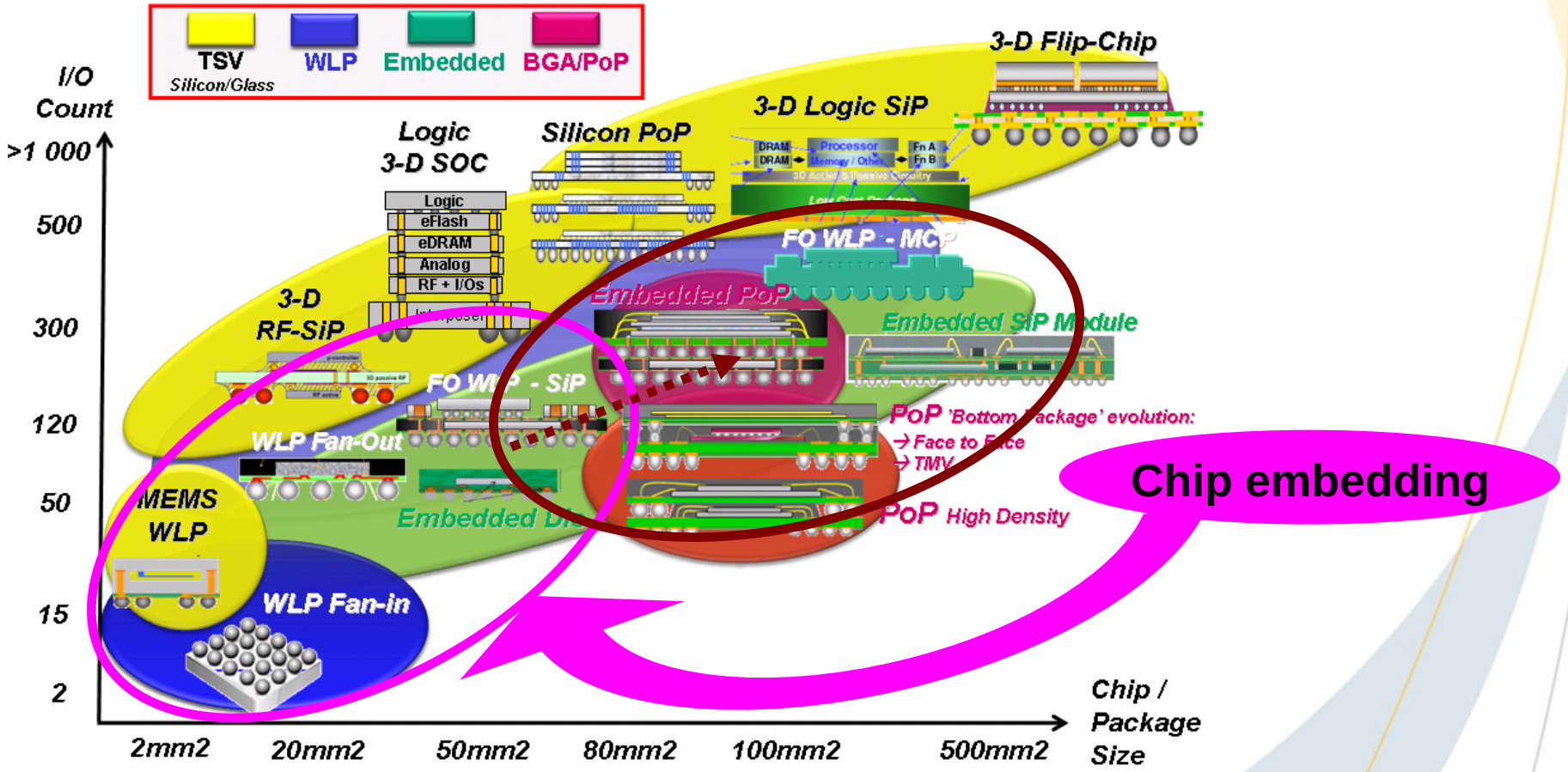
PCB has become a strategic "component "





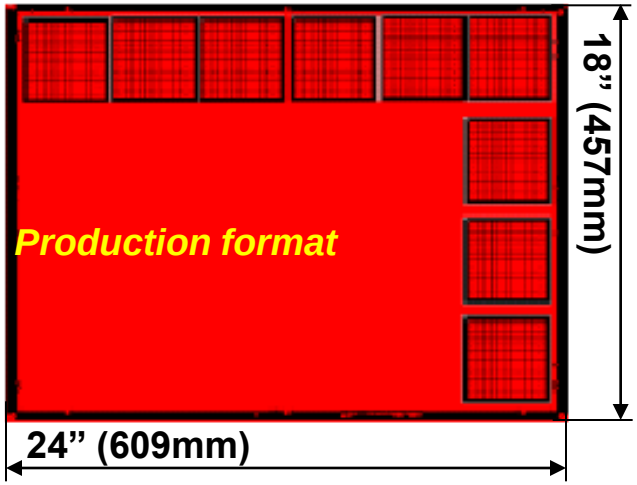
Context – 3D Packaging Roadmap

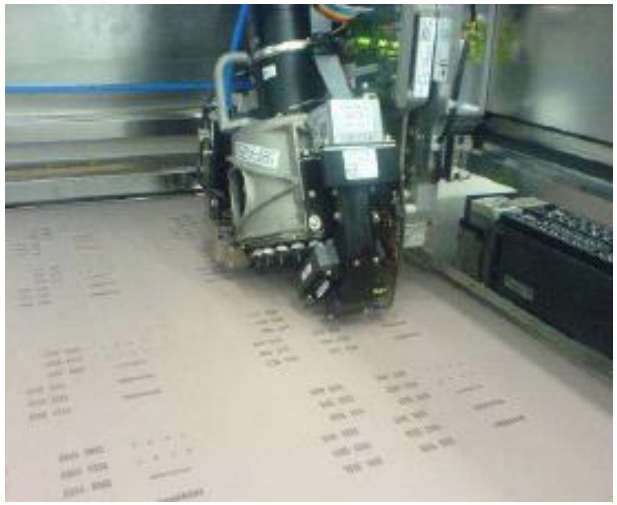
- The constant search for higher levels of integration forces new interconnect and packaging solutions
  - –Emergence of several competitive 3D approaches

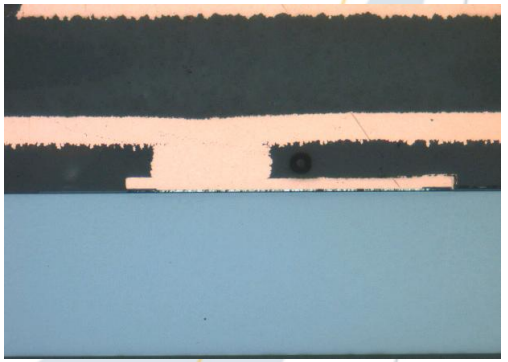


Chip Embedding Key Advantages

- Strong potential to achieve cost effective packages/PCBs
  - Relies on standard base materials
  - Relies on industrial mature PCB processes
    - Multilayer PCB fabrication processes
    - Connections made of filled laser drilled microvias
  - Large panel sizes : 24" x 18"

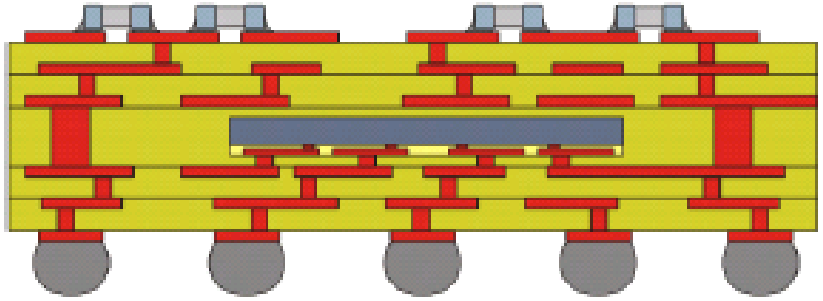


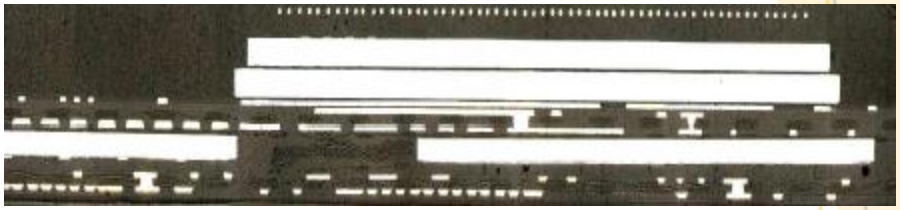




Typical Applications

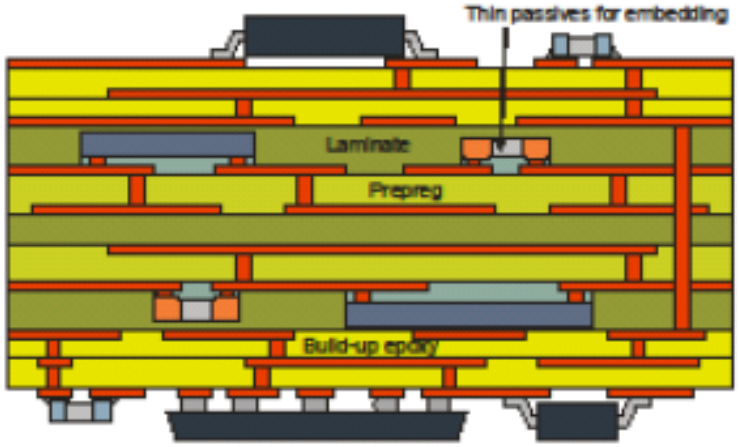
Packages including
several dies





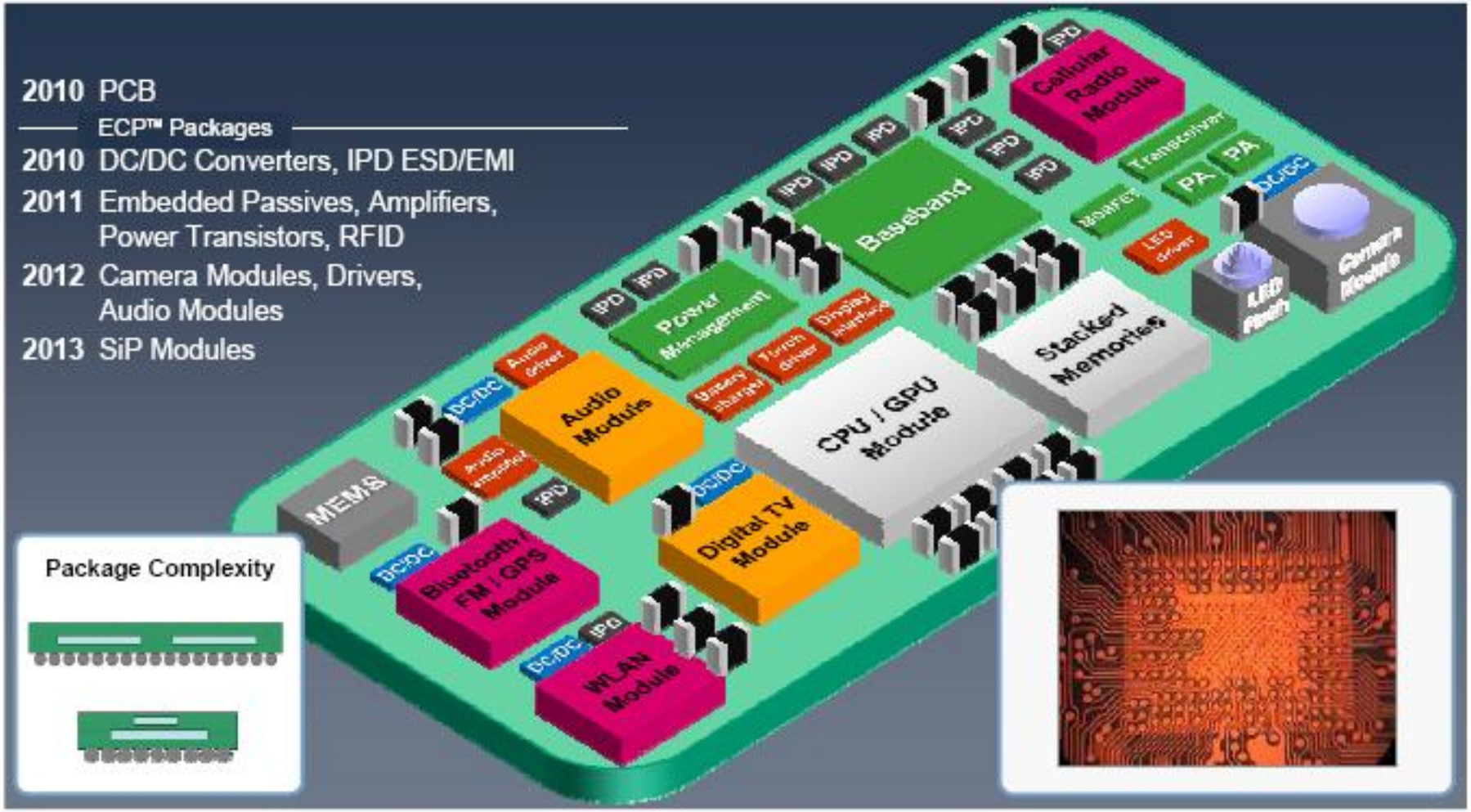
Module with :

- 2 embedded dies in the central core
- 2 stacked dies on the top layer



Highly integrated PCB/modules
with embedded passives & ICs

Mobile Phone Example

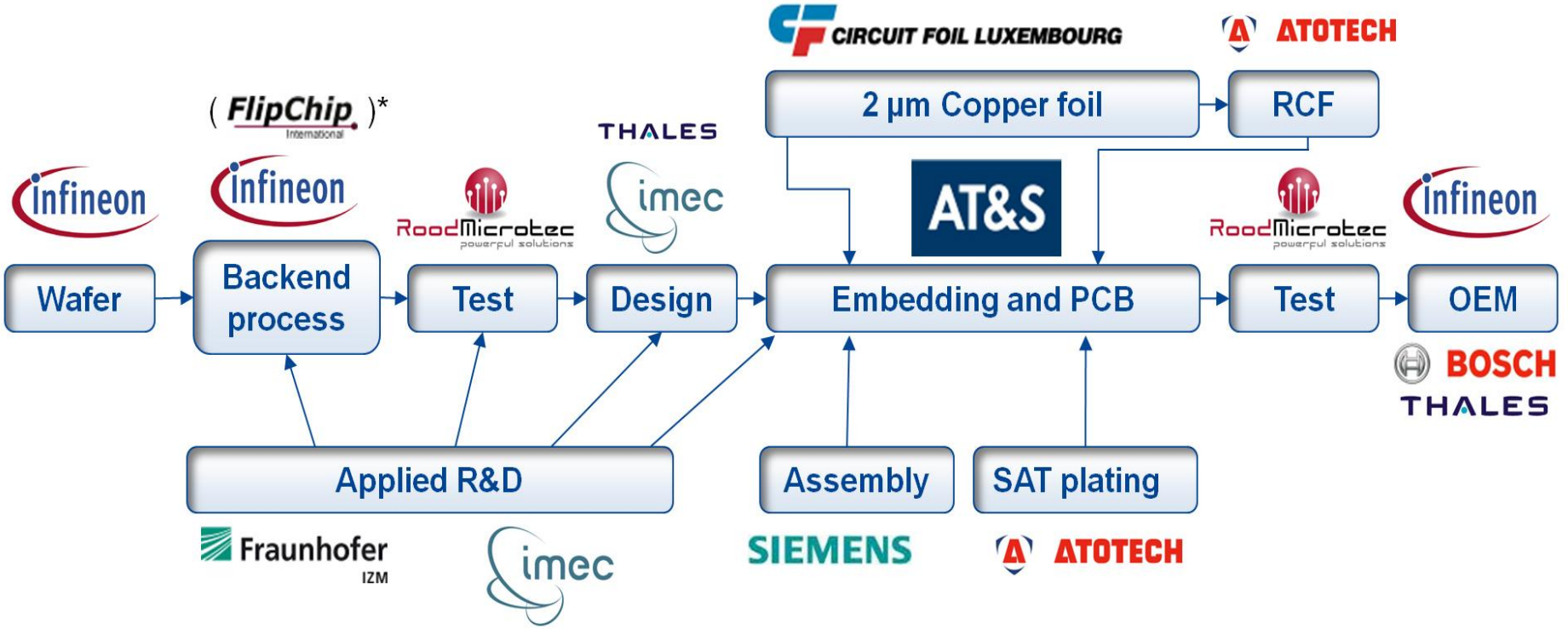


Hermes Project

- European FP7-ICT-2007.3.6 research program
  - Funded by the European Commission
    - Overall budget : 15M€ (~ 22M$)
  - Consortium of 11 partners
  - 3-year duration : 1st May 2008 – 30 April 2011
- Project targets
  - *INDUSTRIALIZE* PCB embedding technology
    - 2 levels of embedded dies (production)
    - 4 levels of embedded dies (prototype, research)
  - Build a supply-chain infrastructure
  - Characterize the technology reliability
  - Demonstrate the technology on fully functional applications

Hermes Consortium Overview

- Complementarity all along the supply-chain
  - From wafer to end-user applications

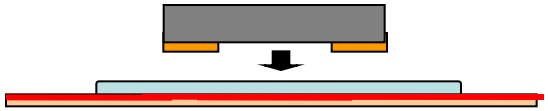


Hermes Technical Objectives

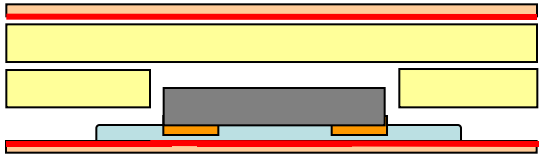
Specification	Hiding Dies achievement – Last AT&S project on embedded chip	HERMES objective – Mass Production	HERMES objective – Technology Prototype
Pad pitch of embedded chip	250um	125um	60um
Panel size for fully integrated process	18" x 12"	24" x 18"	24" x 18"
Chip placement accuracy	10um @ 3σ - 18" x 12" and 1.000 comps/hr	15um @ 3σ - 24" x 18" and 10.000 comps/hr	7,5um @ 3σ
Copper foil	6um	2um	1um
Structuring process	Subtractive	Semi-additive	Semi-additive
Chip interconnect	Laser drill + via metallisation	Laser drill + via metallisation	Laser drill + via metallisation Via-less connection Embedded Flip Chip
Fine line interconnect	50um line width	25um line width	15um line width
Multi-level stacking by embedding	1 chip layer	2 chip layers	4 chip layers

Chip Embedding Process Flow

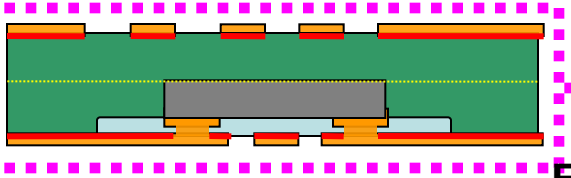
Component assembly



Core lamination

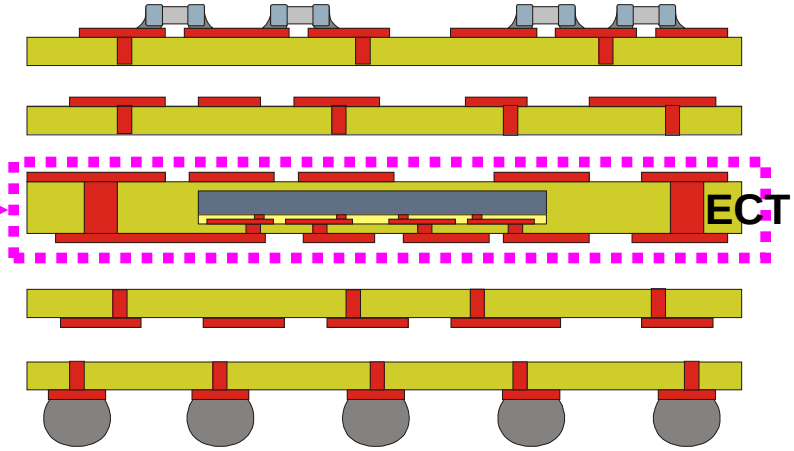


Drilling , Plating , Patterning



Embedded core (passive, active)

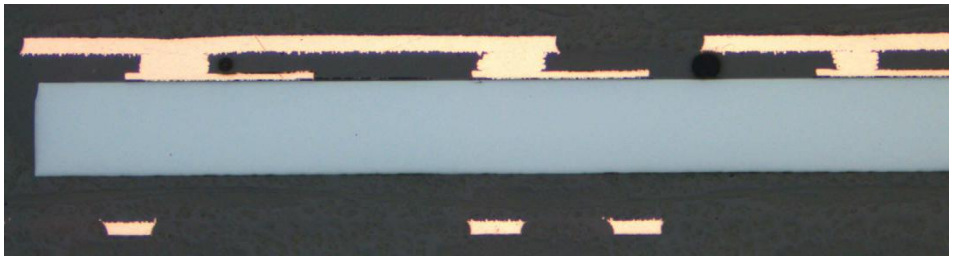
Build up to a HDI multilayer

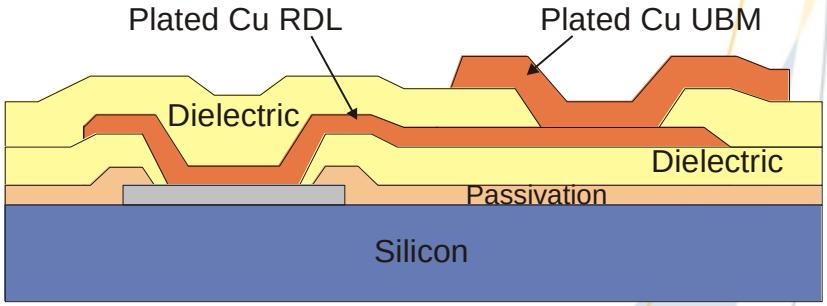


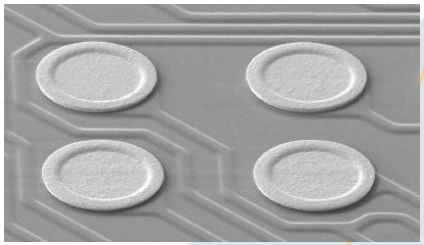
ECT core

Embedding Process Pre-requisites (Die)

- **Silicon wafer/die conversion into embeddable form**
  - **Pad finish : Cu plating needed for contacting with PCB microvias**
    - **Existing processes used for WLP chips**
  - **Pad pitch : adaptation to the PCB scale**
    - **Achieved through a RDL**
  - **Thickness : 100 – 150µm preferred range**
    - **Wafer thinning mostly necessary**

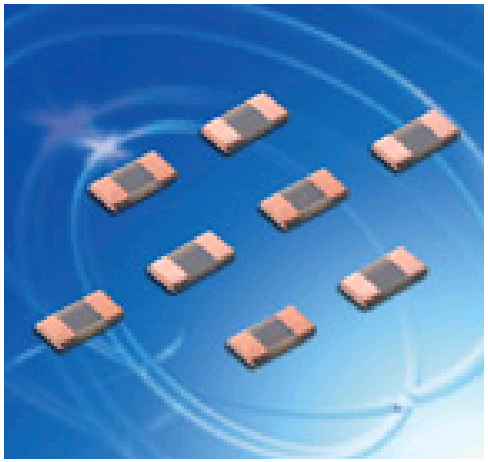


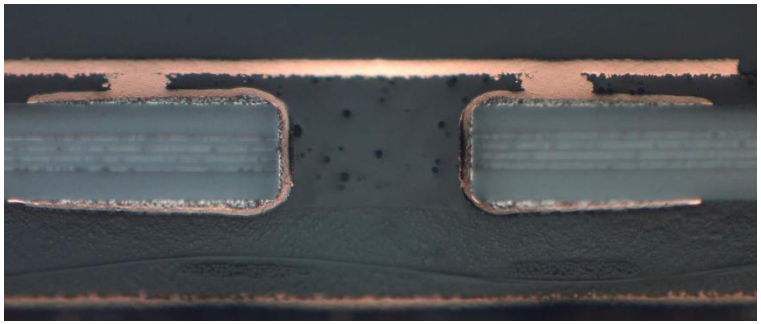


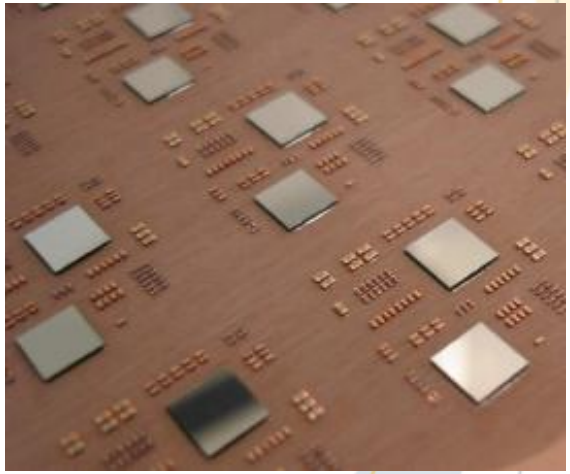


Embedding Process Pre-requisites (Passive)

- **Passive discrete chips**
  - **Use of thin components with Cu terminations**
  - **Capacitors and resistors available on the market**







Technology Implementation in Production

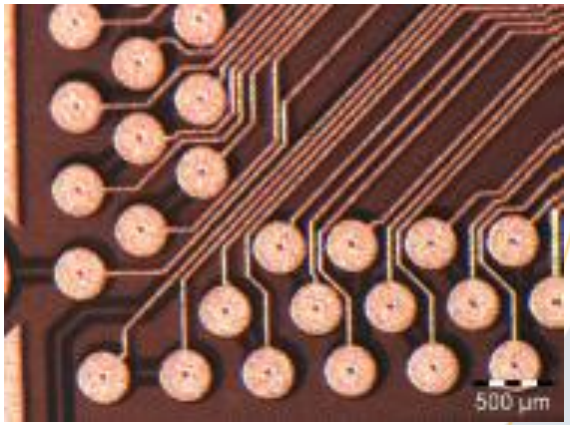
- Maintain high yields and cost effectiveness
  - Introduction of semi-conductor practices and culture
  - Clean room, ESD compliance
  - Site re-configuration to ensure damage–free handling
    - **Touchless processes**

Technology Implementation in Production

- Advanced process capabilities
  - High-speed component assembly
    - **Use of latest generation SMD placement machines**
      - Die bonding from wafer (10000 cph, 15µm@3σ)
      - SMD placement from tape&reel (20000 cph per head, 4 heads)

Technology Implementation in Production

- Advanced process capabilities
  - Semi-additive technology combined with ultra-thin Cu foils to achieve ultra-fine lines
    - **Down to 25/25µm line/space**



Single Board Plating Line :

High uniformity across the panel

High-end Board Reliability Management

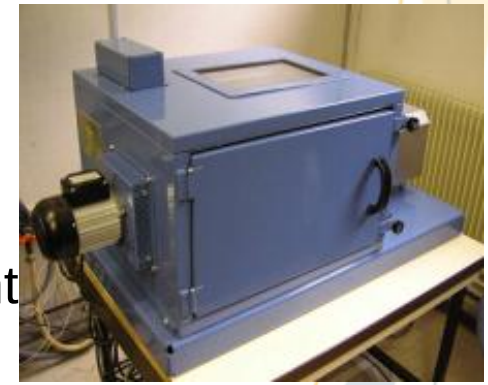
- Goal
  - Define robust design rules for chip embeding adressing :
    - Thermo-mechanical behavior
      - PCB architecture & base materials
    - Thermal management
    - Signal integrity* (Cross-talk, power integrity, controlled impedance)
    - Reliability
      - PCB interconnect & 2nd level assembly

- Methodology
  - Many dedicated test vehicles
    - Experimental test results
    - Physical data to calibrate FEA simulation
  - Build generic models
    - In order to accelerate the design phase of any new product

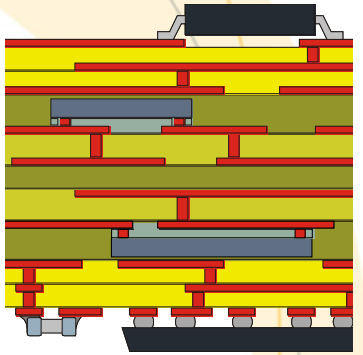
**** Not developed in this presentation***

Thermo-mechanical Evaluation

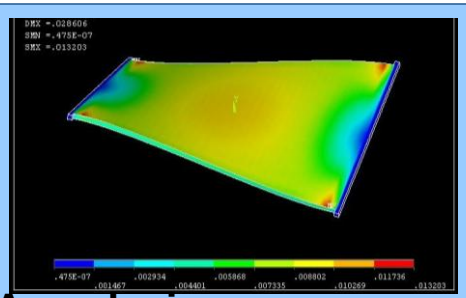
- Objectives
  - Extract physical material parameters from experiments
  - Assess the thermo-mechanical behavior of chip embedded PCBs
- Methodology
  - Large experimental plan based on multiple stack-ups focused on:
    - Face down technology
    - One embedded core (200 to 400µm thickness)
  - Introducing :
    - Torsion tests on a new test bench generation
    - Embedded and external strain gage measurement
  - Develop a generic FEA strain distribution model
    - Including
      - 2 layers of embedded dice
      - QFN & BGA assembled on external layer
  - At the end, measure the reliability using optimized designs
    - On test vehicles reflecting functional demonstrators



Thermo-mechanical Evaluation Synoptic

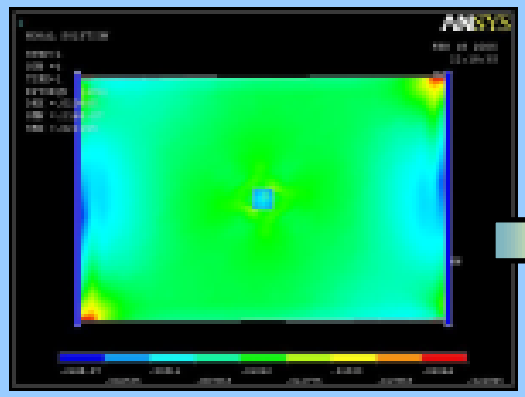


- Modelling of stress & strain in embedded structures
  - Incidence of the die size & relative position (Z-axis)
  - Focused on one level of embedded active dies
    - Overlapping investigation for 2 embedded layers
- Validation by strain gage measurements under torsion



FEA analysis

Torsion test with strain meas.



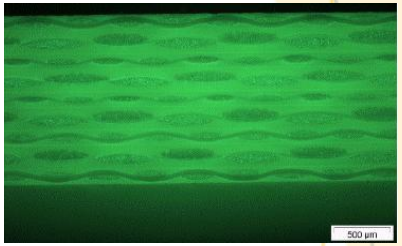
Strain distribution

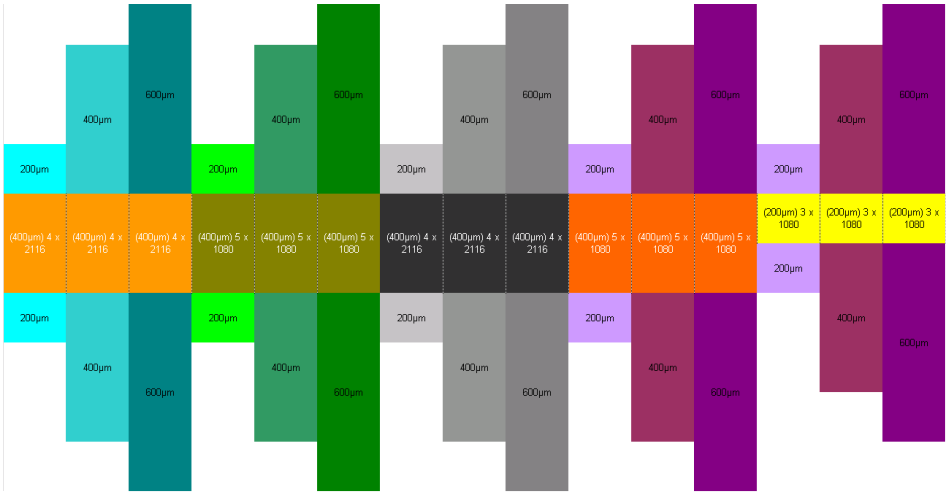
Results analysis
&
Failure mechanism

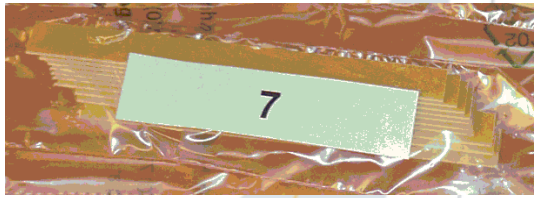
Design rules

PCB Physical Property Measurements

- Rationale : need for actual measurements
  - Data supplied by PCB laminate manufacturers are useless
    - Relevant to simple constructions, no consideration of resin content
    - PCB stiffness not taken into account *
- Test program
  - 46 different PCB build-ups
  - Samples of 10mm x 100mm without internal copper
  - 2 high-Tg halogen-free epoxy materials



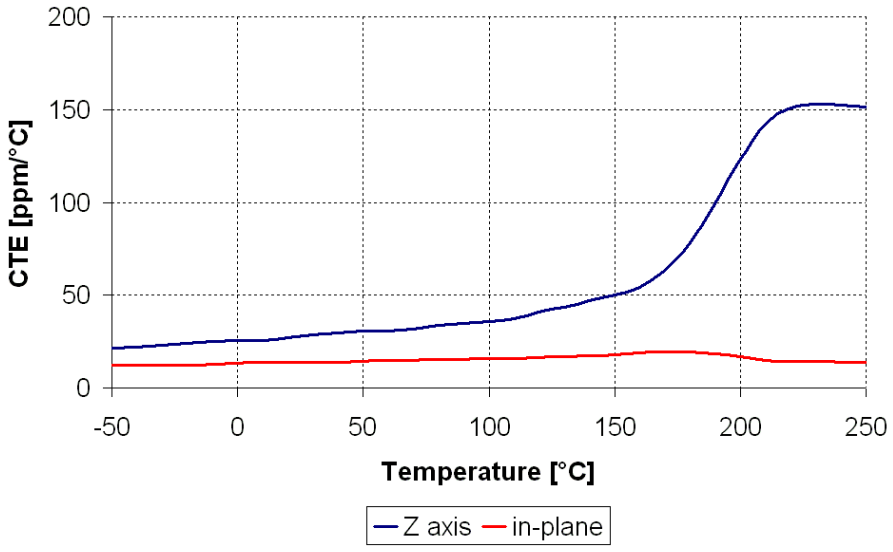


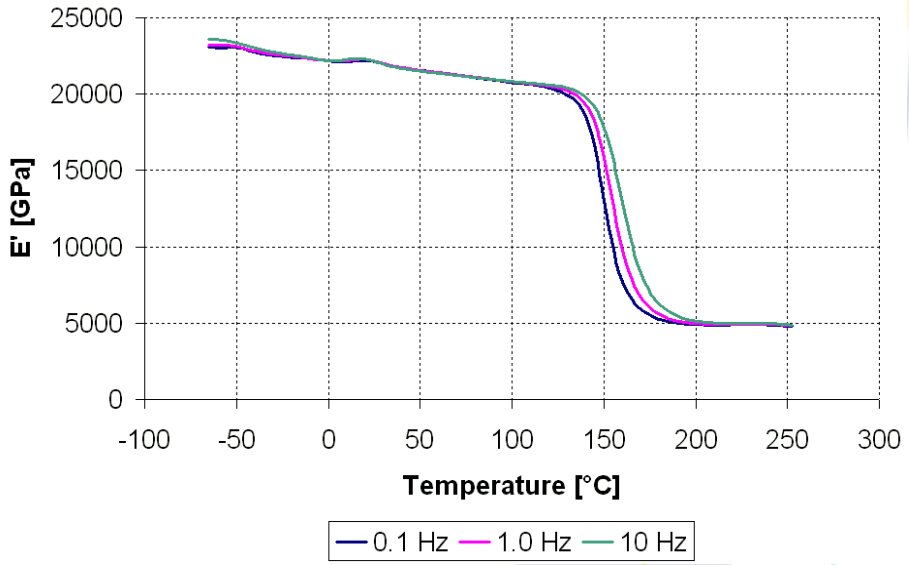


* *W. C. Maia Filho et al., "Influence of build-up construction and resin-content on mechanical behavior of printed circuit boards", Proceedings of 10th IEEE Eurosime, Delft, Netherlands, April 2009.*

PCB Physical Property Measurements

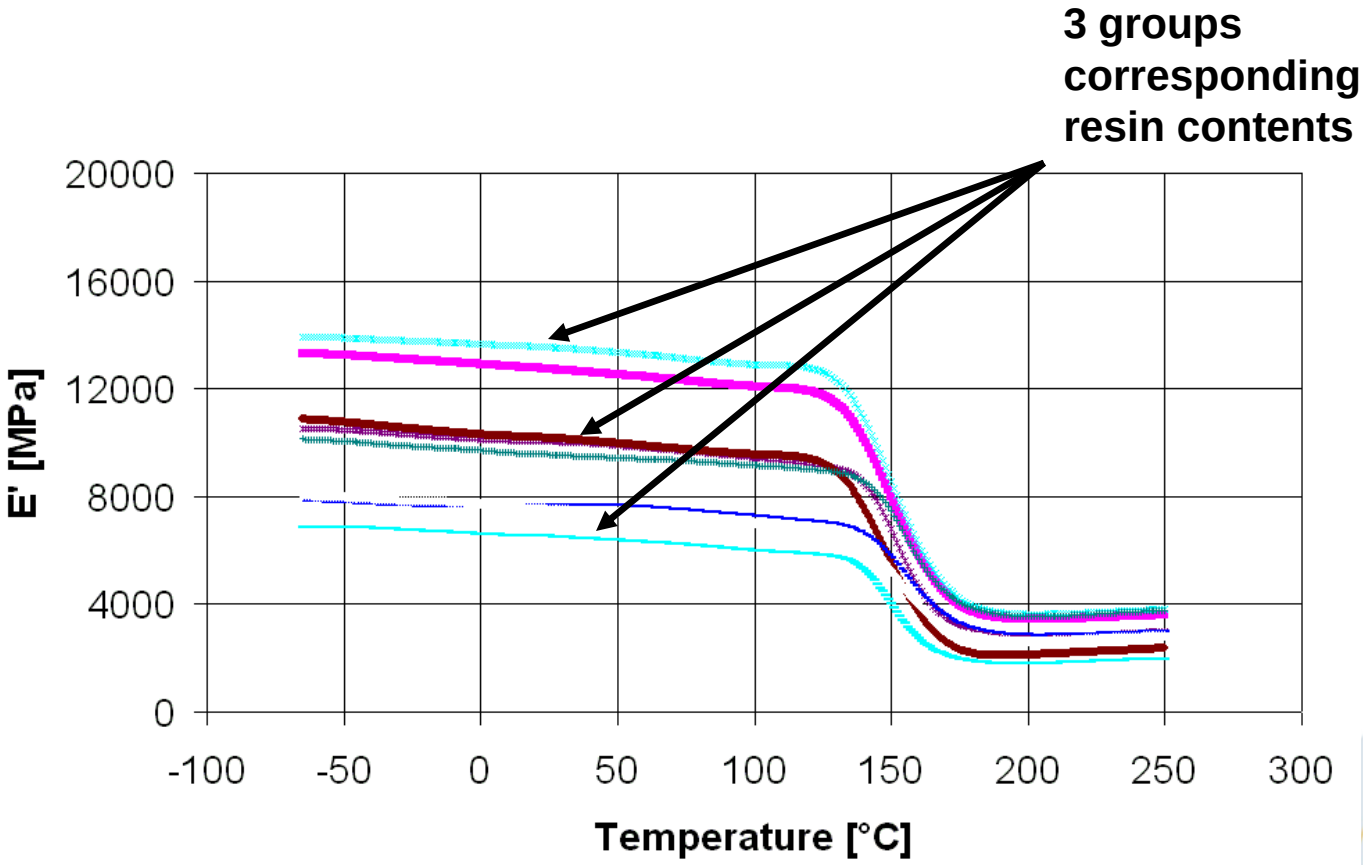
- Measured characteristics
  - Resin content : Thermo Gravimetry Analysis (TGA)
  - $CTE_{x, y}$ & CTE_z : Thermo Mechanical Analysis (TMA)
  - Elastic modulus : Dynamic Mechanical Analysis (DMA)
    - –60° C / +260° C temperature range
    - 3 different frequencies : 0.1 – 1.0 – 10Hz





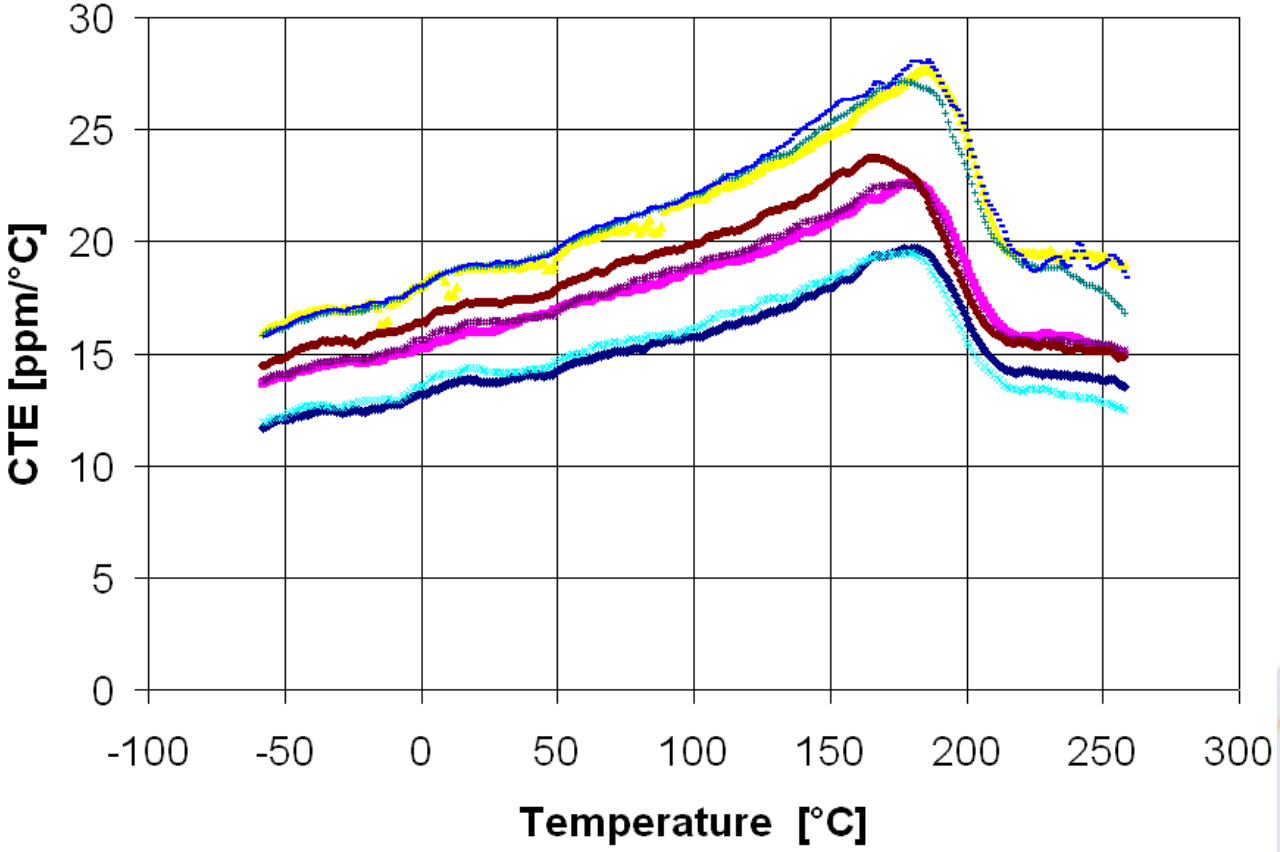
PCB Physical Property Measurements

- Examples of results (Material #1, DMA)
  - Incidence of resin content



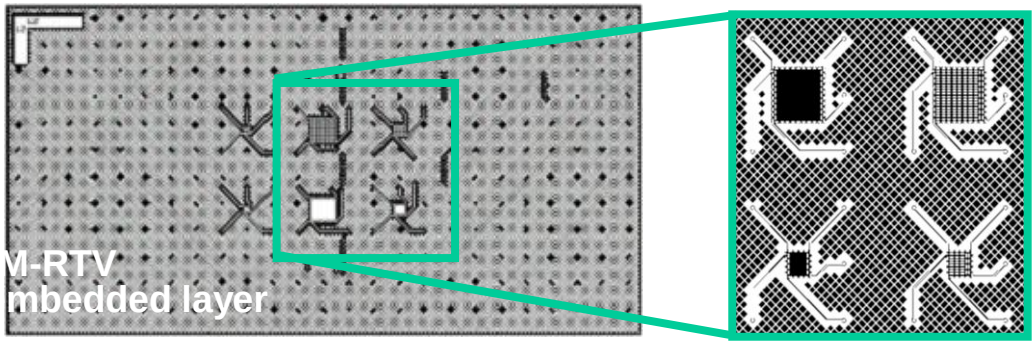
PCB Physical Property Measurements

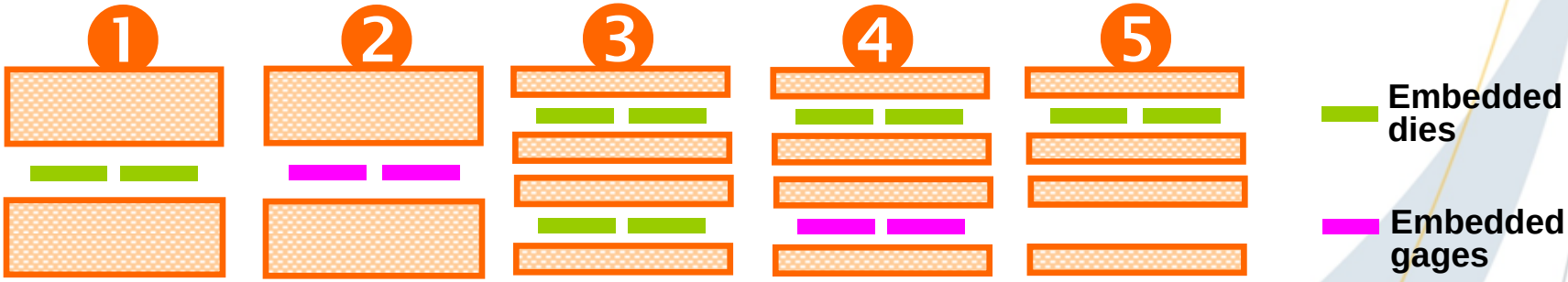
- Examples of results (Material #2, TMA)
  - Incidence of pre-preg style on $CTE_{x,y}$



PCB Strain Characterization

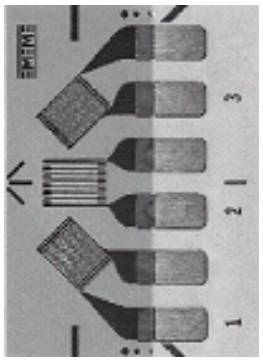
- PCB test vehicle features
  - 260mm x 125mm dimensions
  - Various constructions with embedded components and/or gages
    - Daisy-chain dies : 3 x 3mm², 5 x 5mm², 10 x 10mm²
    - Passive chips : 0201, 0402 (Cu finish)

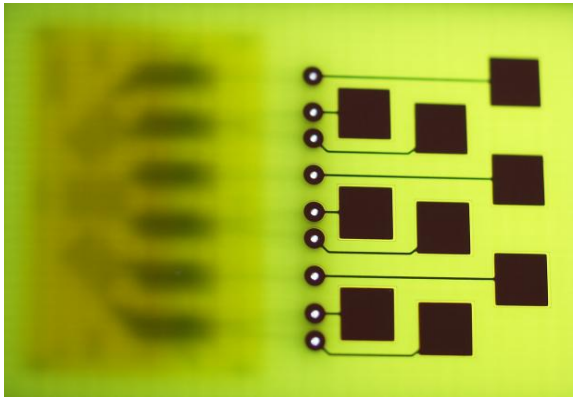


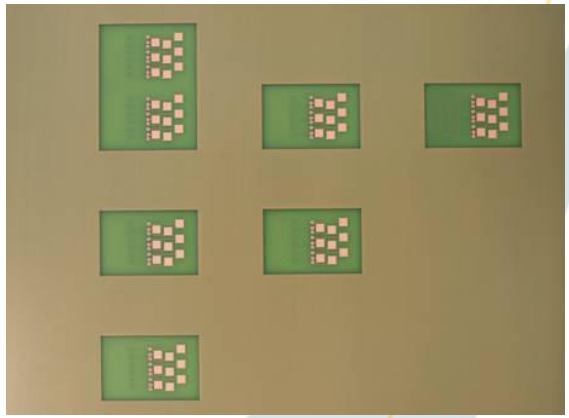


Embedded Strain Measurement Validation

- Strain gage embedding is very challenging
  - Large panel dimensions
  - Complex gage structure for embedding (flexible polyimide support)
  - Specific manual assembly process
- Validation done on 8mm x 12mm gages
  - Active length of 1.2mm

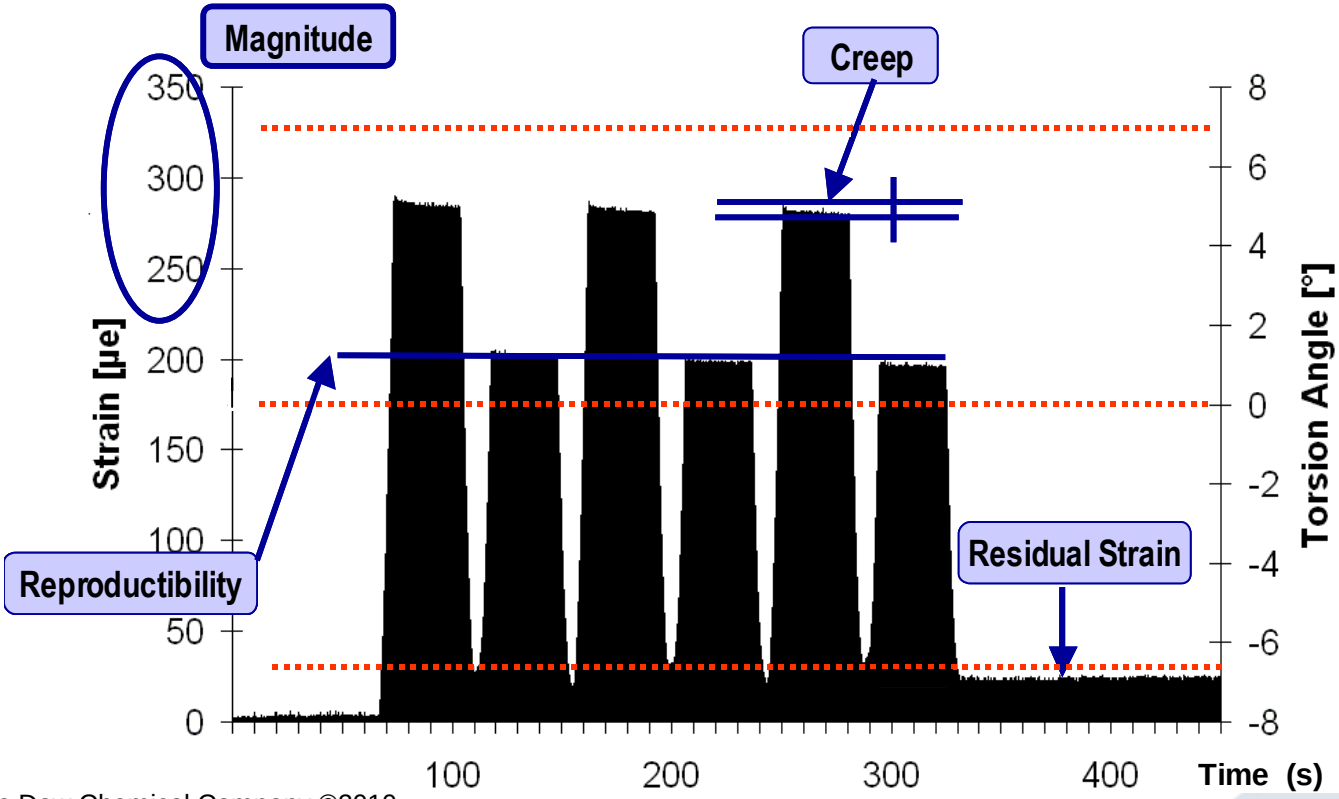






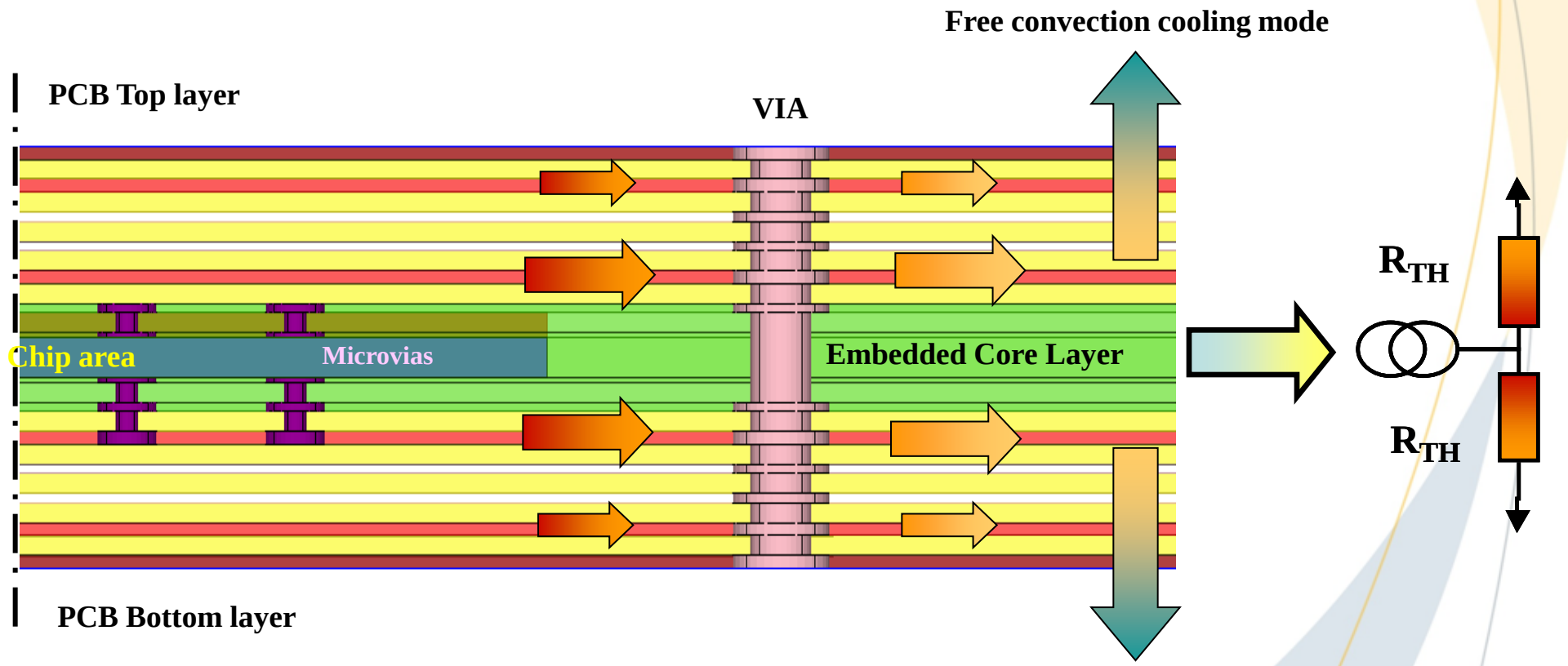
Embedded Strain Measurement Validation

- Response analysis of the embedded gage under torsion
  - Magnitude consistent with previous studies
  - Good reproducibility during several torsion cycles
  - Creep consistent with external gages results
  - Observation of a normal residual strain due to bench backlash



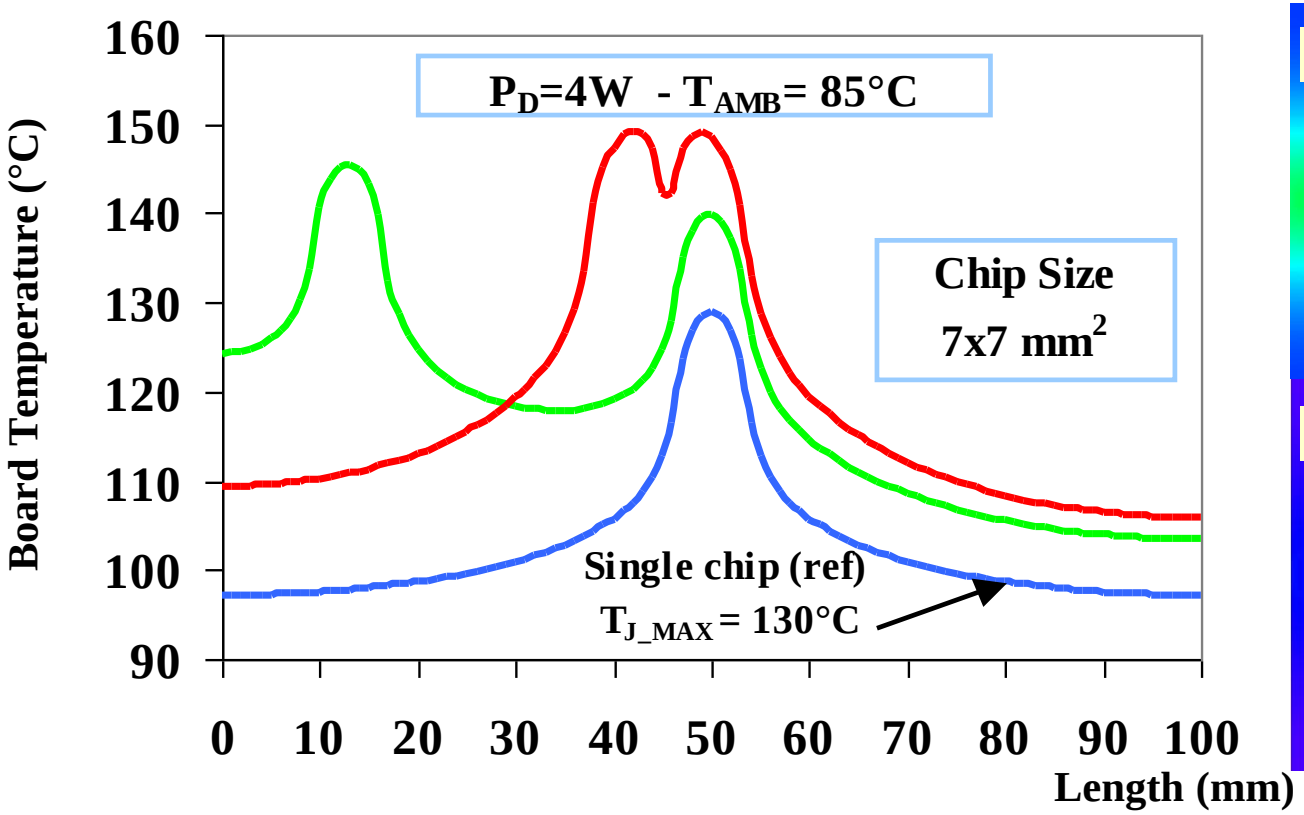
Thermal Aspects

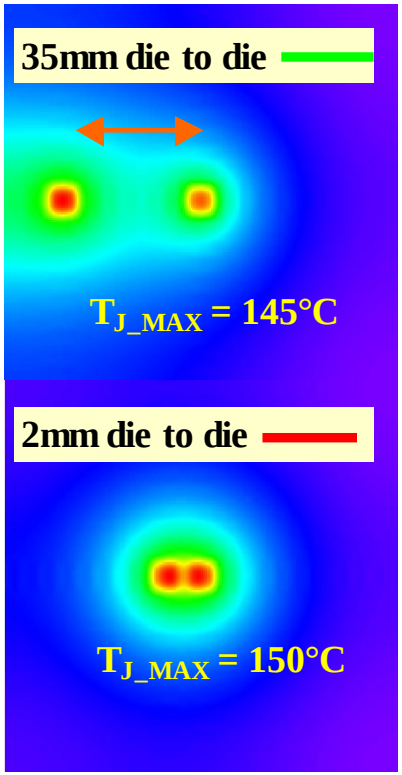
- Objectives
  - Build an analytical model to predict the thermal behaviour of an embedded chip at an early stage of the design



Example of Thermal Design Variables

- Analytical approach benefits
  - Possibility to quickly define the most appropriate
    - PCB layer arrangement
    - Chip placement according to its dissipation





Conclusions

- Passive & active chip embedding developped in HERMES:
  - Is mandatory to achieve extremely high density SIP & boards
    - Accommodate the last generation of complex digital ICs
    - Compliant with large range of resistor & capacitor values
      - Needed for signal integrity and routability
- Industrialization of "face down" chip embedding is
  - In the last stage of manufacturing investment
  - Finalizing the SPC monitoring of critical process parameters
  - Shortly ready for ramping up volume production phase
- HERMES will provide robust design rules
  - For critical aspects such:
    - Base material and stack-up
    - Breakthrough of thermal management in still air
      - Energy stored in the middle of the PCB
    - Signal integrity

Acknowledgements

The HERMES consortium would like to thank the European Commission for having :

– Trusted in our ambitious project

– Funded this 3-year FP7-IP project

Thanks for your attention

For more information, consult Hermes website :

http://www.hermes-ect.net