PCB Design and Assembly for Flip-Chip and Die Size CSP

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Abstract

As new generations of electronic products emerge they often surpass the capability of existing packaging and interconnection technology and the infrastructure needed to support newer technologies. This movement is occurring at all levels: at the IC, at the IC package, at the module, at the hybrid, the PC board which ties all the systems together. Interconnection density and methodology becomes the measure of successfully managing performance. The industry must address the technology gap between printed boards and semiconductor technology and how the semiconductor and IC packaging suppliers can combine resources in furnishing viable solutions. Although the development of fine-line substrates and assembly refinement has narrowed the gap somewhat, minimizing component outline, the array contact format and reduced contact pitch is proving to be the most practical solution for uncased flip-chip and die-size package applications.

This paper outlines the basic elements furnished in the newly released IPC-7094 '*Design and Assembly Process Implementation for Flip-Chip and Die Size* Components' providing a comparison of existing and emerging wafer level and chip-size package methodologies. It will focus on the effect of PCB design and assembly of bare die or die-size components in an uncased or minimally cased format. The PCB design guidelines and assembly process variations furnished will provide useful and practical information to those who are considering the adoption of miniature bare die or die size array components.

Introduction

Semiconductor suppliers have abandoned the traditional wire-bond package assembly for many of the higher I/O products, opting for the more compact die face-down flip-chip attachment methodology. The face-down, direct attachment method significantly reduces the semiconductors package size as well as enhancing product performance. While wire-bond interface may remain the preference for many applications, face-down direct chip attachment has gained popularity for a growing number of higher-speed processor and ASIC products. Flip-chip technology, although in the past was regarded as limited to specialized applications, is gaining greater acceptance for addressing the need for smaller package outlines. The bumped flip-chip process has historically served as the main interconnect method in direct-die attach packaging. The minimum perimeter solder bump pitch for flip-chip currently ranges between 150µm and 200µm. To enable a more uniform interconnect for the higher density and higher I/O semiconductors, companies are redistributing conductor layers on the die surface to provide an array contact format that is more easily accessed on the mating interposer substrate. As die complexity increases, however, we are faced with a several challenges:

- Increasing I/O requirements
- Decreased contact pitch
- Thermal management
- Circuit routing optimization

Additional factors that must be addressed when adopting WLBGA include; performance, reliability and cost. Although each factor carries equal status when assessing the merits of any flip-chip or re-distributed array packaging innovations, cost remains the primary concern. Cost of the product will always influence adoption of one technology over the other. When companies choose to adopt uncased WLCSP semiconductors, quite a few issues must be resolved:

- Managing multiple IC vendors
- Availability of 'Known Good Die' (method of test and burn-in)
- Die and wafer availability/uniform quality
- Compound yield expectation for less mature ICs
- Anticipation of future die shrinks

A number of single-die wafer-level package innovations have been developed for a broad market; however, many supplier companies are not able to meet acceptable manufacturing yields. This is due in part to the difficulty of simultaneous testing of die while in the wafer format. The definition of known quality die (KQD) is that the supplier

will demonstrate with data that the defect level and early failure rate estimates on die shipments are within the negotiated range, and retain a level of confidence in those estimates. Wafer level probe test is typically employed to perform only basic analysis and is not widely utilized for performance sorting, reliability screening or massively parallel contacting. If the uncased die elements are only to be tested while in the wafer format, the user still expects the same quality and reliability level of packaged part.

Flip-chip and Die-size Package Standards

Because of the rapid movement toward semiconductor package miniaturization, members of the Joint Electronic Device Engineering Council (JEDEC) have developed a number of standards and guidelines to help maintain a degree of uniformity for the semiconductor devices final configuration. Its membership includes semiconductor manufacturers, packaging services companies, material suppliers and users. The organizations JC-11 subcommittee is responsible for developing the mechanical outline requirements for solid state semiconductor packaging. The two standards that the IPC-7094 document has focused on are JEDEC 95 Publication 'Design Guide 4.18' for WLBGA and 'Design Guide 4.7' for DSBGA. Their definition is as follows:

- A Wafer Level Ball Grid Array (WLBGA) has an array of metallic balls on the underside of the package. The substrate of the package is the semiconductor die with or without a redistribution layer that may have a square or rectangular shape with metallic balls applied onto the circuit side of the die. The array pattern of metalized balls provides the mechanical and electrical connection from the package body to the next level component such as a printed circuit board or intermediate substrate.

- A Die-size Ball Grid Array (DSBGA) also has an array of metallic balls on the underside of the package. The die elements are, however, attached to a dielectric substrate or carrier for redistribution of the die bond pads to a uniform contact array pattern. The package substrate may have a square or rectangular shape with a metalized circuit pattern applied to one or both sides of a dielectric structure. The size of the substrate or carrier is as close to the die size as practically possible.

The contacts on the WLBGA and DSBGA are balls, bumps or other protruding terminals constructed from a variety of alloy and/or polymer materials. The alloy ball or bump features are, as noted, added to each contact site to provide both mechanical and electrical connection from the package body to the next level component such as a substrate or printed circuit board. Typically, when balls are present, they consist of eutectic tin/lead solder alloy composition or one of several lead-free solder alloys. For purposes of the JEDEC documents, these contacts of whatever final form are referenced generically as "balls". In regard to accommodation for board level assembly processing, the perimeter bumping process is generally limited to mounting uncased die having a relatively few contact sites. Larger die requiring higher pin count, will likely be processed to redistribute the peripheral located wire-bond sites to a uniform area array format.

The profile height of the WLBGA and DSBGA devices are very thin. The finished devices are not encased in plastic typical of the coarser pitch BGA families, however, some suppliers may furnish these miniature components with a thin polymer coating to protect the exposed silicon surfaces. The actual height of the array device is defined as the distance from the seating plane (the surface of the mating circuit board) to the highest point on the package body. This distance is measured perpendicularly to the seating plane.

WLBGA vs. DSBGA

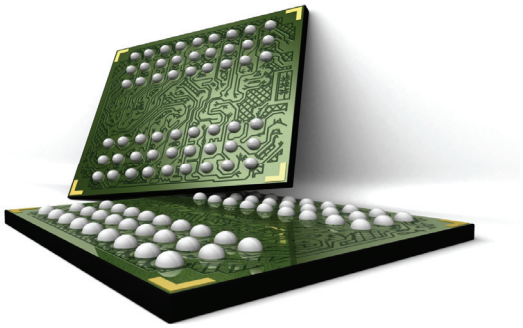
There are a number of factors to consider when selecting an optimal semiconductor package configuration for the newer generations of high density controllers and processors; I/O requirement, package footprint, form factor, thermal dissipation, electrical performance, and cost. The more advanced microprocessor and ASIC semiconductor packaging currently require several thousand contact sites and they are expected to expand contact I/O by 30% in the very near future.

It is not uncommon for these higher pin count die elements to be furnished with bond sites spacing less than 100µm. To overcome flip-chip mounting and circuit routing difficulties companies are redistributing the contact locations directly over the active surface of the die. Following surface passivation and a surface metallization process, copper circuit features are pattern plated to connect the perimeter wire-bond features to contact sites arranged in a column and row configured array. The copper conductors are then coated with a photo-imageable polymer allowing the contact sites to remain free of the coating for the subsequent solder bumping process.

Several methods have been developed for furnishing solder compatible contact features while the die elements remain in the wafer format. The most common and economical process simply deposits or electro-plates a solder compatible alloy at each contact site and, following some means of heating the surface, reflows the alloy to form a near-spherical bump profile. A

more complex (and rather lengthy) proprietary wafer-level process actually electroplates a raised solid copper post feature at each contact site and after planarizing, adding a small profile of solder at its tip.

When the contact sites are arranged in the array package format it furnishes a more uniform interface configuration by providing better access for circuit routing. The array format also accommodates more efficient electrical test. Some companies may perform some level of electrical test while the die elements remain in the wafer format, however, the most thorough and reliable electrical testing is when bump or ball contacts are furnished on a singulated die element (see Figure 1), allowing each device to be socketed.

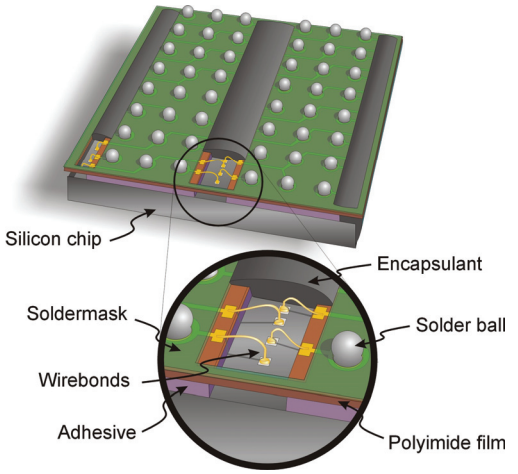


Source: Micron Semiconductor

Figure 1. The uncased WLBGA, when prepared with compatible alloy bump contacts can be socketed for electrical testing.

As an alternative to solder bumping or ball contacts, gold alloy contacts can be furnished for device attachment. The gold contact is generally applied by electroplating or by using a common wire-bond system. When a wire-bond process is used, the wire is snapped off at the top surface of the basic bond mass leaving a reasonable uniform bump feature.

Die size (DSBGA) array package technology has evolved using widely differing constructions including a number or proprietary packaging methodologies. Many applications have been successful in employing flip-chip technology, however, when handling and testing the uncased die, users realize that without some form of reinforcement (post assembly underfill or encapsulation) that they are prone to cracking and, because of the thermal co-efficient of expansion differences of silicon and PCB laminates, solder joint fatigue is common. Companies have found that even minimal packaging of the bare die element can reduce assembly process damage. Although DSBGA package methods differ somewhat, a number of companies offer a structure that enhances both functional performance and physical robustness. One of the most widely adopted packaging processes used for packaging silicon is the face-down wire-bond µBGA®. The technology enables the smallest possible finished package outline while providing a method for furnishing a uniform contact size. Although the use of the methodology requires a licensing agreement with the patent holder, the material set used in the package process significantly contributes to the physical integrity of the end product (illustrated in Figure 2).



Source: Tessera

Figure 2. Face-down DSBGA with through-slot wire bond interconnect

The de-size µBGA package methodology was developed to minimize the impact of the thermal coefficient of expansion between the silicon die element and the circuit board. When completed, the structure provides a unique compliant polymer adhesive layer between the die surface and package substrate to decouple the differential expansion of the silicon (3ppm per ºC) from that of the circuit board substrate (~16ppm per ºC). Unlike the flip-chip configured device, the µBGA package, when soldered onto the circuit board, does not require underfill.

PCB Design

Design for flip-chip or die-size component assembly is similar to that for presently used for soldered surface mount assembly except the flip-chip die may adapt a non-solder process for attachment. After establishing the contact type (ball or bump) and diameter, determine the contact feature geometry and pitch. Contact sites designed for wire-bond processing on the die may be randomly or uniformly spaced at the die periphery. Array configured devices, on the other hand, are generally more uniform with a larger diameter contact and wider spacing between contacts. Land patterns developed for spherical (ball) contacts can the same diameter as the sphere or slightly smaller, however, with lower profile bump contacts, the land pattern diameter is more likely to be equal to the bump diameter. Because there is little time for the user to build, test and evaluate land pattern variations for each device, JEDEC states that the supplier is obligated to specify the recommended land pattern geometry that will furnish the most satisfactory electrical interface between the device and package interposer or module substrate.

In most applications only one bump contact diameter will be furnished because varying bump diameter may impair chip attach. Although not recommended, specialized applications requiring multiple contact pitch variations do exist. The IPC-7094 standard suggests that the minimum bump pitch be no less than 250 microns when possible to facilitate the assembly of standardized substrates. Many bumped die, however, may be furnished with a contact pitch as close as 100 microns. When this occurs, the product designer should be aware of the potential for contact-to-contact, contact-to-trace, and trace-to-trace shorting. Whether using a common perimeter solder bump layout or designing an array footprint format, the package designer is entrusted to position the power, ground, signal, and clock I/O locations with respect to optimizing performance of the host package interposer or substrate structure.

Substrate and PC Board Level Assembly Processing

Current generations of high density wafer fabrication processes are providing significantly smaller die in relationship to the number of contacts traditionally needed for electrical interface. The ‘die-shrink’ factor forces the semiconductor company to further reduce wire-bond pitch. As noted, most of the flip-chip and die-size packaged devices will be furnished with solder alloy bump or preformed solid solder contacts. This alloy bump or ball is applied to the contact features using a thick electro-plating process, solder deposition or by placement of individual preformed ball contacts. All of these processes require mass reflow to complete the forming or joining of the finished bump or ball contact. Of course, the alloys selected for bumping the die must be compatible with the solder composition used on the mating substrate.

When ordering the solder paste printing stencil, the assembly specialist may choose to make subtle changes to the land pattern master to ensure solder paste coverage. Depending on the solder alloy composition selected, the engineer may reduce or increase solder paste print volumes at key locations. In specifying the stencils aperture (opening) for the very fine-pitch WLBGA and DSBGA devices, the process engineer will likely adapt the same diameter as the land pattern features on the board. Others may determine that to ensure a more robust solder joint that the solder deposit be slightly greater. To achieve a greater volume of solid solder particles, the engineer can either increase the stencil thickness or expand the size of the aperture or both. For a 0.45 mm diameter ball contact, for example, the allowable tolerance range is 12 microns while the 0.40 mm diameter contact has a 10 micron range and the 0.30 mm diameter ball is maximized at 8 microns. The IPC-7095 suggests that for array devices having a contact pitch greater than 0.40mm, that the land pattern diameter on the substrate be furnished 20% smaller than the nominal ball contact size.

In regard to the solder paste and alloy compositions, suppliers offer materials that cover the complete range of applications, including no-clean, water soluble and lead-free technologies. Suppliers note that the choice of solder alloys is determined by the requirements of both process and reliability. Besides meeting the solder wetting requirement, the solder composition selected should be able to maintain its physical and mechanical integrity during processing and the products ultimate use. In regard to lead-free soldering, experts advise that, although not currently mandatory in North America, lead-free soldering for electronics is a global trend and the favored Pb-free solder alternatives will often vary from region to region. In general, the high-tin alloys have wide acceptance. The most common lead-free alloy compositions include tin and silver (Sn/Ag), tin and copper (Sn/Cu), tin, silver and copper (Sn/Ag/Cu) and other more complex combinations that include elements of bismuth, zinc and even antimony.

Placement accuracy and cycle time are factors that contribute most significantly to the overall assembly cost. A wide range of choices exist for both low and high volume assembly of flip-chip and surface mount devices. The solder

connection process for flip-chip begins with pickup and machine vision inspection of the device outline. To ensure that a satisfactory electrical interface is made, the die must be precisely aligned over the corresponding lands provided on the substrate. The most common process places the flip-chip or die-size device directly onto printed or deposited solder paste patterns. An alternative mounting process applies flux to either the device contacts using a dip-transfer process or the flux is printed or deposited directly onto the contact pattern of the substrate. When all devices are mounted, the board is ready for reflow soldering.

There are several optional methods available for heating the solder to complete the attachment process. The most common soldering system for high volume assembly operations is convection reflow solder processing that elevates the assembly temperature using heated air or gas. Reflow soldering can be performed using infrared energy as well, although the process is rather harsh and if not carefully controlled, may damage components and the circuit board. A popular low cost and affective method for reflow soldering single sided assemblies uses surface convection. For this process the solder is heated through the bottom surface of the board. Although somewhat specialized, another method for mass reflowing the solder is the vapor phase process. For this method a liquid material is heated to its boiling point creating a controlled vapor that maintains the exact temperature required for melting the solder and completing the joining process.

An alternative low temperature process for attachment of the device to the substrate or PCB is achieved using conductive polymer containing a high concentration of noble alloy particles that, when cured, provides a uniform electrical interface between device and substrate contact features. When using solder or conductive polymer material for flip-chip device attachment, the gap (standoff) between the die surface and the substrate surface will likely require an under-die-filling (underfill) with epoxy to ensure mechanical integrity of the die-to-substrate interface. Capillary underfill epoxy is generally added to the assembled flip-chip circuit to increase mechanical strength. Epoxy underfill can enhance solder interface reliability of the flip-chip component up to 10X over components without underfill.

Addressing Next Generation Semiconductors

The more advanced microprocessor and ASIC semiconductor packaging will require several thousand I/O contacts and they are expected to expand contact I/O by 30% in the very near future. Consistent die-to-substrate interface, however, remains the most critical barrier in achieving optimum assembly process yield. Semiconductor suppliers have been forced to abandon the traditional wire-bond package assembly for many of these higher I/O products, opting for the more compact die face-down flip-chip attachment methodology. There are two issues that continue to impede defect free joining of the high-density flip-chip die to the interposer substrate; solder bump uniformity and substrate flatness. In regard to the solder bumping process, deposition of solder paste at the die contact sites has variables.

The solder paste material, whether deposited or printed, is comprised of both solid alloy particles' and flux. Depending on the powder size, the ratio of solids to flux can vary somewhat, causing slight differences in the solder bump height when reflowed. Electroplating solid solder alloy on the contact sites has significantly tighter thickness tolerances, however, plating is a slower process than printing and the plating thickness may not be uniform on all areas of the wafer. The result of this plating variation is, when the electro-plated contacts are reflowed, the contact bump height can vary by several microns from one die to another. To overcome these planarity concerns, a new interconnect solution has been developed. Tessera has recently introduced the "µPILR™", a unique substrate fabrication methodology that provides a very uniform array of raised solid copper contact features. These contact features are integrated onto the substrate interposer and have proved ideal for mounting very fine pitch bumped flip-chip semiconductor die.

This raised µPILR contact substrate process enables semiconductor developers to significantly reduce contact pitch on the die without reducing pad size. Solder bumped die are placed directly onto the raised contact features eliminating the need for solder printing on the package substrate. Mounting the bumped die element on this planer topography solves fundamental issues associated with electro-migration and avoids many of the current assembly process related defects. This is because the raised contact features provide a uniform package interconnect that furnishes a consistent standoff height for improving underfill flow control (even with low melt solders). For solderability, electroless nickel, immersion gold (ENIG) plating is applied over the solid copper contact surface (see Figure 3).

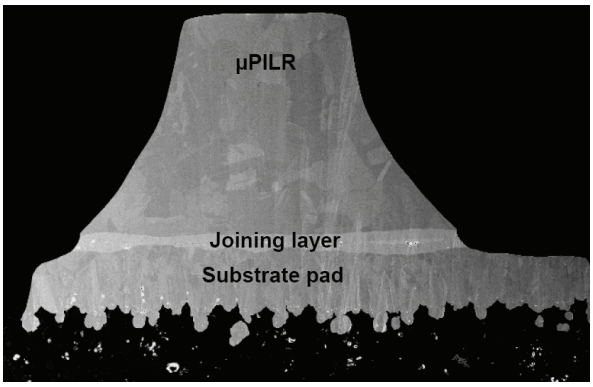
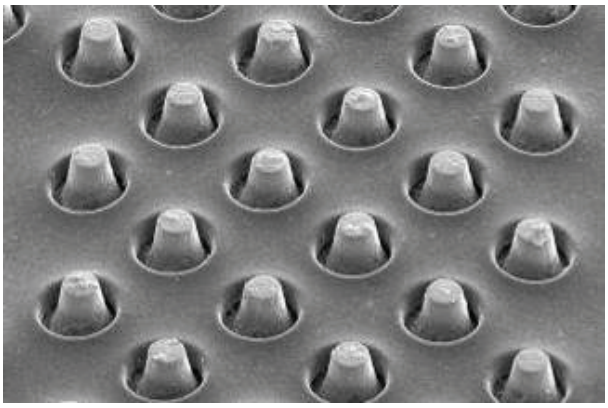


Figure 3. µPILR contact joined to land on substrate

The two step Ni/Au alloy combination has proven ideal for both eutectic and Pb-free solder attachment of the flip-chip die elements. And because the copper foil base for the µPILR is furnished with a uniform thickness, a near perfect planer surface is retained for mounting the solder bumped flip-chip die. The example shown in Figure 4 shows an array of raised contact features furnished on the top surface of the substrate interposer or PCB.



Source: Tessera

Figure 4. The closely spaced raised µPILR contact features provide very precise planarity.

The raised contact format provides a more uniform and viable solution for the finer-pitch flip-chip applications because it overcomes most of the assembly process variables. This is due to the precise standoff height and the slightly tapered profile of the solid copper contacts.

The µPILR flip-chip substrate evolved from a fabrication process originally developed for complex, single-die packaging and multi-layer substrates that were designed for high-density 3D package-on-package applications. The most common substrate fabrication processes utilized for direct flip-chip attachment typically begin with a multiple circuit layer, laminated glass reinforced epoxy-resin core structure typical of that shown in Figure 6.

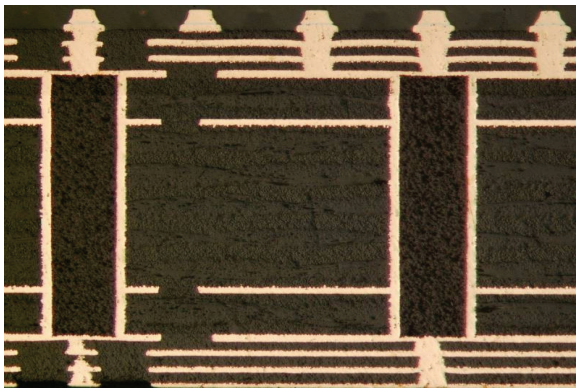


Figure 6. µPILR contact applied to a 3-4-3 build-up substrate for flip-chip mounting.

Additional circuit interconnects are provided by sequentially building-up layers of dielectric and copper. The final step in this sequential fabrication process is the application of a single layer of roller copper foil on the die-attach side of the interposer. The copper foil layer (ranging between 25µm and 75µm in thickness) is bonded onto the top surface of the substrate using a proprietary metal-to-metal joining process. In preparation for developing the µPILR features, a photo-resist material is applied over the copper foil, exposed and developed to define the specific array contact pattern. The uncoated copper is then ablated using standard chemical etching methodology. The remaining process steps include the application of the photo-imaged solder mask and subsequent plating of the exposed copper features to provide the flip-chip mounting sites.

As a practical test for the process and in cooperation with a major Silicon Valley semiconductor manufacturer and its substrate supplier, Tessera configured one of the companies' existing high-density interposer designs with the µPILR contact features. The test die replicated the physical outline and contact pattern of the semiconductor model. The non-functional vehicle developed for flip-chip-on-µPILR modeling and simulation included a face-down 20mm x 18mm x 1.75mm thick solder bumped die mounted onto a 40mm x 40mm x 1.25mm thick µPILR array configured substrate.

The example furnished in Figure 5 includes the top view of the package assembly and cross-section that clearly shows the finished solder joining of a bumped flip-chip die and µPILR contact.

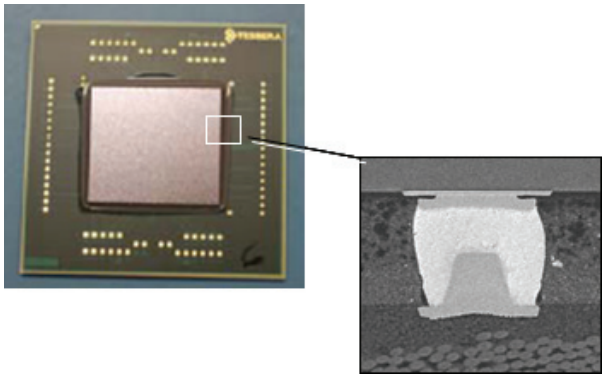


Figure 5. Bumped flip-chip to µPILR™ post reflow solder interface

Because of the wide co-efficient of thermal expansion disparity between the silicon die and the glass-reinforced polymer substrate structure noted above, stabilizing the die attach area with an epoxy based underfill is quite common. For this test vehicle, a commercial grade liquidus material was dispensed at two joining edges of the die allowing it to uniformly flow through the array to the opposite edges. The underfill material was then thermally cured at 160ºC for 60 minutes resulting in a void-free bonding between the die and interposer surfaces. Following the curing process for the underfill material, a heat spreader cap was attached using Indium as the thermal interface material (TIM) onto the backside (non-active) surface of the die element.

To meet the semiconductor company's qualification requirements an extensive reliability test program has been conducted at Tessera's development laboratories in San Jose, California. Beginning with finite element modeling techniques to identify potential failure mechanisms, the company was able to calculate and predict inelastic strain energy accumulated during thermal cycling. Industry standard approaches were then employed to conduct the actual physical testing. For this evaluation program, three lots were tested from -55ºC to +125ºC for 1000 thermal cycles. The results of the testing yielded zero failures, consistent with those predicted by the modeling. Furthermore, the testing was extended beyond thermal stress to include measurement for electro-migration.

Conclusion

Feature sizes for WLBGA and DSBGA packages will continue to shrink as the silicon fabrication technology adopts significantly higher circuit densities. This trend will allow the IC designer to further compress the functionality onto even smaller die outlines. To maintain the minimal finished package outline it will be necessary to reduce the contact size and move the contact features closer together. We can expect the next generation of these components to push the limits of printed circuit fabrication capability. In preparation for higher density circuit boards, designers and suppliers will need to work together in selecting the best laminate materials and adopt more advanced fabrication processes. Even today, the higher density circuit routing and minimal spacing of the contact features are very near the size of early semiconductor technology, prompting circuit fabrication specialist to employ more sophisticated clean-room enclosures around advanced photo lithography processes.

As the die I/O increases and the contact pitch decreases on the uncased flip-chip configured die, users will need to consider how to achieve the most reliable and efficient solution for both mounting and circuit routing.

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References:

1. IPC-7094, '*Design and Assembly Process Implementation for Flip-Chip and Die Size Components'*
2. IPC-2220, *'Design Standard Series including IPC-2221, IPC-2222, IPC-2223 and IPC-2225'*
3. IPC-2226, *'Design Standard for High Density Interconnect (HDI) Printed Boards'*
4. JEDEC Publication 95 Section 4.7,'*Die-Size Ball Grid Array Package (DSBGA')*
5. JEDEC Publication 95 Section 4.18, '*Wafer Level Ball Grid Arrays (WLBGA)'*

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- As die complexity increases, however, we are faced with a several challenges:
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  - Thermal management
  - Circuit routing optimization

Addressing primary concerns-

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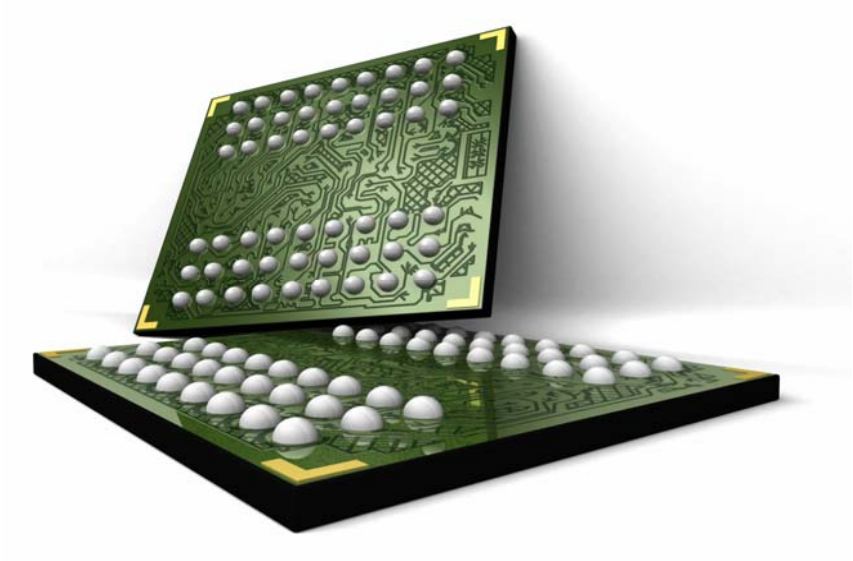

Example source: Micron Technologies

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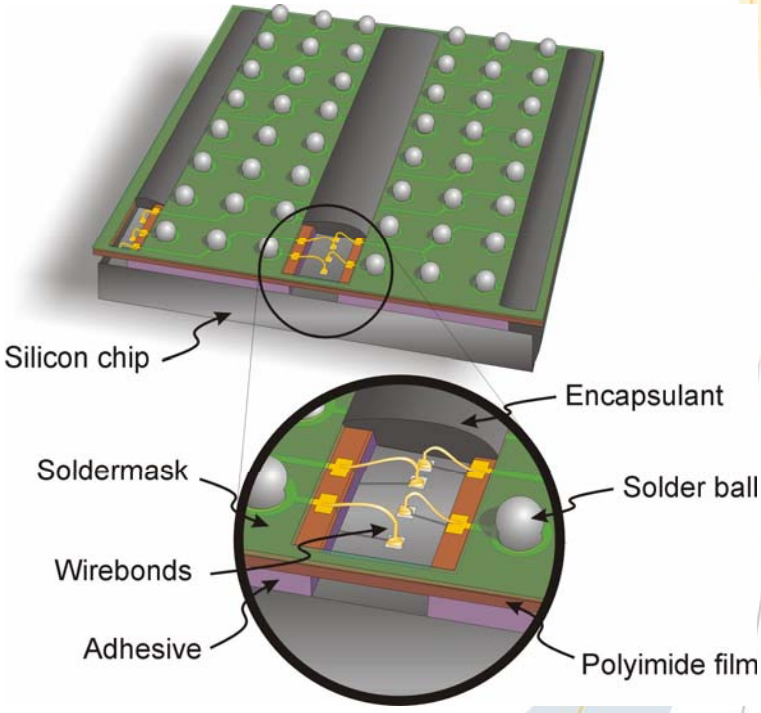
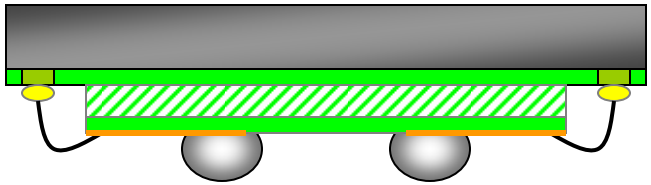
  - The size of the substrate or carrier is as close to the die size as practically possible.

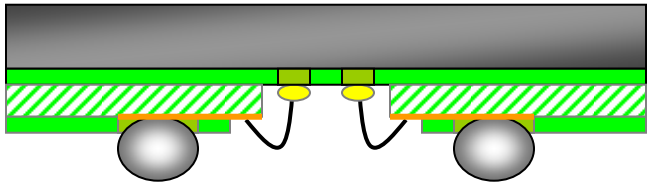


Example source: Tessera

DSBGA package assembly variations



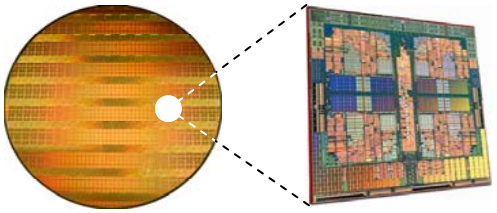
DSBGA w/ perimeter bond pad

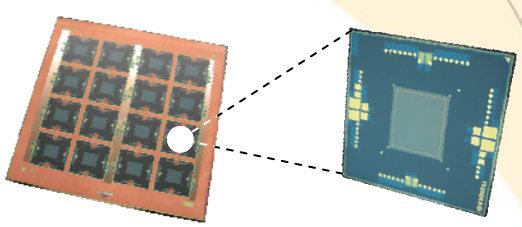


DSBGA w/ center bond pad

Following die attach and wire-bond processing, the wire-bond area is encapsulated with a dielectric polymer material.

Flip-Chip packaging challenges

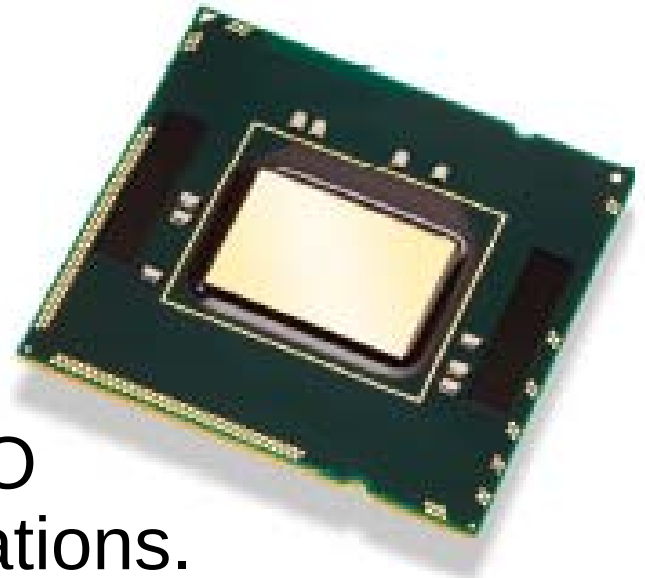




	Chip	Substrate
Power delivery	• Feature scaling • High-k dielectrics • Multi-core processors	• Lower inductance • ground and power • Decoupling passives
Signal speed, bandwidth	• Internal/external IO • Low-k dielectrics • Cache size/positioning	• Feature sizes and tolerances • More IO • Memory proximity
Thermal management	• Hot spots • Interconnect resistance • Load balancing	• High thermal conductivity IO • Short routings • Hot-spot spreading
Electromigration and reliability	• Current draw and field at joint • Low-k dielectric fracture toughness	• High electrical conductivity IO • Low CTE dielectrics • Low temp flip-chip joining

- Flip-chip technology has traditionally been limited to very specialized applications.
  - The process has historically served as the main interconnect method in direct-die attach packaging.

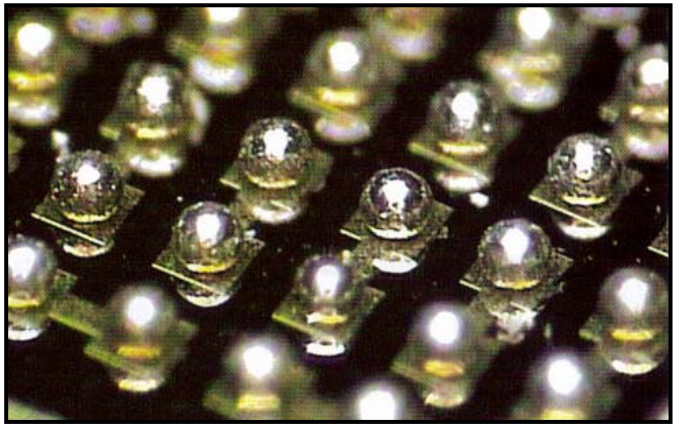
- With the current need for smaller package outlines, flip-chip has gained in acceptance, most recently for a number of very high I/O consumer electronic applications.



Intel CORE i7

Die Level Redistribution

- To better enable flip-chip mounting of the higher density and higher I/O semiconductors, companies are adding copper conductor layers on the die surface to provide a more uniform array contact format.



Source: BTU

The solder bumped array configured contact is more easily accessed on the mating interposer substrate.

Contact Application Process

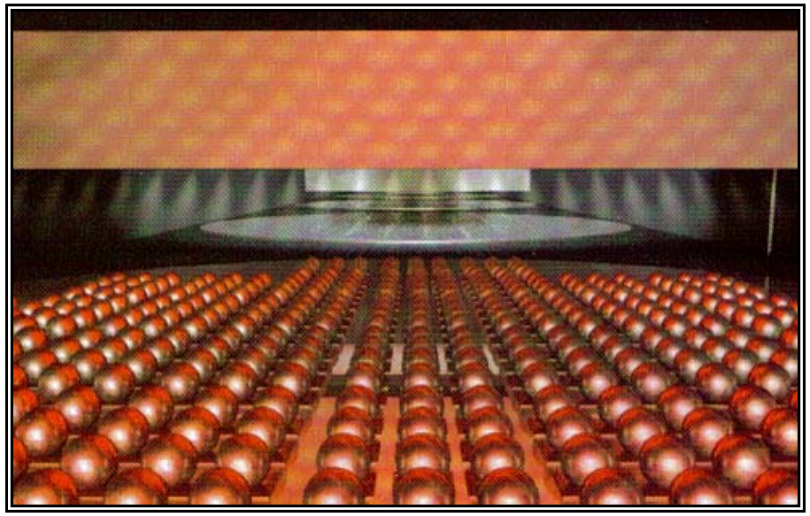
- A majority of the flip-chip and die-size packaged devices will be furnished with solder alloy bumps or solid solder ball contacts.
- Process variations:
  - electro-plating process
  - solder deposition
  - placement of individual preformed ball contacts.
- These processes require a mass reflow process to complete the forming or joining of the finished bump or ball contact.

Solder Alloy Selection

- The choice of solder alloys is determined by the requirements of both process and reliability.
- If the product is to be in compliance with RoHS, a Pb-free alloy composition will be mandatory.
- The most common lead-free alloy compositions include:
  - tin and silver (Sn/Ag),
  - tin and copper (Sn/Cu), tin, silver and copper (Sn/Ag/Cu)

More complex alloy combinations may include elements of bismuth, zinc and even antimony.

- Although several methods have been developed for furnishing solder compatible contact features directly on the die surface...
  - The most common and economical process simply deposits or plates and reflows a solder compatible alloy at each contact site.



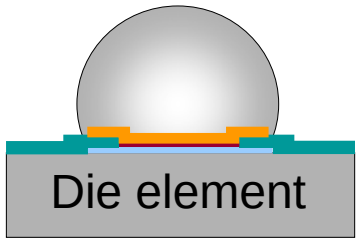
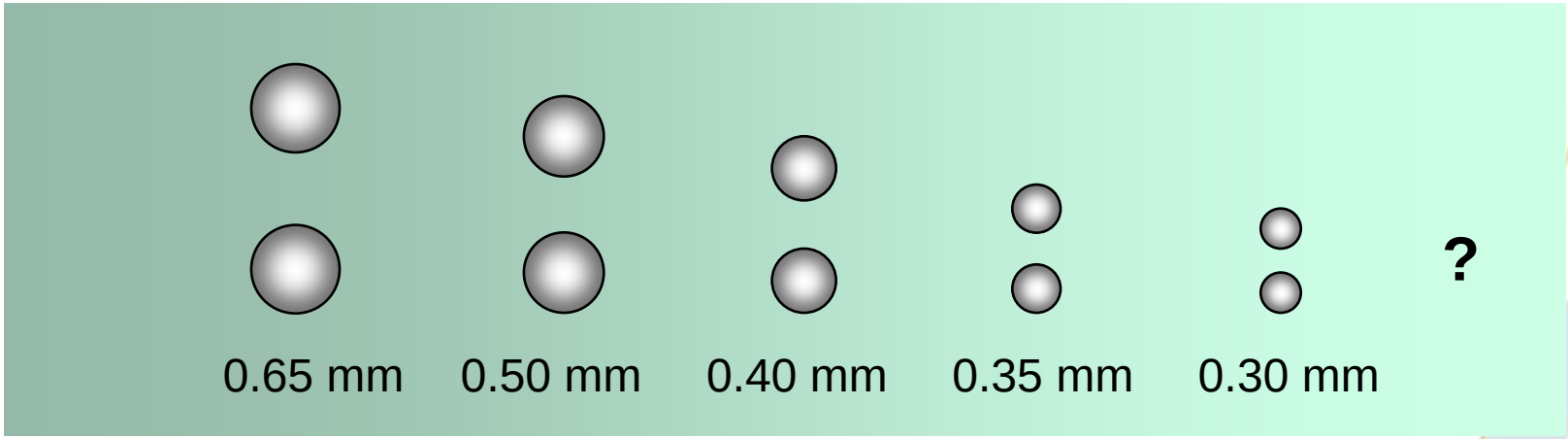


Photo source: BTU

Substrate and PC Board Level Assembly Processing

- Current generations of high density wafer fabrication processes are providing significantly smaller die in relationship to the number of contacts traditionally needed for electrical interface.



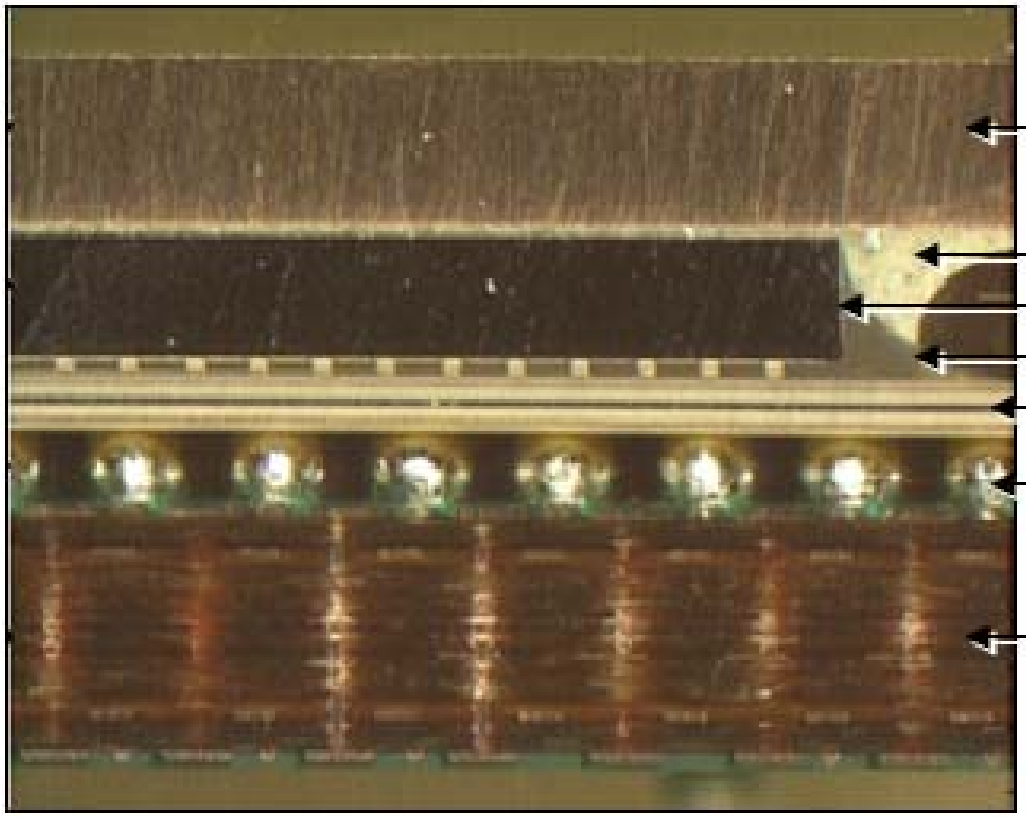
  - The ‘die-shrink’ factor forces the semiconductor company to further reduce wire-bond pitch.

- The IPC-7094 standard suggests that the minimum bump pitch be no less than 250 microns when possible to facilitate the assembly of standardized substrates.
  - Many bumped die, however, may be furnished with a contact pitch as close as 100 microns.
  - When this occurs, the product designer should be aware of the potential for contact-to-contact, contact-to-trace, and trace-to-trace shorting.
- Whether using a common perimeter solder bump layout or designing an array footprint format, the package designer is entrusted to position the power, ground, signal, and clock I/O locations with respect to optimizing performance of the host package interposer or substrate structure.

Addressing Next Generation Semiconductors

- The more advanced microprocessor and ASIC semiconductor packaging will require several thousand I/O contacts and they are expected to expand contact I/O by 30% in the very near future.
  - Consistent die-to-substrate interface, however, remains the most critical barrier in achieving optimum assembly process yield.
- Semiconductor suppliers have been forced to abandon wire-bond package assembly altogether, opting for the more compact die face-down flip-chip attachment methodology.

High Density Flip-chip on interposer application

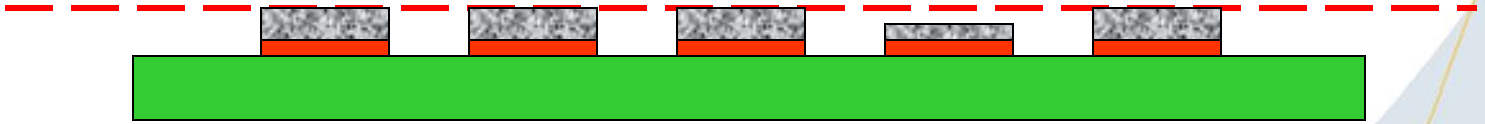


Source: IBM

Board or Substrate Assembly

- Attachment variations:
  - Solder paste print, place and reflow
  - Dip-flux, place and reflow
  - Dip-paste, place and reflow
- To ensure print registration and placement accuracy the process equipment will require vision assisted robotics.

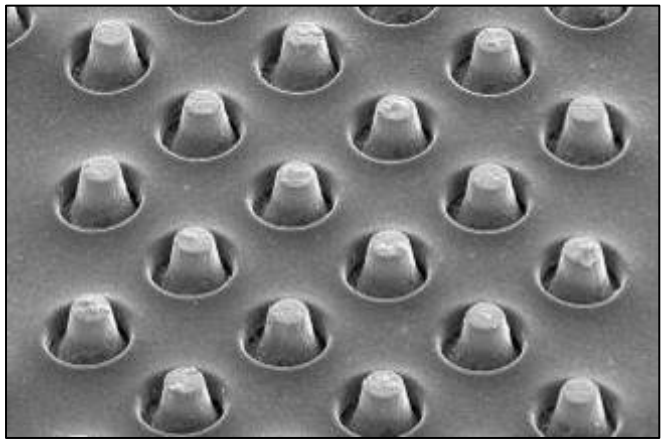
- There are two issues that continue to impede defect free joining of the high-density flip-chip die to the interposer substrate;
  - solder bump uniformity on the die
  - substrate flatness
- Deposition or stencil printing of solder paste on the substrate contact sites can have variables as well.



- The solder paste material, whether deposited or printed, is comprised of both solid alloy particles' and flux.
  - Depending on the powder size, the ratio of solids to flux can vary causing slight differences in the solder bump height when reflowed.
- Electroplating solid solder alloy on the contact sites has significantly tighter thickness tolerances, however, plating thickness may not be uniform on all areas of the wafer.
  - When the electro-plated contacts are reflowed, the contact bump height can vary by several microns from one die to another.

Planarity Solution

- To overcome planarity concerns for high density flip-chip a new interconnect solution has been developed that provides a very uniform array of raised solid copper contact features.

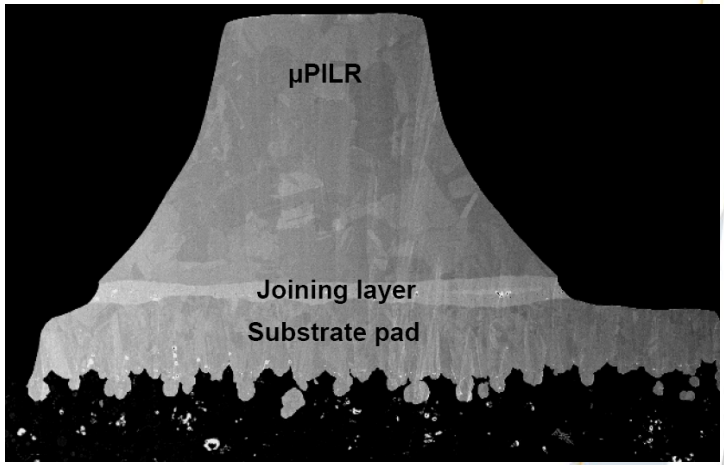


Example source: Tessera

The µPILR™ contact features are integrated onto the substrate interposer, ideal for mounting very fine pitch bumped flip-chip semiconductor die.

- Mounting the bumped die element on this planer topography solves fundamental issues associated with electro-migration and avoids many of the current assembly process related defects.

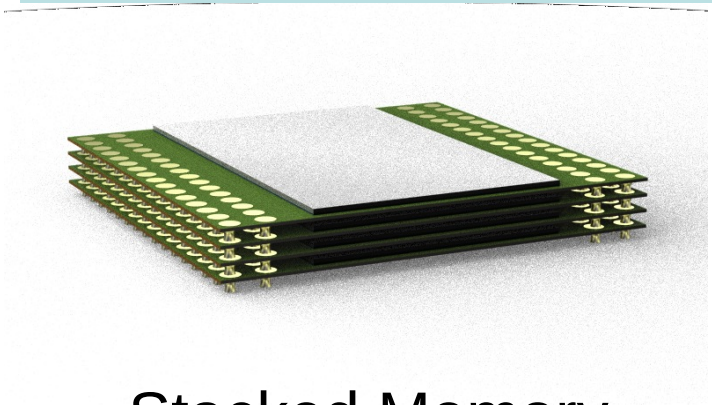
This is because the raised contact features provide a uniform package interconnect that furnishes a consistent standoff height.



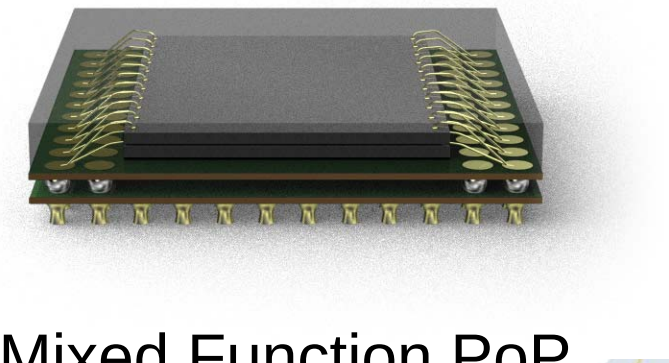
µPILR™ Contact Profile

µPILR Evolution

- The µPILR flip-chip substrate evolved from a fabrication process originally developed for complex, high-density 3D package-on-package applications.

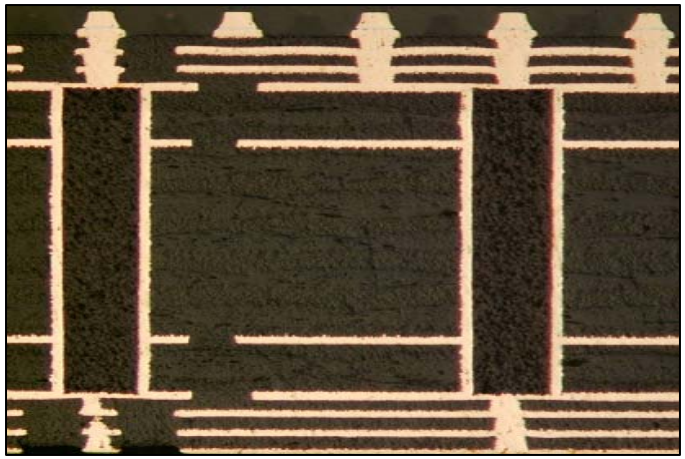


Stacked Memory



Mixed Function PoP

- Direct flip-chip attachment typically begin with a multiple circuit layer, laminated glass reinforced epoxy-resin core structure



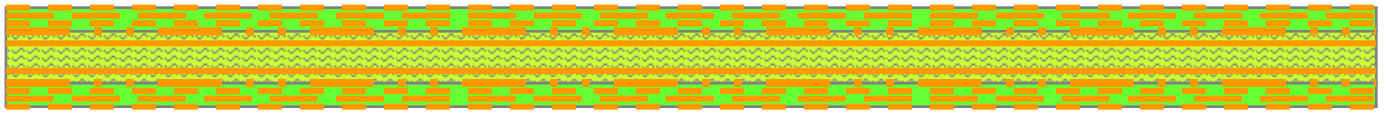
Additional circuit interconnects are provided by sequentially building-up layers of dielectric and copper.

A copper foil layer (ranging between 25 and 75 micron thickness) is bonded onto the top surface of the substrate, coated with resist, pattern photo-imaged and chemically etched.

µPILR substrate fabrication sequence

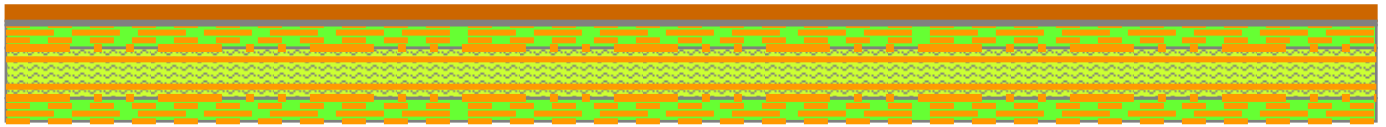
3-4-3 Substrate base

1



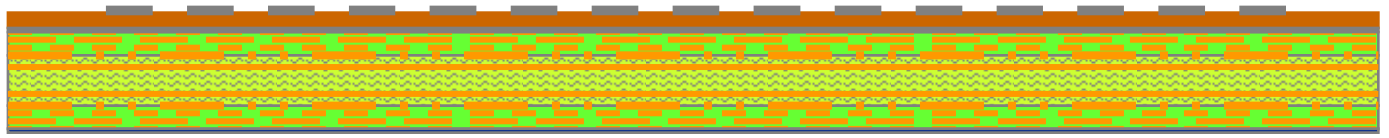
Four layer glass reinforced B-T core with three build-up layers on both sides

2



25-75 m thick copper foil is bonded to top surface of base substrate

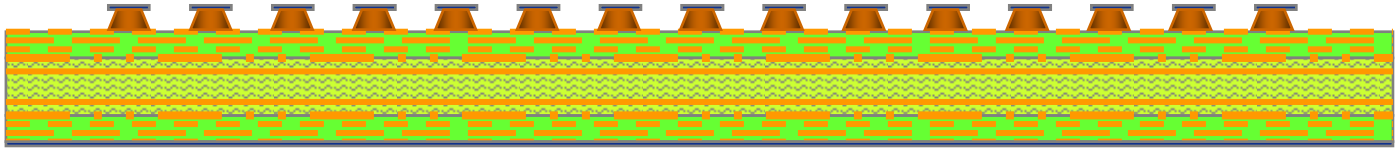
3



Resist is applied to the copper surface, exposed and developed

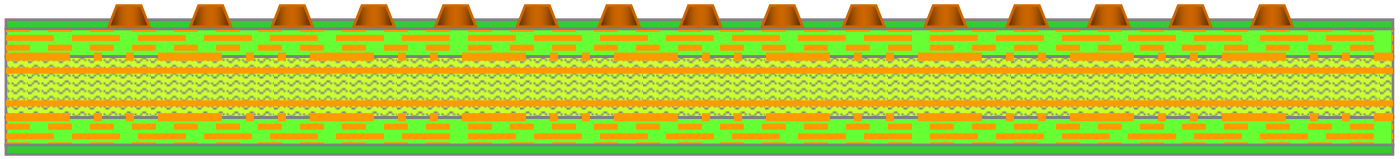
substrate fabrication sequence continued…

4



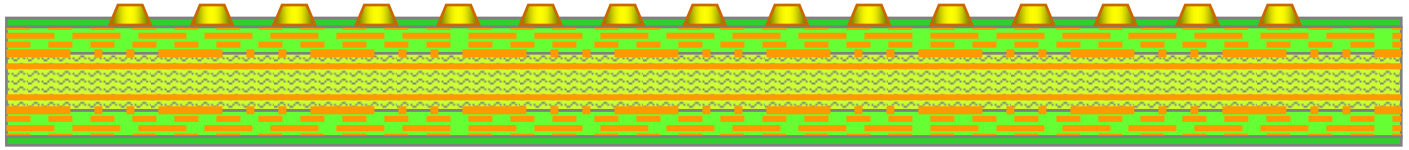
Exposed copper foil is chemically ablated

5



Etch resist is removed and photo-imaged solder mask applied

6

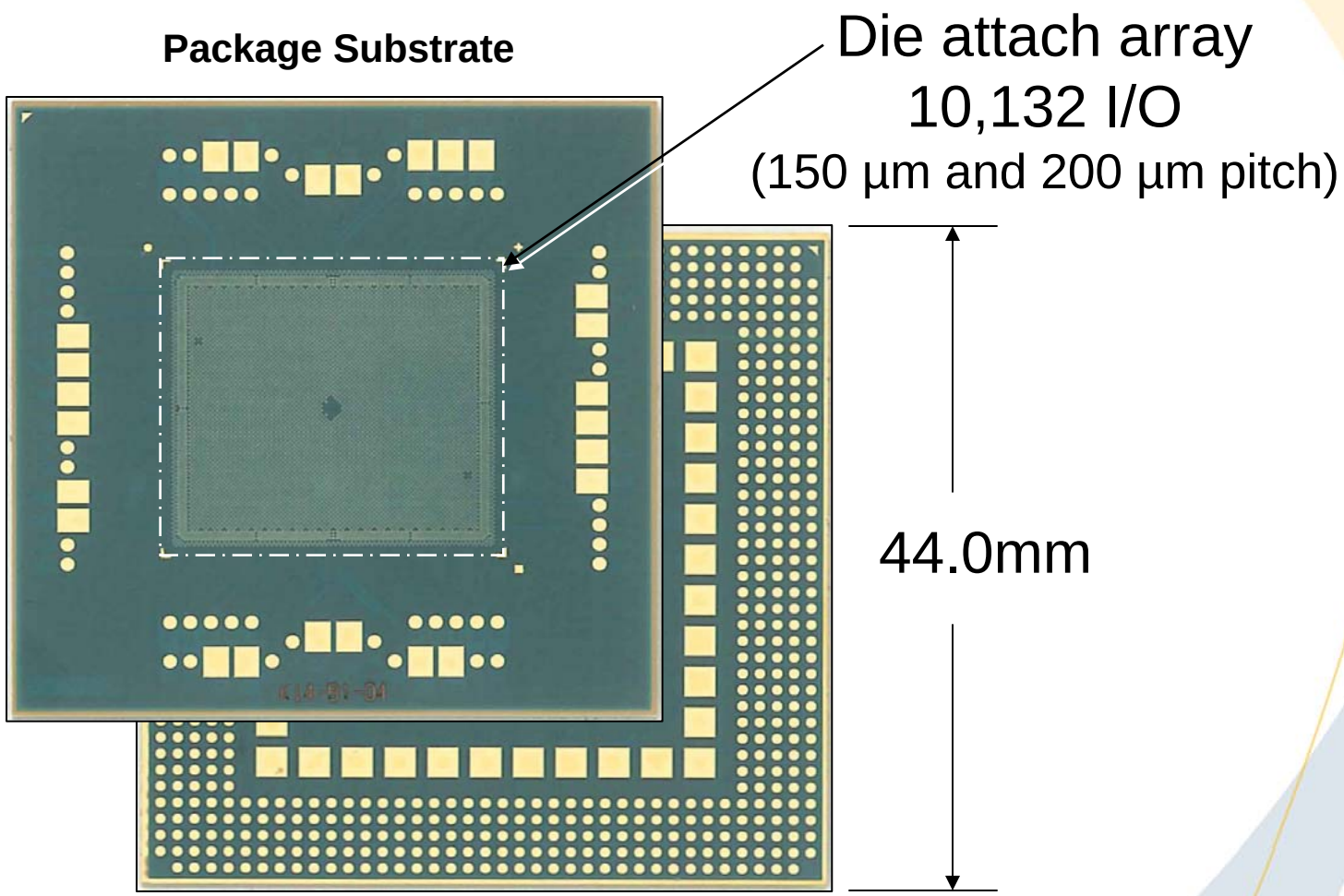


Contacts are ENIG plated and ready for solder bumped flip-chip mounting

µPILR Process Verification

- In cooperation with a major Silicon Valley semiconductor manufacturer and its substrate supplier, Tessera configured one of the companies' existing high-density interposer designs with the µPILR contact features.
- A test vehicle was developed for modeling and simulation
  - 18mm x 20mm x 1.75mm thick, solder bumped die
  - 40mm x 40mm x 1.25mm thick 3-4-3+ µPILR configured substrate.

Resulting interposer substrate



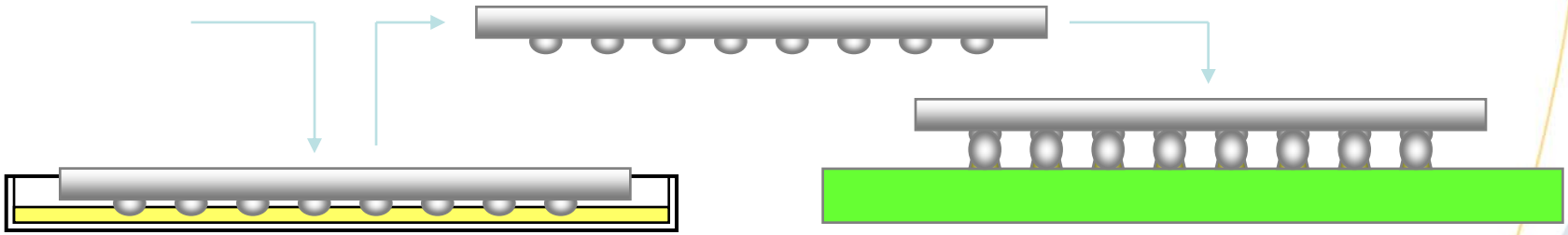
Requirements for flip-chip mounting

JUKI CX-1

- Placement of the bumped die to the µPILR interposer or µPILR configured host circuit board can utilize a standard die-attach system or any SMT assembly system having ~20 micron placement accuracy.

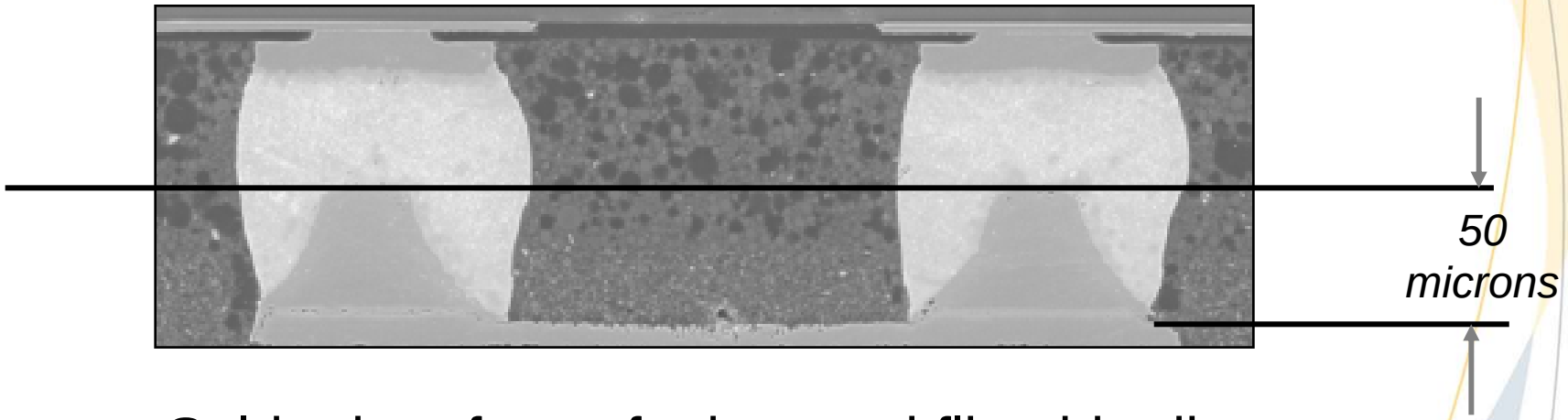
Placement and joining

- The die-to-substrate assembly process begins with the transfer of the alloy bumped die element from their carrier tray or wafer carrier to a shallow flux reservoir tray.
- A precise level of the flux is maintained in the tray so that only the lower half of the bump contact is coated.



- Following the flux coat process, die are aligned and placed on top of the µPILR contact and reflow soldered to complete the joining process.

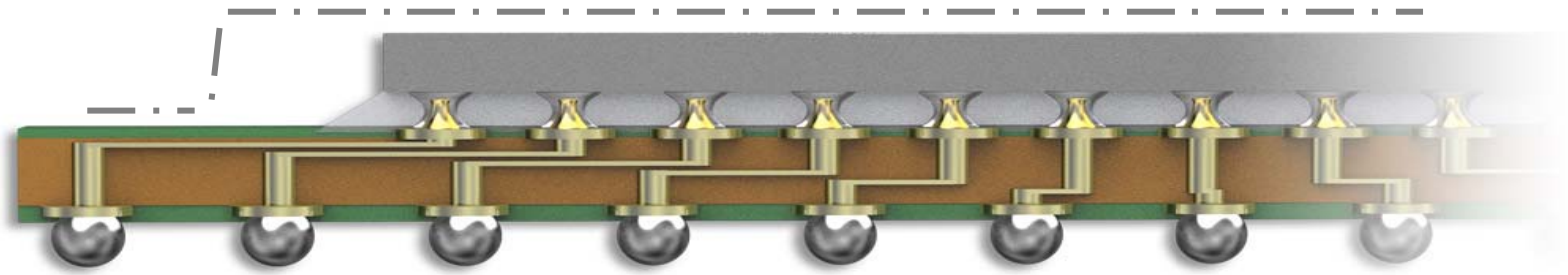
Post reflow solder joint profile analysis



Solder interface of a bumped flip-chip die mounted onto a µPILR™ configured interposer.

Solder ball attachment

- The 300 µm diameter Pb-free pre-formed solder ball contacts are placed onto a pre-fluxed land array and reflow soldered using a forced air/gas convection furnace.

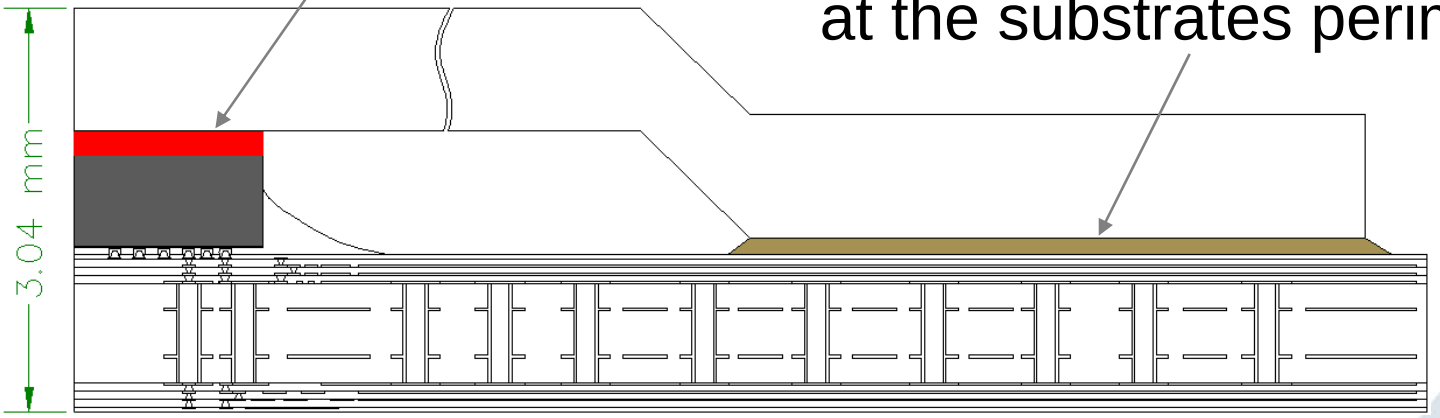


- Following the solder ball reflow process, the finished package is cleaned, tested, underfill applied and the heat spreader attached.

Heat spreader mounting

The heat spreader was attached to the back surface of the die using an Indium alloy composition as the thermal interface material (TIM).

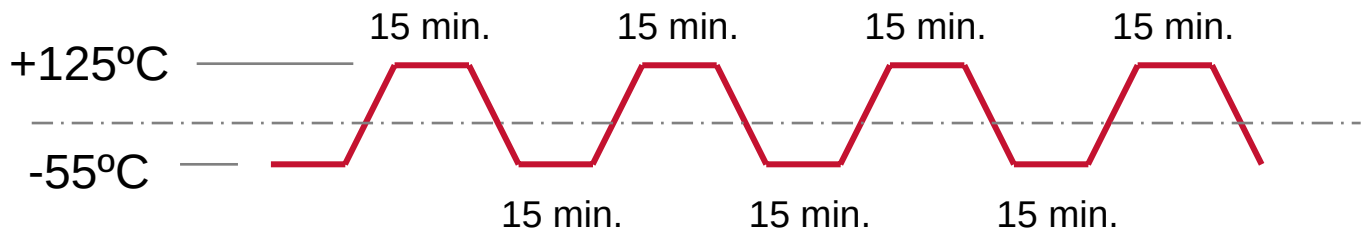
A polymer based bonding material retained the heat spreader at the substrates perimeter

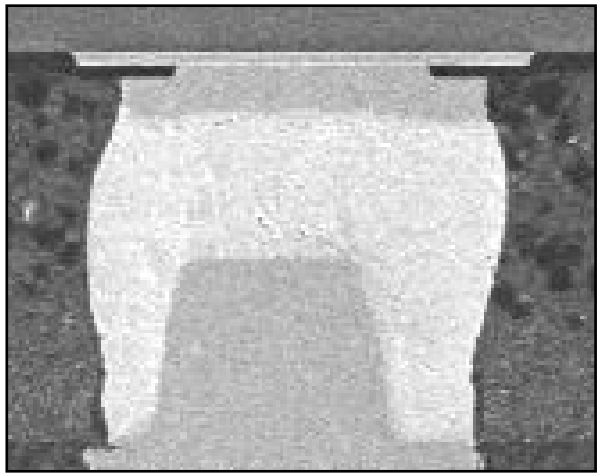


Package Cross-section

Thermal shock test results

- Three lots were tested for 1,000 cycles
  - No interface failures detected





Cross-section of contact interface after 1,000 thermal shock cycles

Summary

- Feature sizes for WLBGA and DSBGA packages will continue to shrink as the silicon fabrication technology adopts significantly higher circuit densities.
- This trend will allow the IC designer to further compress the functionality onto even smaller die outlines.
- To maintain the minimal finished package outline it will be necessary to reduce the contact size and move the contact features closer together.

Summary cont….

- We can expect the next generation of these components to push the limits of printed circuit fabrication capability.
- In preparation for higher density circuit boards, designers and suppliers will need to work together in selecting the best laminate materials and adopt more advanced fabrication processes.
- As the die I/O increases and the contact pitch decreases on the uncased flip-chip configured die, users will need to consider how to achieve the most reliable and efficient solution for both mounting and circuit routing.

Example source: Intel

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