A Strategy for Via Connections in Embedded Sheet Capacitance Designs

J. Lee Parker, Ph. D.
JLP Consultants
Mechanicsville, Virginia
Leep001@msn.com

Abstract
Predicting the electrical performance of embedded capacitor PCB designs has been a major stumbling block for the technology. In particular, one of the key questions has been how quickly can charge be delivered to a device from the embedded capacitor. As pointed out in earlier papers (1, 2) the major attenuator is the via connection between the ground plane and the embedded capacitor. These studies determined the performance when all of the charge is delivered through a single via. The index of performance for these investigations was the time constant associated with the capacitor's discharge. It was found that a major reduction in inductance and hence the time constant could be achieved by minimizing the barrel length of the via; usually using blind vias.

The core of this paper examines other techniques for reducing the effective time constant and thereby improving performance. A potential strategy is using multiple vias between the device and the embedded capacitance. The analysis consists of developing a mathematical model of the circuit using the "lumped sum" approach commonly used in most electronic circuit analysis. With the model, we are able to predict the performance of the embedded sheet capacitor with multiple vias. Potential avenues for performance enhancement can then be identified.

Introduction

There are presently several techniques for forming a buried capacitor in the core of a multilayer board. For purposes of this discussion, attention will be directed toward a sheet capacitor; although most of what is presented below can be extended to the other techniques as well.

A buried sheet capacitor is essentially a thin innerlayer. The core is composed of an organic material often reinforced with a woven glass structure. A classic example is FR-4. The laminate extends over the entire board and is essentially a very thin innerlayer. The copper weight is normally one ounce and the thickness of the dielectric is typically two mils or less. The innerlayer is biased top to bottom thus creating a large capacitor in the interior of the multilayer board. Except for through holes connecting pads and antipads the innerlay is normally not imaged. A cross-section is depicted below:

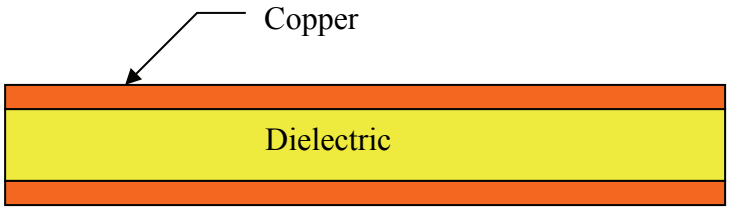


Fig 1. Sheet Capacitor Structure

The purpose of this technology is to offer the designer a technique for EMI suppression and an alternative to the by-pass capacitors normally mounted on the surface of the board to minimize "voltage sag" in the power being supplied to the active devices. A more complete discussion of the electrical performance will follow later.

Material Description

The parameter of primary interest in this construction is the capacitance per unit area of material. Typical values of the unit capacitance and other parameters are shown in the Table (1) below.

Table 1. Electrical Properties of Typical Buried Capacitor Materials

Material	Dielectric	Thickness	Capacitance

	Constant	Microns	pF/cm^2
A	3.1	12.5	216
B	3.1	25	108
C	4.1	25	143
D	4.1	50	71
E	18	8	1962
F	18	16	981

Potential Advantages and Limitations

There are potentially two major incentives for using a buried capacitance PCB design. The first is a reduction in EMI radiation. Buried capacitor innerlayers will reduce EMI radiation and often offer a simple solution to what can be a difficult and time consuming issue.

The second advantage is a reduction in the number of bypass capacitors required by a design to over come "droop" in the power delivered to an active device. Reducing the number of bypass capacitors obviously results in additional routing space on the outer layers of the board. This can result in a reduction of board size or even innerlayer count; both of which reduce the cost of the board. Other advantages are a reduction in assembly cost, a decrease in the number of components, not to mention fewer solder joints which results in improved reliability.

The issues associated with buried capacitance are design tools, board material cost and fabrication. Also the number of potential fabricators is limited and some due diligence should be performed by the OEM to be certain any patent issues are resolved. The designer should also carryout "sanity checks" to verify the buried capacitance design will deliver the charge required to power the devices and that the design is compatible with the frequencies associated with the board. A few simple calculations described below will normally uncover any potential issues of this nature.

Design Issues

A paramount issue inhibiting the use of buried capacitance is a design procedure which will insure that the required charge will be delivered to a device within the time allotted by the switching cycle. The major issue here is depicted in Figure 3 below.

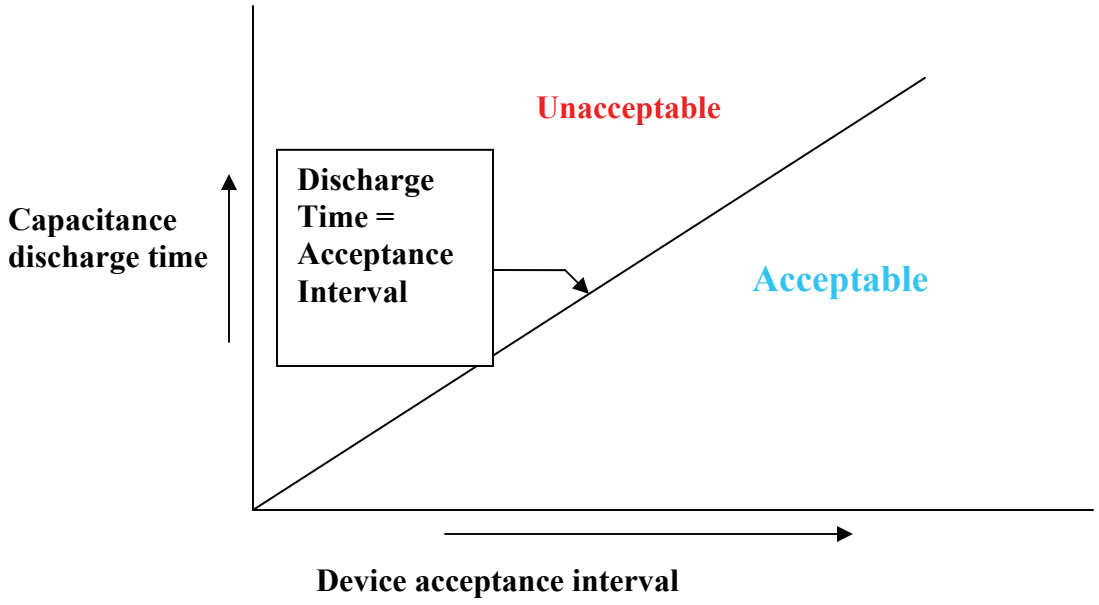


Figure 3

In particular, the discharge time of the capacitor (i.e. buried capacitance) must be less than the acceptance interval as dictated by the device switching frequency.

The well known relationship between frequency and period is shown below in Figure 4.

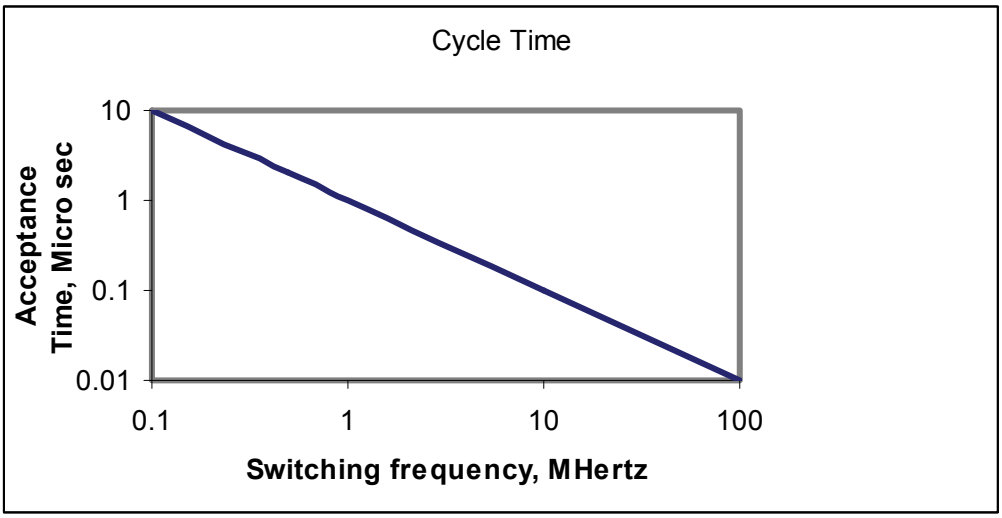


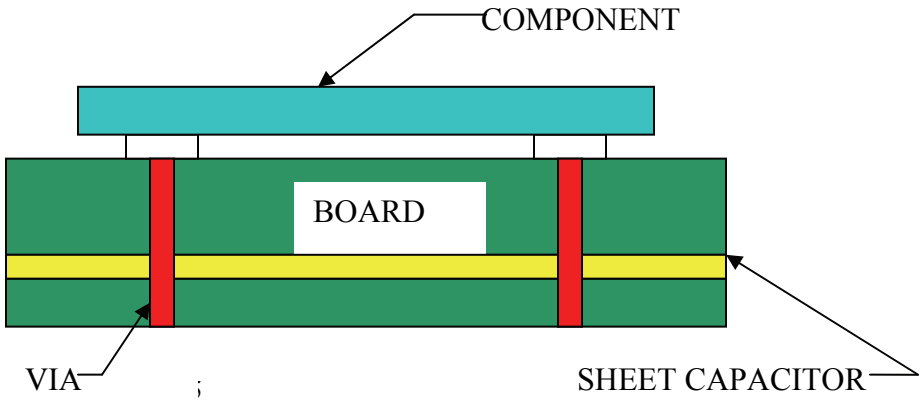
Figure 4

Typically, the switching frequency for the power cycle of a device is in the kilohertz – megahertz range. Consequently the time available to deliver charge from the buried capacitance layer to the device is on the order of microseconds.

At the board level there is little that can be done to overcome the limitations imposed by the devices. So it becomes an issue of designing the PCB to be compatible.

Board design

A drawing of the buried sheet capacitor concept is shown in Figure 5.



In Reference 1, the electrical loop connecting the buried capacitor to the device is modeled as a lumped sum "LCR" circuit. From this analog a relationship is developed for the discharge of buried capacitance

$$Q = Q_O \exp(-t/\tau)\cos(\omega t - \theta) \qquad (1)$$

Where Q is the charge delivered from the buried capacitor to the device
Q_O is the initial charge of buried capacitor

t is time

$\tau = L / R$ (time constant)

L is the inductance and R the resistance of the circuit.

ω is the frequency

θ is a constant

As seen the transfer of charge is controlled by the time constant τ. The major contributor to the time constant is the inductance, in this case the inductance of the vias connecting the buried capacitance planes to the device (see Reference 1).

The inductance of a via is discussed in Reference 2 and shown to be

$$L = 5.08h\left[\ln(\frac{4h}{d}+1)\right] \text{ nH} \qquad (2)$$

For a via with a 13 mil diameter in a 62 mil board the inductance is

L=1.2 nH (3)

The charge decay between the buried capacitor and a device connected by the via described above is shown in Figure 6.

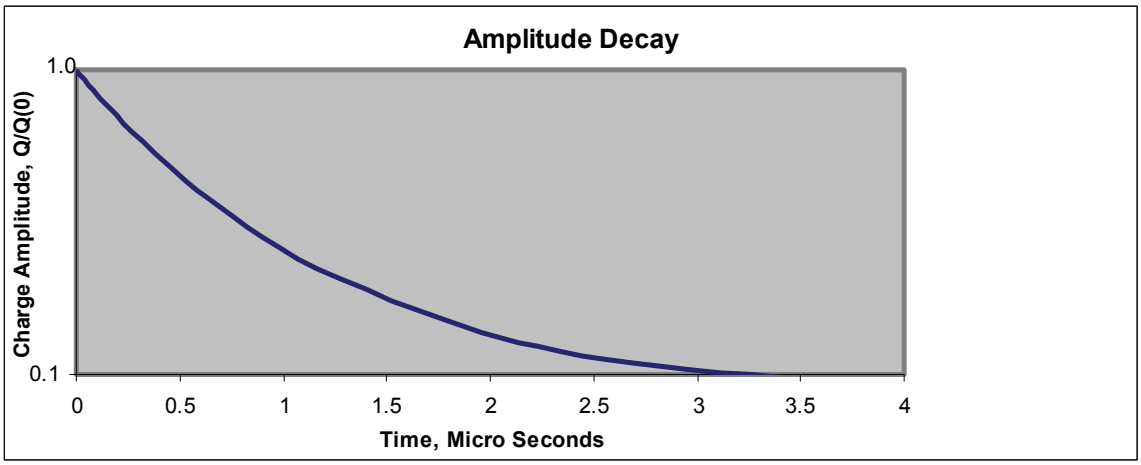


Figure 6

In this case approximately ninety percent of the charge is delivered after 3 micro seconds. While this is adequate for devices with a switching frequency in the high kilohertz range it may not be adequate for devices operating in the megahertz range.

The issue then becomes how to increase the delivered charge per unit time.

As discussed below, a substantial improvement can be achieved by incorporating multiple power connections to the device as shown in Figure 7.

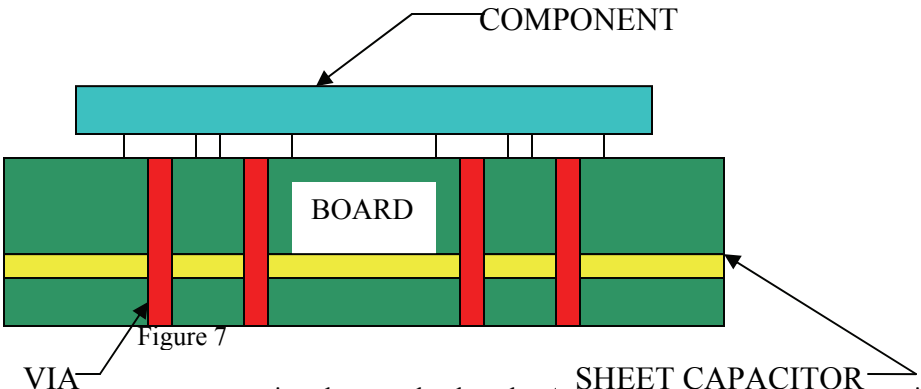


Figure 7

The buried capacitor c[illegible]t capacitor that may be thought of [illegible]ical charge. With this in mind, each via connecting the sheet capacitor to a device essentially operates uninfluenced by the other vias. This being the case, when a particular device is connected to the sheet capacitor using multiple vias each connection can be modeled as an independent electrical loop each governed by equation 1.

Consequently, the total charge delivered is

$$Q = NQ_O \exp(-t/\tau)\cos(\omega t - \theta) \qquad (4)$$

where N is the number of vias connecting the device to the sheet capacitor. Notice that while multiple vias will increase the charge delivered per unit time it does not influence the time constant τ. The result is summarized in Figure 8.

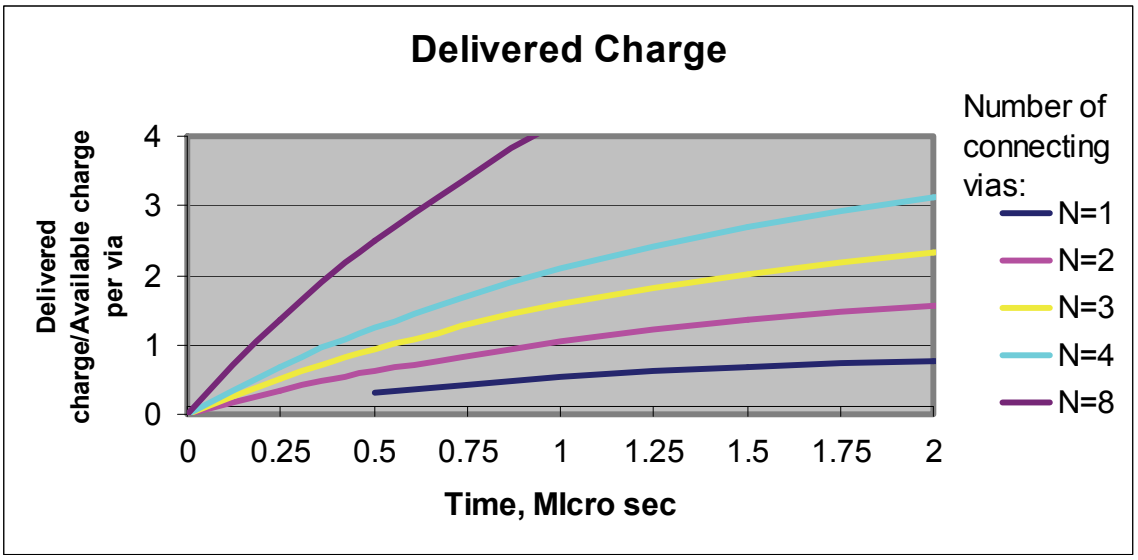


Figure 8

Obviously, a multiple connection strategy will appreciably increase the charge delivered to the device at any given time in the cycle. For instance, at one microsecond into the switching cycle a single connection will discharge approximately half of the available charge for that connection. If four connections are made to the sheet capacitor using four separate vias, the delivered charged is increased by a factor of four.

Summary

The amount of charge delivered to a device from a buried sheet capacitor per unit time can be appreciably increased by using a multiple connection (via) strategy. At the same time the actual time constant for the charge transfer is unaffected. By using a multiple connection strategy the amount of charge demanded by the device within the switching cycle should be satisfied by a buried sheet capacitor.

References

1 Parker, John Lee, "An Analytical Analysis of the Discharge of a Buried Sheet Capacitor Using a LCR Analogy"

2 Johnson and Graham, High Speed Digital Circuits, Prentice Hall, 1993

A Strategy for Via Connections in Embedded Sheet Capacitors

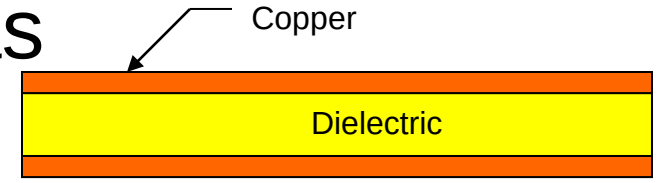
by
J. Lee Parker, Ph.D.
JLP Consultants, LLC
leep001@msn.com

Topics to be Discussed

- Buried sheet capacitor
- Advantages and disadvantages of buried sheet capacitors
- Design issues
- Performance of buried sheet capacitors
- Performance comparison using multiple power vias
- Observations

The Buried Sheet Capacitor

- Dielectric is usually an organic material
  - Often using a woven glass
  - *i.e.* FR4
- Each side of laminate is bonded to a continuous sheet of copper
- Imaging is typically connecting pads and anti-vias



Sheet Capacitor Structure

Electrical Properties of Buried Capacitor Materials

Material	Dielectric Constant	Thickness (microns)	Capacitance pF/cm^2
A	3.1	12.5	216
B	3.1	25	108
C	4.1	25	143
D	4.1	50	71
E	18	8	1962
F	18	16	981

Design Purpose of Embedded Capacitance

- EMI suppression
- Minimize “power droop” in power signal delivered to active devices
- Thereby provide an alternative to placing by-pass SMT capacitors on the outer layers

Potential Advantages

- Additional routing space becomes available on the outerlayers
- Potential Result
  - Decrease in board size
  - Decrease in number of innerlayers
- Reduction in number of components
- Reduced assembly cost
- Reduction in number of solder joints

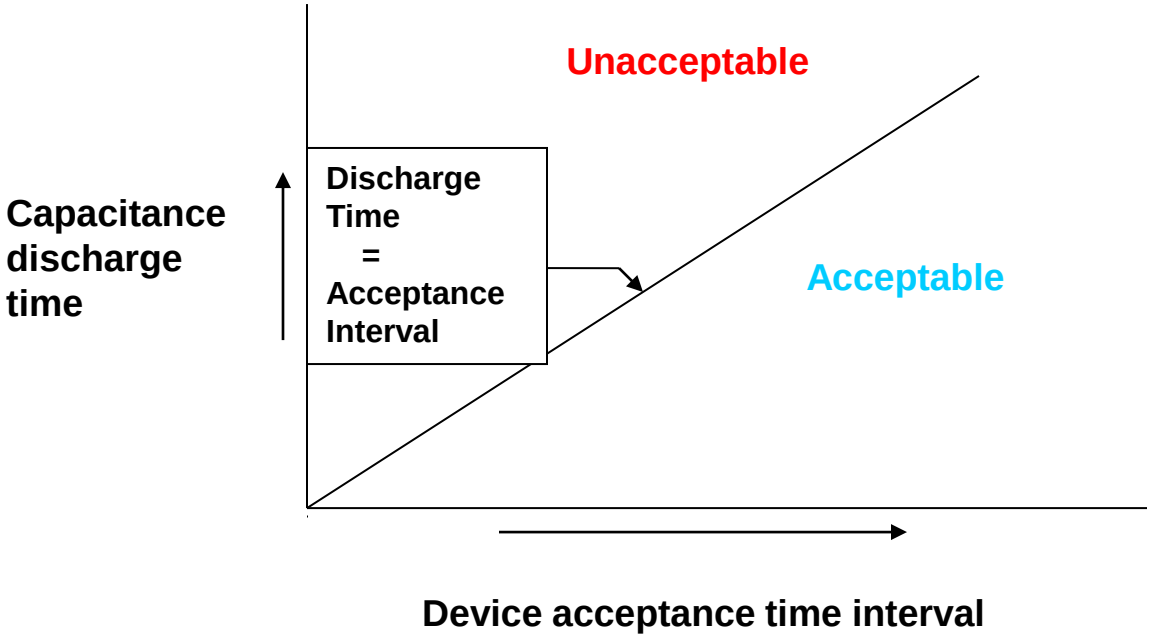
Potential Issues

- Availability of design tools
- Limited number of fabricators especially in Asia
- Patent issues (some due diligence should be practiced by OEM)

Design Analysis

- Compatibility between device acceptance window and charge delivery time
- Determine the duration of the acceptance window
- Determine time required for buried sheet capacitance to deliver charge to device

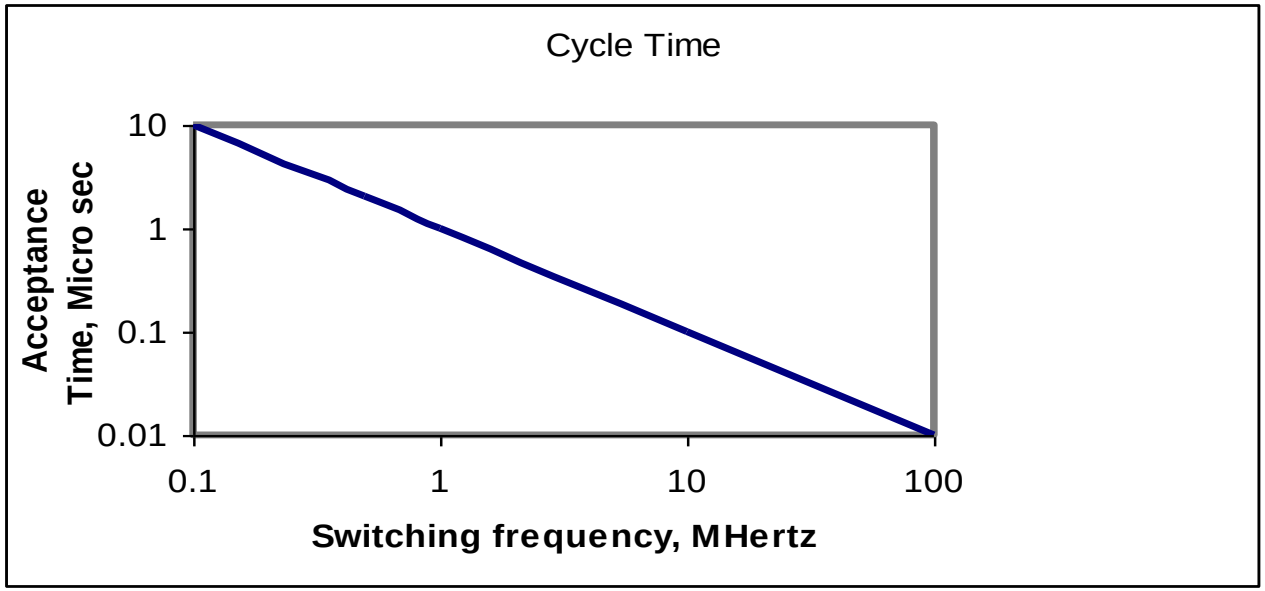
Compatibility Match Between Device and Buried Capacitor



Design Analysis

- Device acceptance window is dependent upon the switching frequency
- Delivery time is controlled by board circuitry between device and sheet capacitor

Device Cycle Time

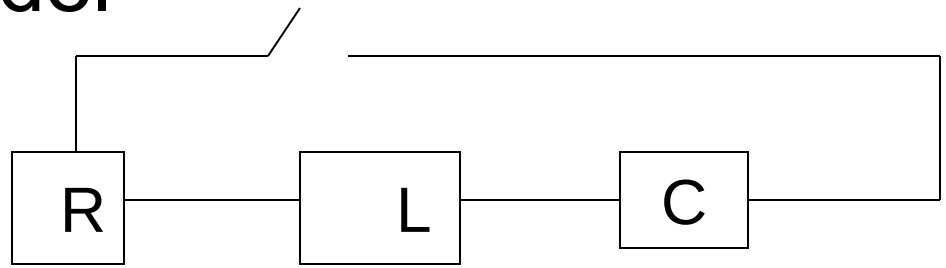


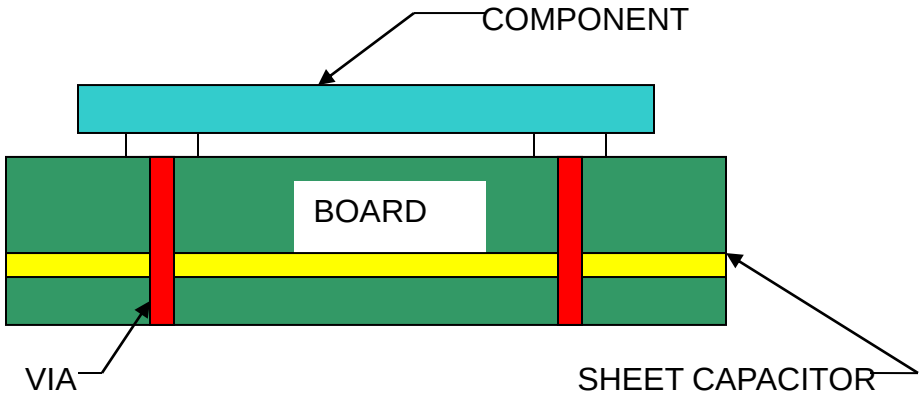
Design Analysis

- Typical switching time of power cycle is in the range of kilohertzs-megahertz
- Consequently time available for charge to be delivered is of order microseconds
- Sheet capacitor delivery time must now be determine to assess design compatibility

Design Analysis
Single Power Connection

circuit analysis: use a “lumped sum model”





Design Analysis
Single Power Circuit

- In Reference 1 of the text it is shown the charge delivered is

$$Q = Q_O \exp(-t/\tau)\cos(\omega t - \theta)$$

where: Q is the charge delivered to the device

Q_0 is the initial charge of the BC plane

t is time

$\tau = L/R$ is the time constant

ω is the frequency

- We will focus upon the exponential

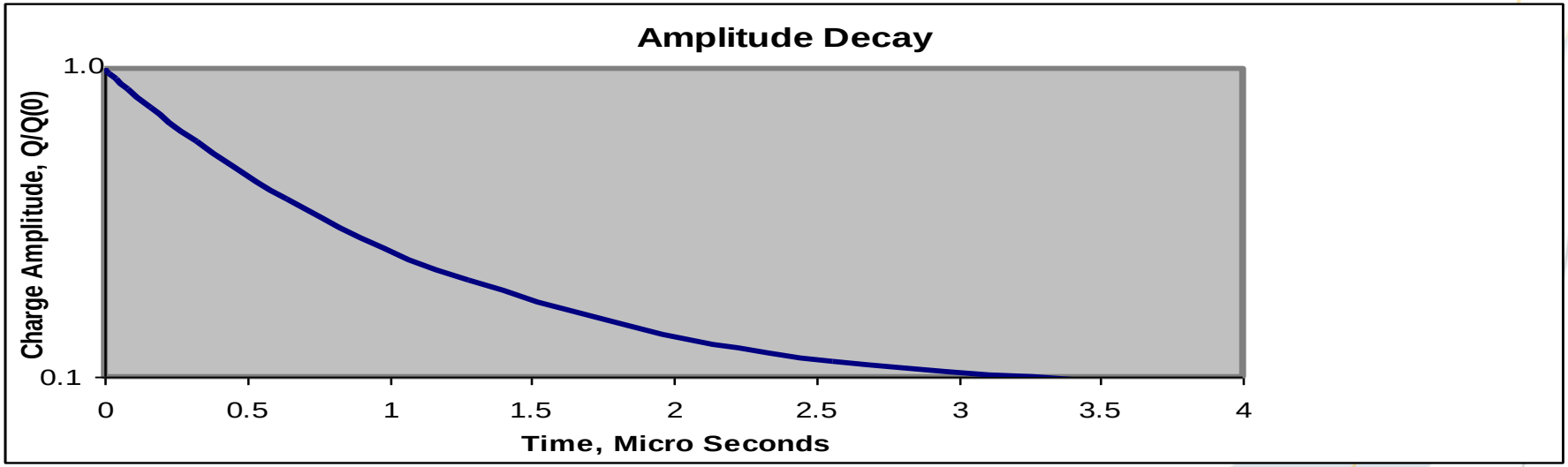
Design Analysis
Single Power Circuit

- The inductance of the circuit is for the most part produced by the via
- As shown by Johnson, *etc.* the inductance of the via is $L = 5.08h\left[\ln\left(\frac{4h}{d}+1\right)\right]$ nH
- Where h is the length of the via and d the diameter

Design Analysis
Single Power Circuit

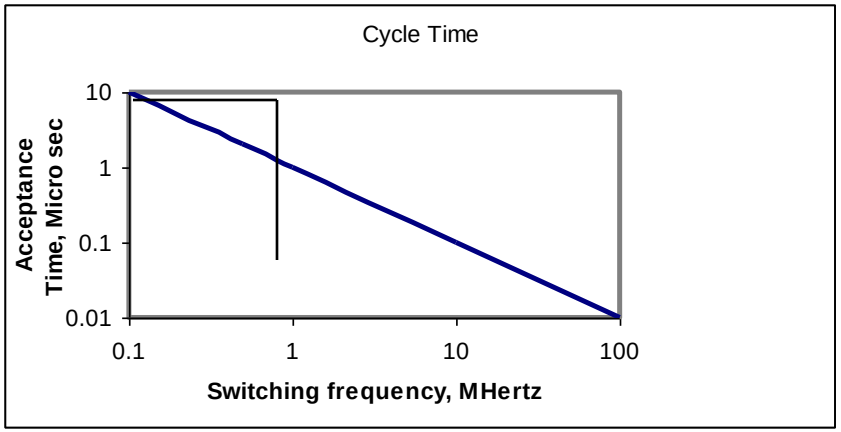
- For a 13.5 mil via in a 62 mil board
- L = 1.2 nH
- The charge decay of the BC is then

- Approximately 90% of the initial charge is delivered to the device in 3 microseconds



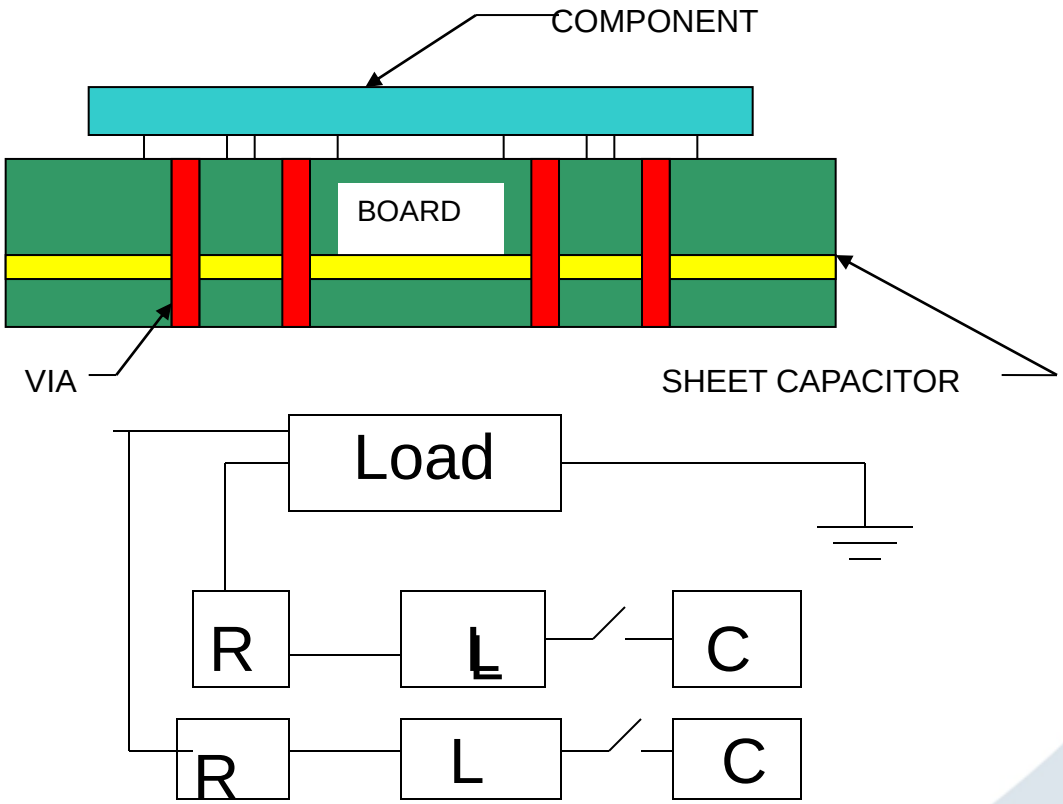
Design Analysis
Single Power Circuit

- A discharge time of 3 microseconds is compatible with a power switching frequency of ≤ 0.8 megahertz
- An alternative for higher switching frequency is:
- Multiple circuits connecting buried capacitor to device



Design Analysis
Multiple Circuits

- Increase the charge deliver per unit time with multiple connecting circuits



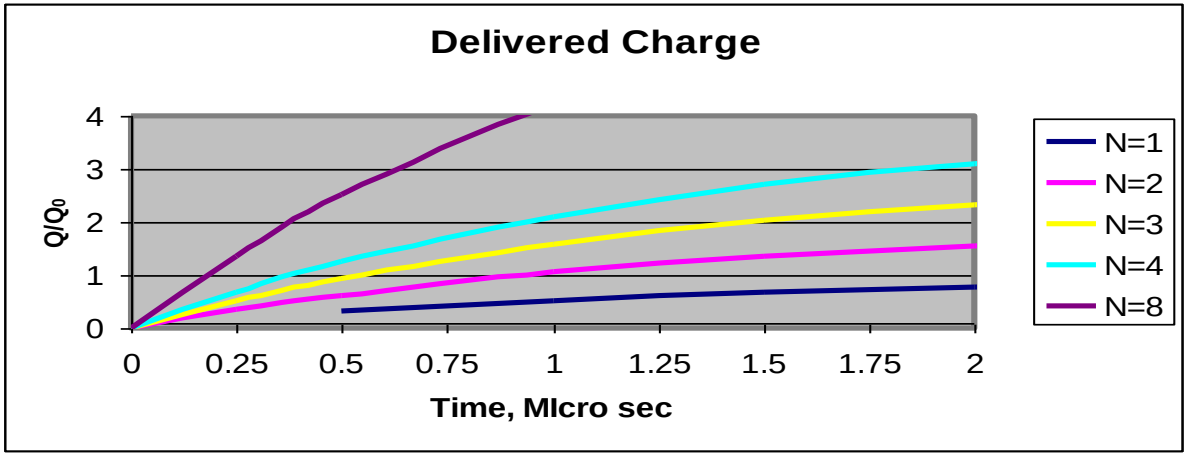
Design Analysis
Multiple Circuits

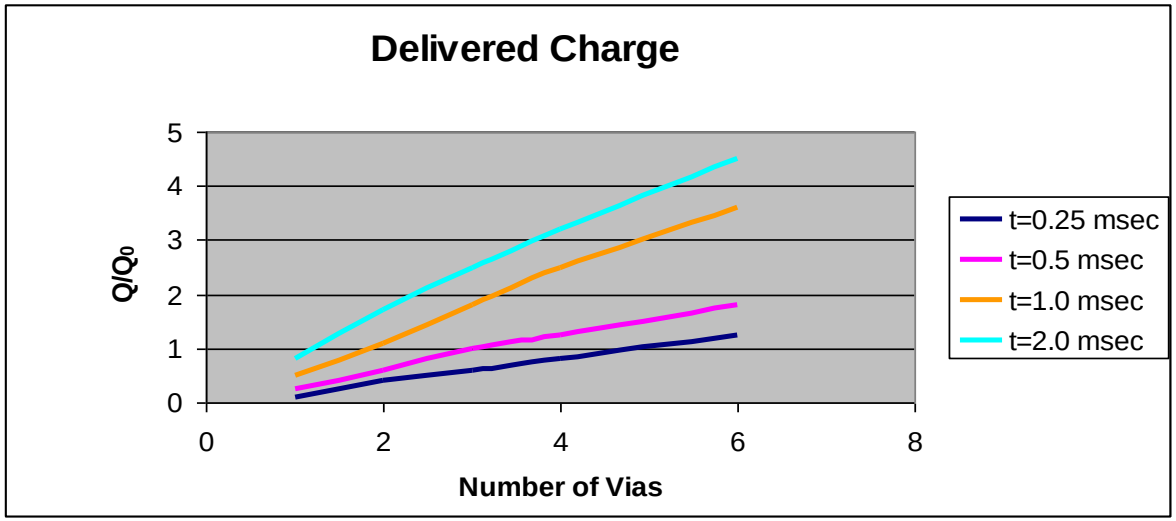
- Assume the via spacing is adequate to insure independent power sources for each connecting path
- It can be shown the delivered charge is

$$Q = NQ_O \exp(-t/\tau)\cos(\omega t - \theta)$$

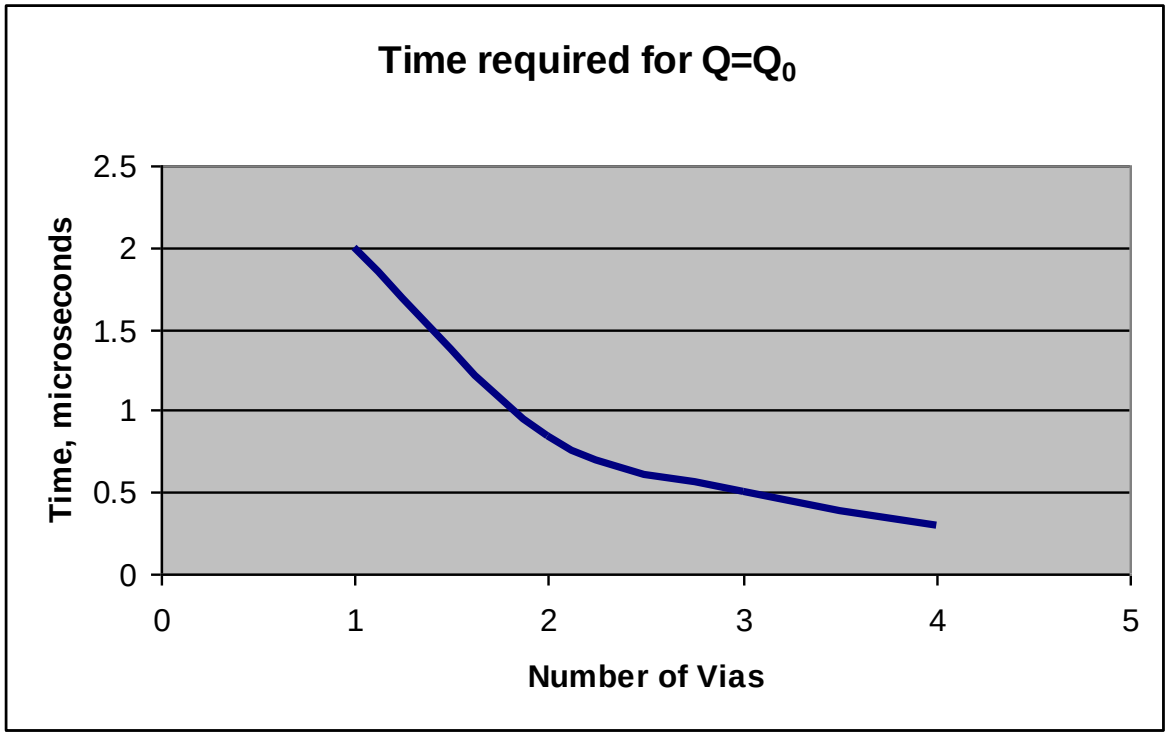
- Where N is the number of independent circuits

Design Analysis Multiple Circuits





Impact of Additional Vias on Rise Time



Observations

- Performance of buried capacitance is strongly influenced by the inductance of the connecting circuit *i.e.* the via
- Inductance of the via is proportional to its length, potential benefits arrived from
  - Blind vias
  - Partial removal of copper from connecting vias
- Transfer of charge from power plane to device is exponentially proportional to time
  - Time constant is proportional to L/R
  - A small time constant is desirable
- Power delivered at a given time is proportional to number of vias connecting device to power plane
  - Point of diminishing returns is two vias

Thank You