Comparison of the Electrochemical and Physical Properties of Nanocrystalline Copper Deposition in the Fabrication of Printed Wiring Boards

David M. Lee, John T. Folkerts, Frank L. Collins, Ann E. Dietrich, Allen Keeney
Johns Hopkins Applied Physics Laboratory Laurel, MD

Abstract
Typical electrodeposition of conventional metals produces deposits that are polycrystalline in nature, comprised of many crystal grains separated by grain boundaries. Adding grain refiners to a plating solution and employing pulse-plating techniques can reduce the grain size and produce a nanocrystalline deposit. The average grain size of the nanocrystalline copper deposit is about 100 nanometers. This is about 80 times smaller than the conventional deposit average grain size of 2 microns. Nanocrystalline copper deposits have negligible porosity and superior physical, mechanical, and electrical properties. The hardness, strength and wear resistance of the deposit are greatly enhanced. Stress corrosion cracking is virtually eliminated, while the hydrogen diffusivity and solubility are increased. This paper compares the electrochemical, mechanical, and physical properties of nanocrystalline copper deposits with conventional polycrystalline copper deposits on printed wiring boards (PWB). Test boards were evaluated after thermal shock and thermal stress tests. Copper thickness and uniformity are evaluated both by microsection and X-ray fluorescence measurement techniques.

Introduction
The electrodeposition of nanocrystalline metals has attracted considerable interest due to their improved electrochemical, mechanical and physical properties. It has been demonstrated that nanocrystalline deposits produced by pulsed electro deposition (PED) have a higher hardness, lower friction coefficient and lower electrical resistance compared to polycrystalline deposits produced by direct current (DC) plating [1].

The deposition of nanostructure deposits by PED is possible by optimizing the pulse length (time on), the time between two pulses (time off), the peak height (pulse), and the average current density [2]. Pulse electro-deposition permits electrolysis with a high current density during a short period of time [3].

The addition of organic additives such as complex formers and inhibitors are also necessary to achieve smaller grains. These additives aid in inhibiting crystallite growth resulting in a finer grained structure.

This paper compares the mechanical and physical properties of PED nanocrystalline copper deposits with DC conventional polycrystalline copper deposits on printed wiring board plated through holes.

Background
As advanced printed wiring board (PWB) designs become more complex, the thickness of the board has increased due to the greater number of layers. The plated through hole (PTH) diameters have become much smaller to accommodate the greater density of advanced designs. The increased board thickness results in the PTH's becoming less reliable due to a coefficient of thermal expansion mismatch between the PCB dielectric material and the plated copper barrel during thermal cycling stress.

Printed wiring boards with PTH's are subjected to thermal shock and thermal stress tests to determine the capability of the PTH's to withstand temperature variations.

The objective of this study is to determine if nanocrystalline copper deposits are superior to polycrystalline copper deposits by employing thermal cycle and electrical resistance tests.

High aspect ratio through hole plating tests were also performed to compare the throwing power of each plating process.

Experimental Detail
Nanocrystalline and polycrystalline copper deposits were produced by PED and DC deposition processes in a copper sulfate electrolyte with citric acid as an additive. Three different bath compositions were used listed in Table 1.

Bath A is a standard copper plating bath consisting of copper sulfate, sulfuric acid and a commercial brightener. Bath B consists of copper sulfate, sulfuric acid and citric acid. Bath C consists of copper sulfate, ammonium sulfate and citric acid. The purpose of Bath A was to produce the industry-typical polycrystalline copper deposits using DC rectification with a current density of 0.138A/in^2. Baths B and C were used to produce the nanocrystalline copper deposits using PED rectification with a current density of 0.165A/in^2 with a peak current of 10A.

Table 1-Bath Compositions

Bath	Component	g/l	Additive	g/l
A	$CuSO_4 \cdot 4H_2O$ H_2SO_4	80 225	brightener	25
B	$CuSO_4 \cdot 4H_2O$ H_2SO_4	28 225	citric acid brightener	30 25
C	$CuSO_4 \cdot 4H_2O$ $(NH4)_2SO_4$	28 50	citric acid	50

This study used test coupons designed specifically for aspect ratio plating test and thermal cycling test. The test coupons were 62 and 93 mil thick polyimide boards. The plated copper thickness in the through holes was 1.25-1.5 mils. 12” X 18” panels were drilled and electroless copper was deposited. The panels were then routed to 2”x 4” test coupons. The test coupons were panel plated then patterned with dry film photoresist and etched.

All experiments were conducted using a 5 gallon plating tank. Agitation was supplied by a recirculation filter pump with a center tank sparger. Oxygen Free High Conductivity copper anodes were and anode bags were used. A Kraft Dynatronix model DP20-5-10 power supply was used.

Analysis of the deposits included SEM micrographs, hardness tests, electrical resistance tests, thermal shock tests, and thermal stress tests.

Deposit Analysis

Scanning Electron Microscopy (SEM) was used to determine the deposit morphology. The deposits from bath A have typical polycrystalline grain structure with an average grain size of about 2 microns (Figure 1 and 2).

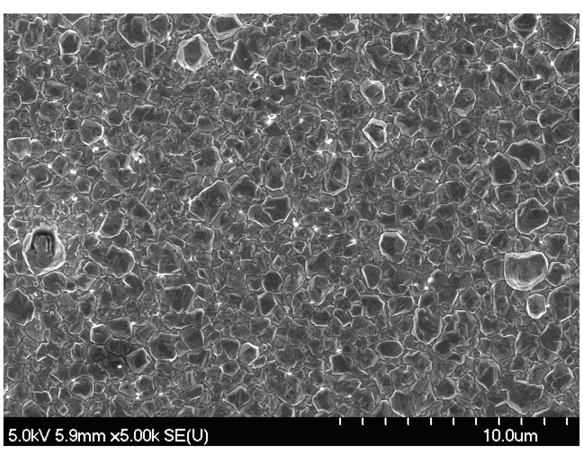


Figure 1 –Bath A

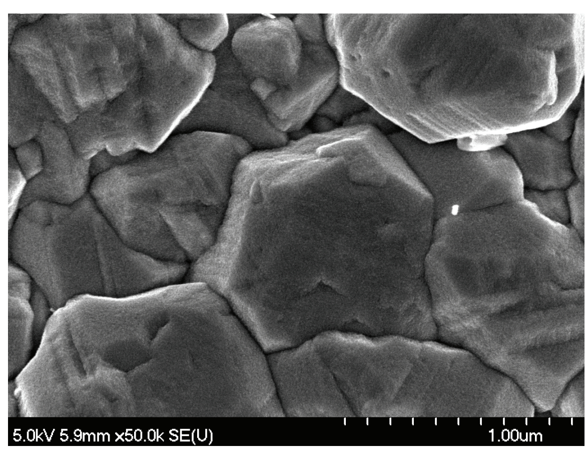


Figure 2 –Bath A

The deposits from bath B have a nanocrystalline grain structure with an average grain size of about 150 nm (Figure 3 and 4).

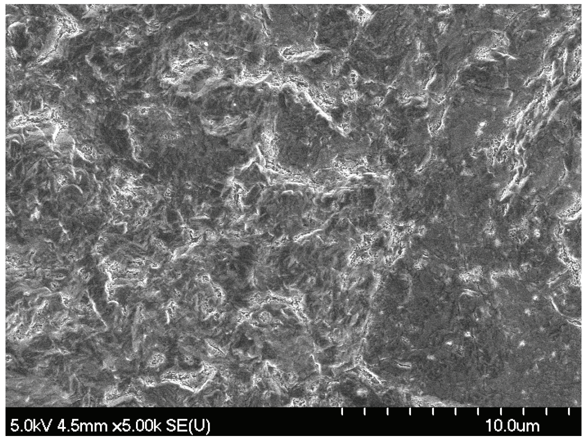


Figure 3 –Bath B

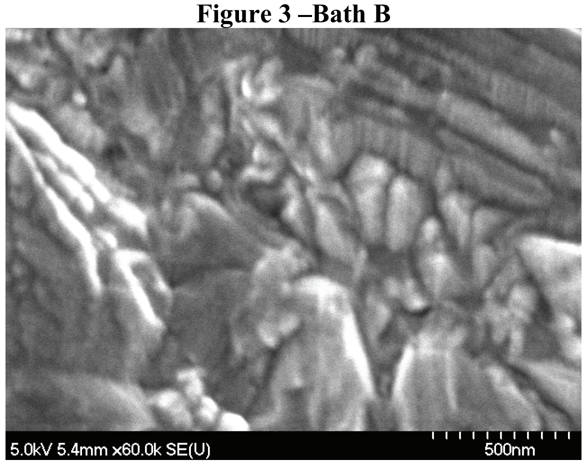


Figure 4 –Bath B

The deposits from bath C have a nanocrystalline grain structure with an average grain size of about 50 nm (Figure 5 and 6).

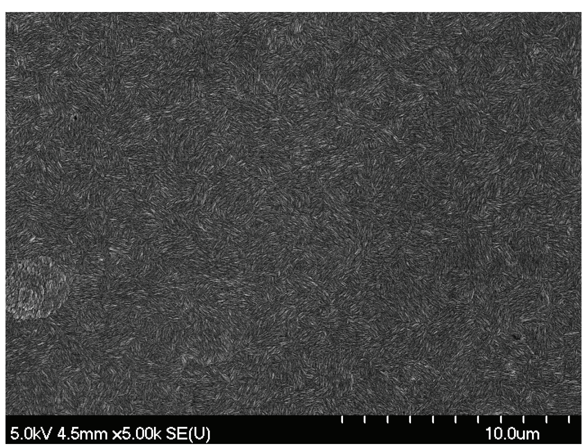


Figure 5 –Bath C

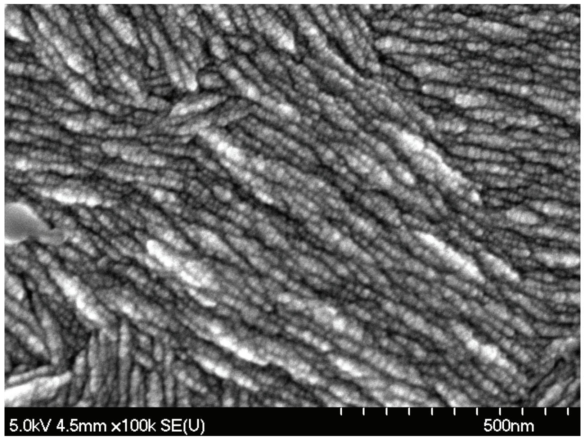


Figure 6 –Bath C

Hardness Test

Hardness tests were performed with a Clark MHT-1 microhardness tester using a Vickers diamond pyramid indenter with an applied force of 50g for 10 seconds. A low force was selected to isolate measurement to the plating layer only. The hardness measurements in Table 2 show as the grain size is reduced the deposit becomes harder.

Table 2- Hardness Test

Bath	Grain size(nm)	Force (g)	Hardness (GPa)
Bath A	2000	50	0.49
Bath B	150	50	1.21
Bath C	50	50	1.56

Thermal Shock Test

Thermal shock tests per MIL-PRF-55110G and IPC-TM-650 were performed on test coupons from each bath. The thermal cycle test board consists of 140 PTH's connected through a daisy chained pattern (Figure-7). The hole size is 28 mils with a 55 mil pad in a 62 mil thick polyimide board. The glass transition temperature of polyimide is 260°C.

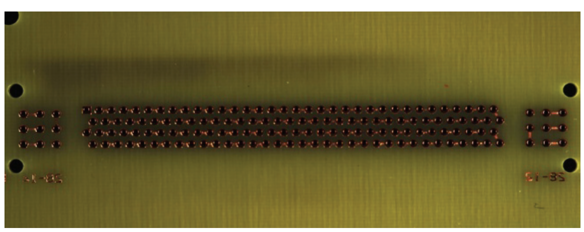


Figure 7 – Thermal Shock Test Coupon

The test specimens were subjected to 90 temperature cycles listed in table 3. The requirements of IPC-TM-650 state a high temperature limit of 170°C for polyimide dielectric material. For this test the high temperature was elevated to 177°C (the temperature limit of the test chamber) to increase the thermal expansion stress in the PTH's.

Table 3- Thermal Shock Temperature Cycle

Low Temperature	Dwell Time	High Temperature	Dwell Time
-65°C	15 (min)	+177°C	15 (min)

Interconnection resistance measurements were taken every minute during the thermal shock test. The test results listed in Table 4 indicate that after thermal cycling, test coupons from each bath passed the continuity test and there was no indication of an open circuit. Test coupons from Bath A and Bath B had a total resistances change of more than 10 percent between the first high temperature cycle and the last high temperature cycle. The requirements of IPC-TM-650 states that the total resistances change shall not be more than 10 percent. The test coupon from Bath C had a much lower initial resistance then the other baths and remained relatively stable throughout the test.

Table 4- Resistance Measurements (ohms)

Bath	Initial	First high temp.	Last high temp.	Final	Change %
A	0.901	1.213	0.882	0.610	28%
B	0.720	0.379	0.427	0.304	11.5%
C	0.165	0.244	0.242	0.161	1%

After thermal shock testing, each coupon was microsectioned and visually inspected. No plating cracks, blistering or delamination was observed in the PTH's (Figures 8-10).

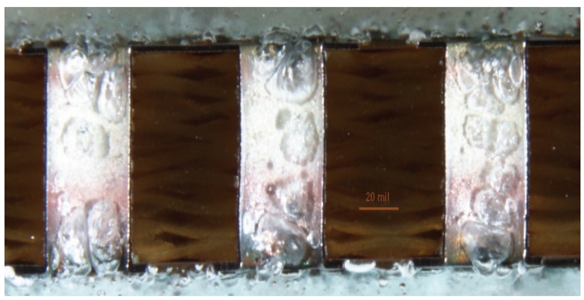


Figure 8 –Bath A

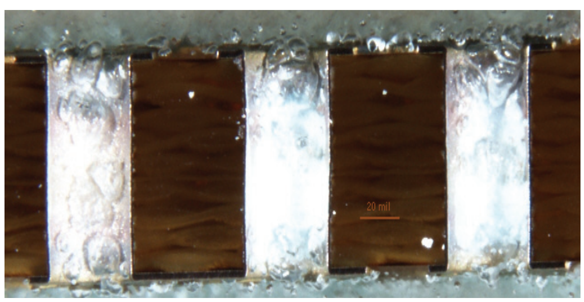


Figure 9 –Bath B

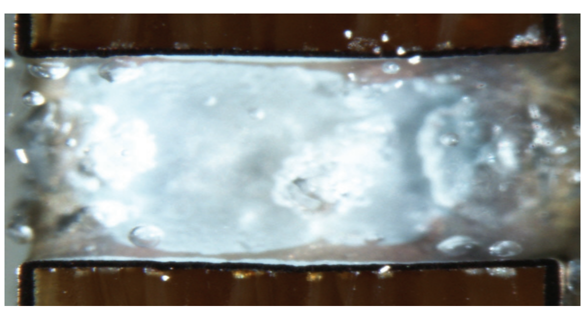


Figure 10 –Bath C

Thermal Stress Test

Test specimens from each bath were subjected to thermal stress tests consisting of an oven bake out at 121°C for a minimum of six hours and a solder dip at 260°C for 10 sec., 20 sec. and 30 sec. Results listed in Table 5 show Bath

A failed at 30 sec., Bath B failed at 20 sec. and Bath C passed all three solder dips. All failures were delamination of the plated copper from the dielectric in the thru hole (Figure-11-13).

Table 5- Thermal Stress Test

Bath	10 sec.	20 sec.	30 sec.
A	pass	pass	fail
B	pass	fail	fail
C	pass	pass	pass

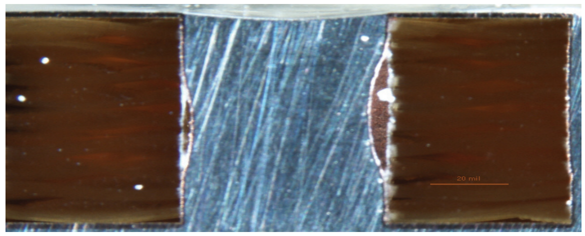


Figure 11 Bath A 30 sec.

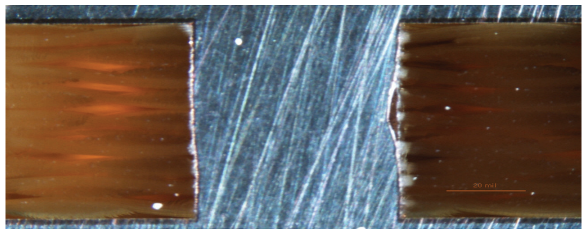


Figure 12 Bath B 20 sec.

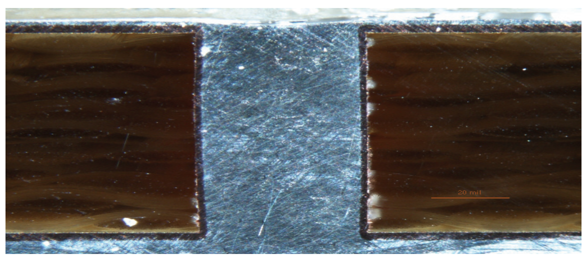


Figure 13 Bath C 30 sec.

High Aspect Ratio Through Hole Plating Test

The high aspect ratio plating test coupon consists of a 93 mil thick polyimide board with seven hole sizes of 8, 10, 15, 20, 28, 40 and 50 mils, representing aspect ratios from 1.25:1 up to 11.37:1(Figure 14).

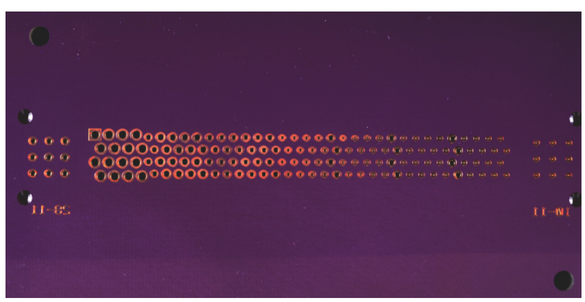


Figure 14 -Test Coupon

Test coupons were plated in each bath then microsectioned to obtain the surface to hole thickness ratio (SHTR). The SHTR is determined by dividing the plating thickness on the surface of the hole by the plating thickness in the center of the hole. The plated copper thickness in the thru holes was 1.25-1.5 mils. The results listed in Table 6 shows Bath B had the lowest SHTR. Baths A and B reliably plated hole sizes down to 8 mils (Figures 15-16). Bath C had the highest SHTR and did not have the throwing power to deposit the 1.25 mils of copper without closing the 8 and 10 mil holes (Figures 17-18).

Table 6- Surface to Hole Thickness Ratio

Aspect Ratio	Bath A	Bath B	Bath C
11.37:1	2.73	1.97	3.03/closed
9.1:1	2.63	1.88	2.98/closed
6.06:1	2.31	1.78	2.78/
4.55:1	1.94	1.68	2.3
3.25:1	1.79	1.62	2.11
2.27:1	1.65	1.58	1.92
1.82:1	1.55	1.43	1.82

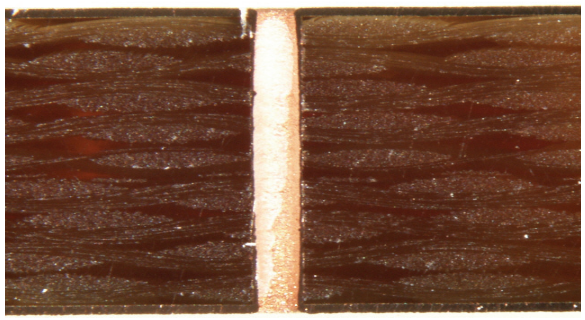


Figure 15- Bath A 8 mil hole

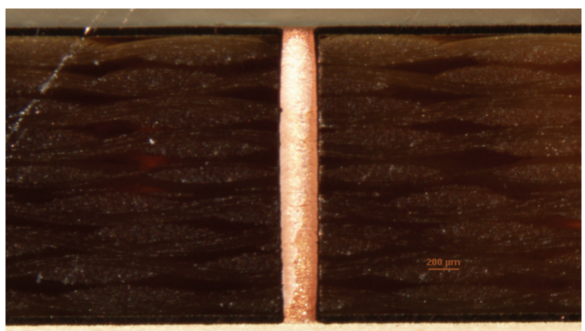


Figure 16- Bath B 8 mil hole

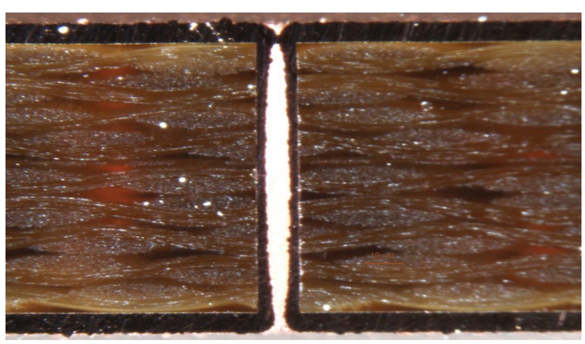


Figure 17- Bath C 8 mil

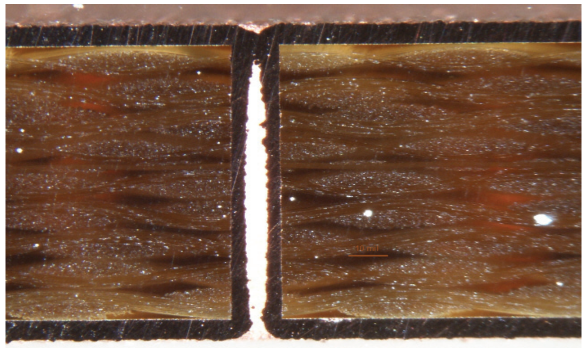


Figure 18- Bath C 10 mil hole

Conclusion

It was demonstrated that the nanocrystalline deposits produced using PED with grain sizes smaller than 100nm have a lower electrical resistance and a higher hardness then polycrystalline copper deposits produced by DC plating. The nanocrystalline deposits passed the elevated temperature of the thermal shock test and the increased dwell time of the thermal stress test.

A nanocrystalline plating process with a brightener additive exhibited a higher throwing power when plating high aspect ratio holes.

It can be concluded that nanocrystalline plating processes can be employed in the fabrication of printed wiring boards and these processes demonstrate superior mechanical and physical properties then conventional polycrystalline plating processes.

Acknowledgements

The authors would like to thank Richard J Saunders for microsectioning and analysis of test specimens and Ryan Deacon for Scanning Electron Microscopy.

References

1. Song Tao1 and D Y Li Tribological, mechanical and electrochemical properties of nanocrystalline copper deposits produced by pulse electro-deposition (2006) Nanotechnology 17 (2006) 65–78 Institute Of Physics Publishing

2. H. Natter and R. Hempelmann**.** Nanocrystalline Copper by Pulsed Electrodeposition: The Effects of Organic Additives, Bath Temperature, and pH Phys. Chem., 1996, 100 (50), pp 19525–19532 DOI: 10.1021/jp9617837 Publication Date (Web): December 12, 1996 Copyright © 1996 American Chemical Society

3. Mohsen Saremi, Maryam Abouie, R. Vaghar Electrochemical and Physical Properties of Nanocrystalline Copper Deposits Produced By Pulse Electrodeposition (2008) International Journal of Modern Physics B Vol. 22, Nos. 18 & 19 3005-3012

Comparison of The Electrochemical and Physical Properties of Nanocrystalline Copper Deposition in the Fabrication of Printed Wiring Boards

David M. Lee, John T. Folkerts, Frank L. Collins, Ann E. Dietrich, Allen Keeney

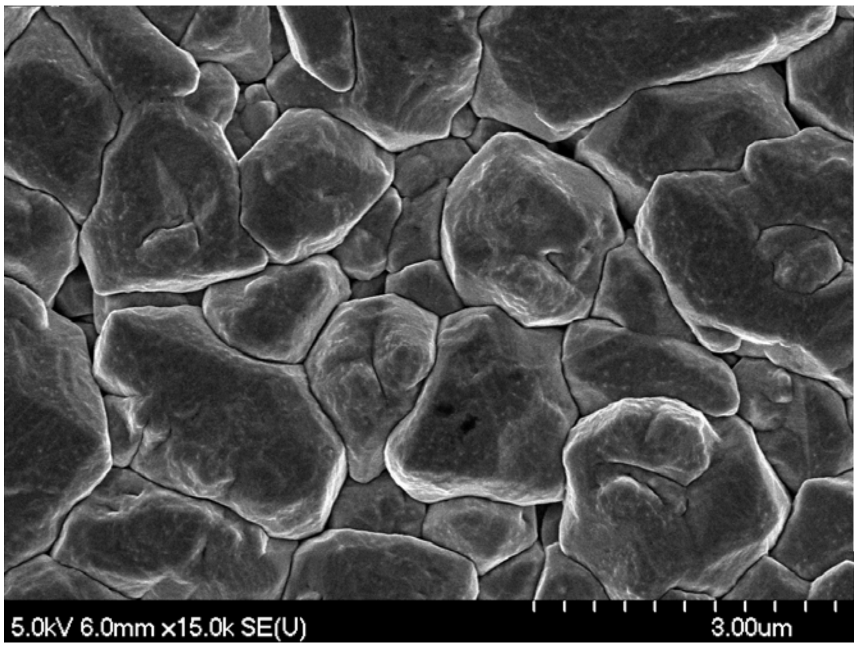
Johns Hopkins Applied Physics Laboratory
Laurel, MD

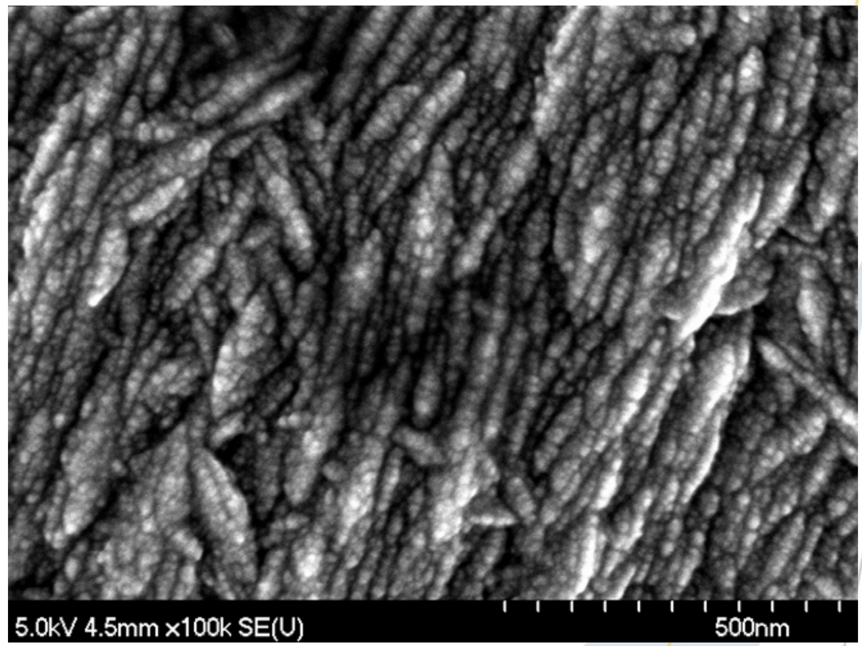
Nanocrystalline Metals

Typical direct current (DC) electrodeposition of conventional metals produce deposits that are polycrystalline in nature.

Polycrystalline deposits have an average grain size of 2 microns

Nanocrystalline deposits produced by pulsed electrodeposition (PED) have an average grain size of 100nm





Mechanical and Physical and Properties of Nanocrystalline Metals

- Nanocrystalline deposits produced by (PED), Compared to polycrystalline deposits produced by direct current (DC) plating have demonstrated…
- Higher hardness
- Lower friction coefficient
- Lower electrical resistance
- Less porosity

Nanocrystalline Deposition

- The deposition of nanostructure deposits by PED is possible by optimizing pulse parameters
- Pulse length (time on)
- Time between two pulses (time off)
- Peak height (pulse)
- Average current density

Organic Additives

- The addition of organic additives such as complex formers and inhibitors are also necessary to archive smaller grains.
- These additives aid in inhibiting crystallite growth resulting in a finer grained structure.

Plated Through Hole Reliability

- As advanced printed wiring board (PWB) designs become more complex, the thickness of the boards has increased

- The plated through hole (PTH) diameters have become much smaller to accommodate the greater density of advanced designs.

- The increased board thickness results in the PTH's becoming less reliable due to a coefficient of thermal expansion mismatch between the PCB dielectric material and the plated copper during thermal cycling stress.

Study Objectives

- This paper compared the mechanical and physical properties of PED nanocrystalline copper deposits with DC conventional polycrystalline copper deposits on printed wiring board plated through holes

- The objective is to determine if nanocrystalline copper deposits in PTH's are superior to polycrystalline copper deposits by employing thermal cycle and electrical resistance tests

- High aspect ratio through hole plating tests were performed to compare the throwing power of each plating process

Experimental Detail

- Nanocrystalline and polycrystalline copper deposits were produced by PED and DC deposition processes
- Bath A is a standard copper plating bath consisting of copper sulfate, sulfuric acid and a commercial brightener
- Bath B consists of copper sulfate, sulfuric acid, commercial brightener and citric acid
- Bath C consists of copper sulfate, ammonium sulfate and citric acid

Bath	Component	g/l	Additive	g/l
A	$CuSO_4 \cdot 4H_2O$ H_2SO_4	80 225	brightener	25
B	$CuSO_4 \cdot 4H_2O$ H_2SO_4	28 225	citric acid brightener	30 25
C	$CuSO_4 \cdot 4H_2O$ $(NH4)_2SO_4$	28 50	citric acid	50

Experimental Detail

- All experiments were conducted in a 5 gallon tank.
- Agitation was supplied by a recirculation filter pump with a center tank sparger.
- Copper anodes were OFHC and anode bags were used.
- Kraft Dynatronix model DP20-5-10 power supply was used.

Test Coupons

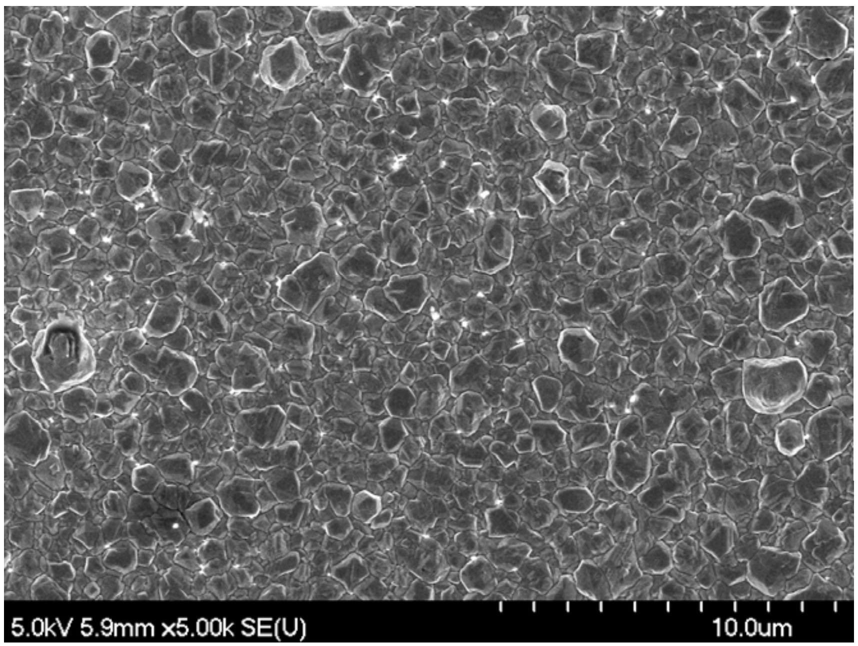
- This study used test coupons designed for thermal cycling test and high aspect ratio plating test
- Test coupons were 62 and 91 mil thick polyimide boards
- The plated copper thickness in the through holes was 1.25-1.5 mils
- The boards were drilled, electroless copper plated as a 12”x18” panel
- The panels were then routed to 2”x 4” test coupons
- The test coupons were panel plated then patterned with dry film photoresist and etched

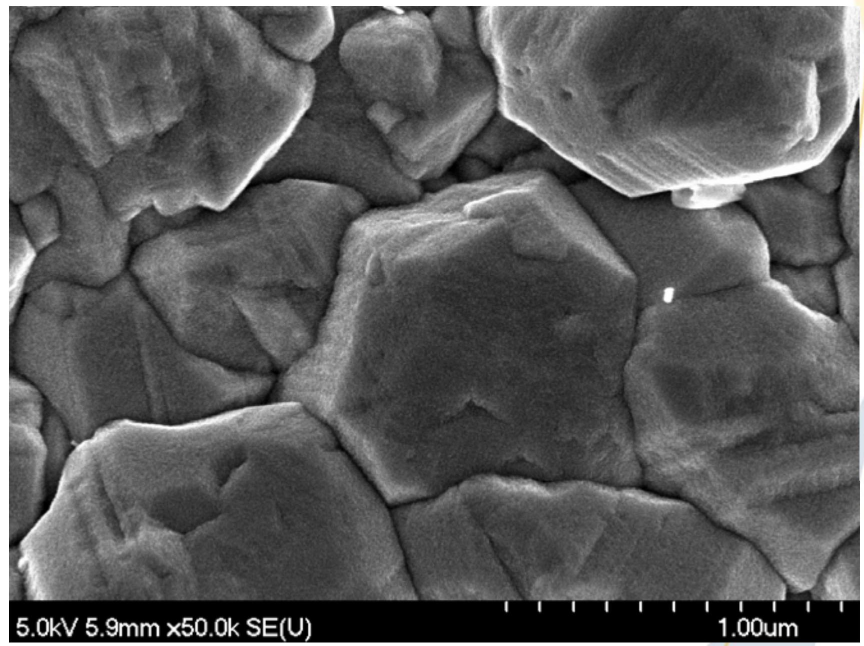
Deposit Analysis

- SEM micrographs
- Hardness tests
- Electrical resistance test
- Thermal shock tests
- Thermal stress tests
- Microsection

Polycrystalline Copper Deposits

Bath A produced polycrystalline copper deposits using DC rectification with a current density of 0.138A/in^2. Average grain size is 2 microns

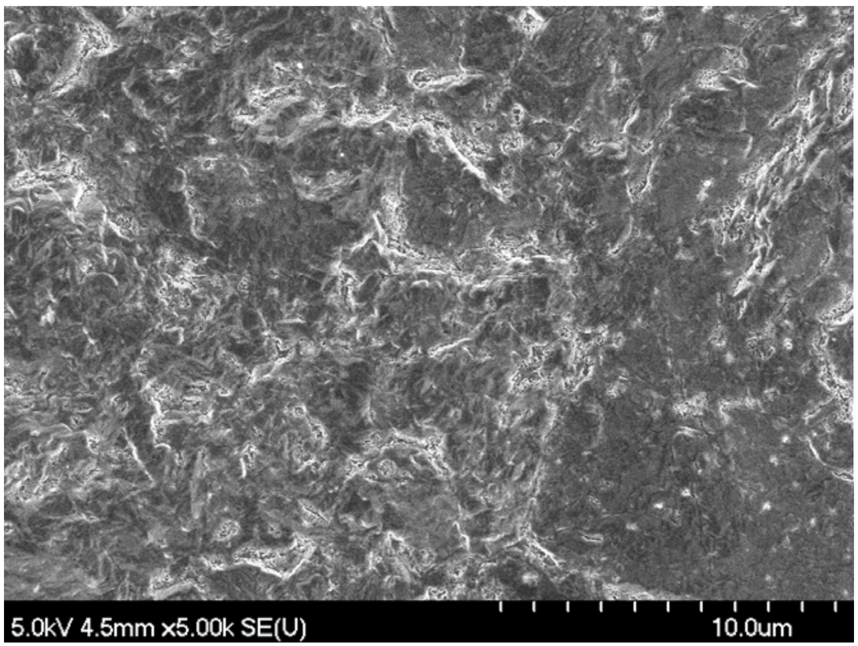




Nanocrystalline Copper Deposits

Bath B produced nanocrystalline copper deposits using PED rectification with a current density of 0.165A/in^2 with a peak current of 10A.

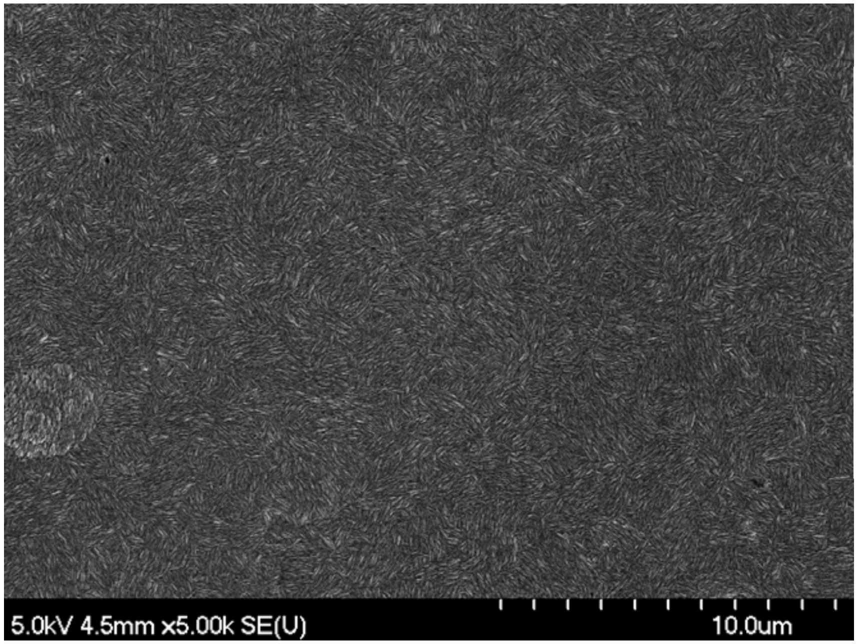
Average grain size is 150 nm

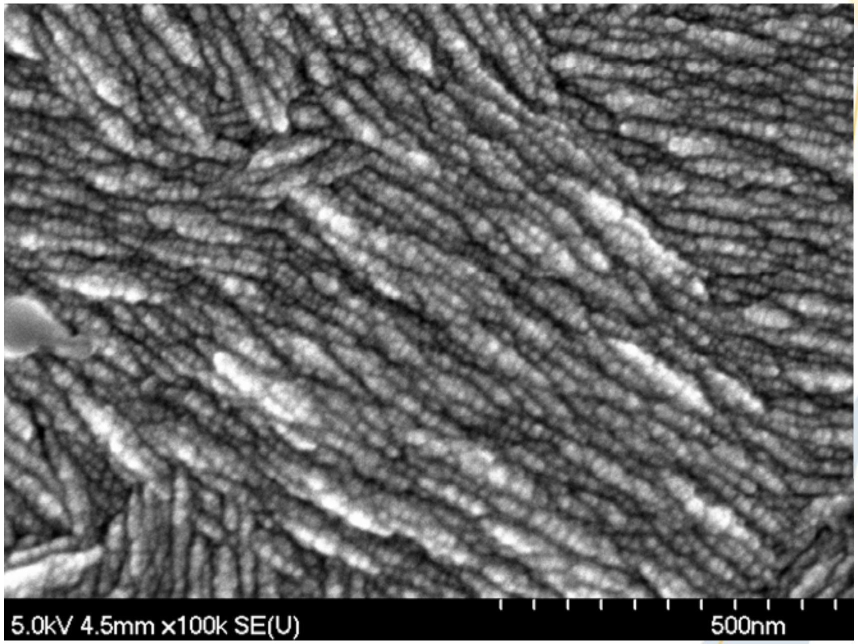


Nanocrystalline Copper Deposits

Bath C produced nanocrystalline copper deposits using PED rectification with a current density of 0.165A/in^2 with a peak current of 10A.

Average grain size is 50 nm





Hardness Test

- Hardness tests were performed with a Clark MHT-1 microhardness tester using a Vickers diamond pyramid indenter with an applied force of 50g for 10 seconds.

- A low force was selected to isolate measurement to the plating layer only.

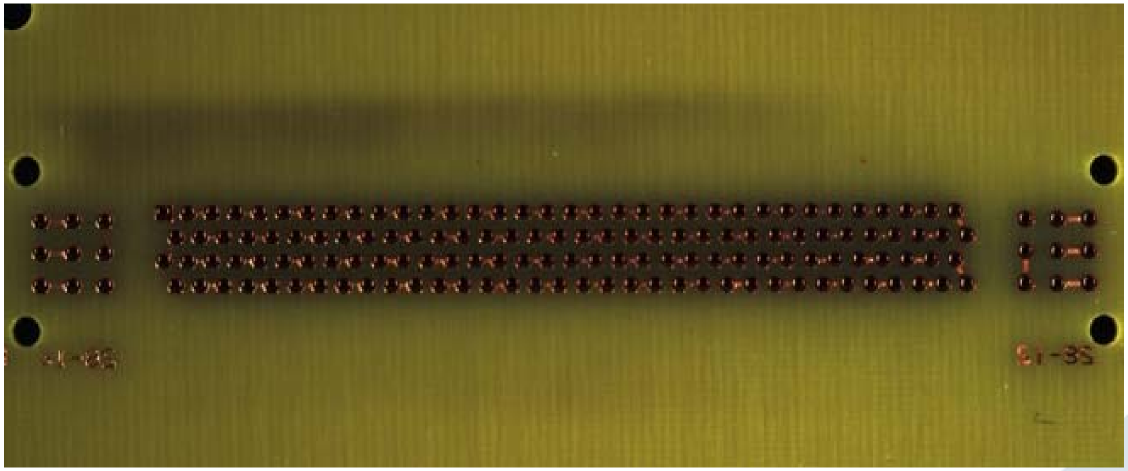
- The hardness measurements show as the grain size is reduced the deposit becomes harder

Hardness Test Results

Bath	Grain size (nm)	Force (g)	Hardness (GPa)
Bath A	2000	50	0.49
Bath B	150	50	1.21
Bath C	50	50	1.56

Thermal Shock Test

- Thermal shock tests per MIL-PRF-55110G and IPC-TM-650 were performed on test coupons from each bath
- The thermal cycle test board consists of 140 PTH's connected through a daisy chained pattern
- The hole size is 28 mils with a 55 mil pad in 62 mil thick polyimide board.
- The glass transition temperature of polyimide is 260° C



Thermal Shock Test

• The test specimens were subjected to 90 temperature cycles.

• The requirements of IPC-TM-650 state a high temperature limit of 170° C for polyimide dielectric material

• For this test the high temperature was elevated to 177° C to increase the thermal expansion stress in the PTH's

•The test results indicate that after thermal cycling, test coupons from each bath passed the continuity test and there was no indication of an open circuit

•Test coupons from Bath A and Bath B had a total resistances change of more than 10 percent between the first high temperature cycle and the last high temperature cycle

•The test coupon from Bath C had a much lower initial resistance then the other baths and remained relatively stable throughout the test

Temperature Cycle

Low Temperature	Dwell Time	High Temperature	Dwell Time
-65°C	15 (min)	+177°C	15 (min)

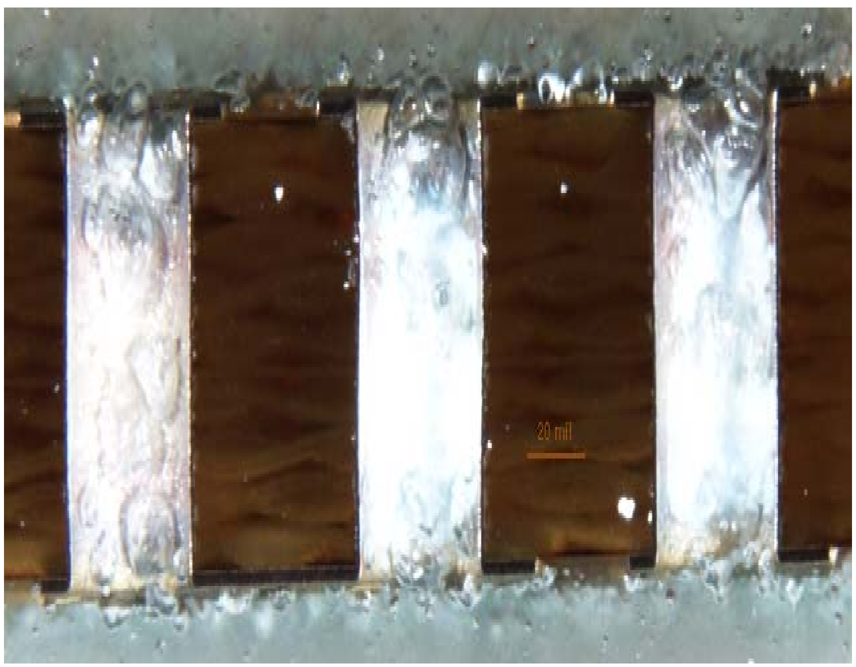
Resistance Measurements (ohms)

Bath	Initial	First high temp.	Last high temp.	Final	Change %
A	0.901	1.213	0.882	0.610	28%
B	0.720	0.379	0.427	0.304	11.5%
C	0.165	0.244	0.242	0.161	1%

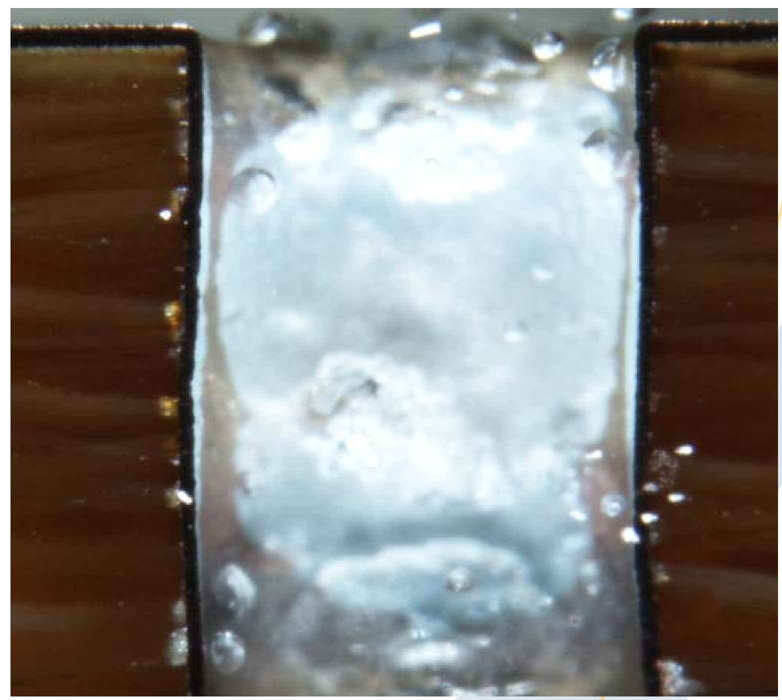
Microsection Analysis

After thermal shock testing, each coupon was microsectioned and visually inspected. No plating cracks, blistering or delamination was observed in the PTH's.

Bath B



Bath C



Thermal Stress Test

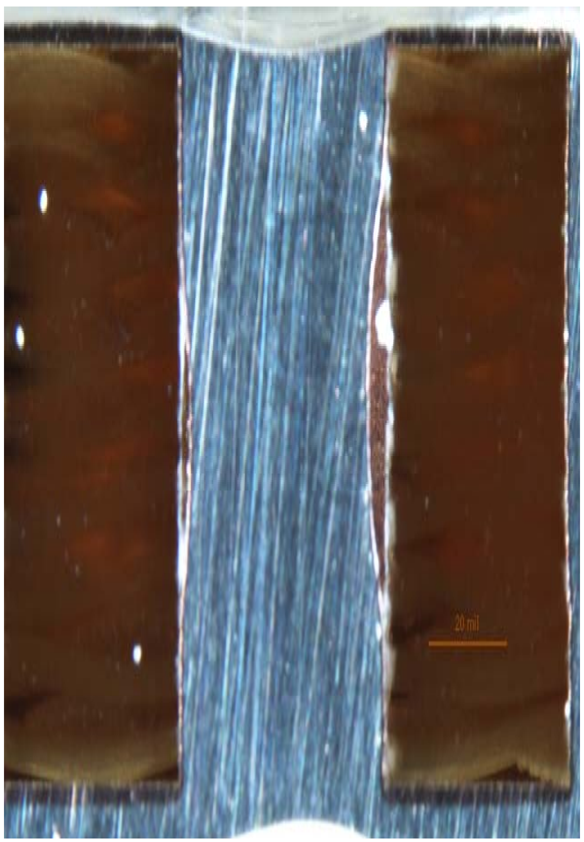
Thermal Stress Test Results

Bath	10 sec.	20 sec.	30 sec.
A	pass	pass	fail
B	pass	fail	fail
C	pass	pass	pass

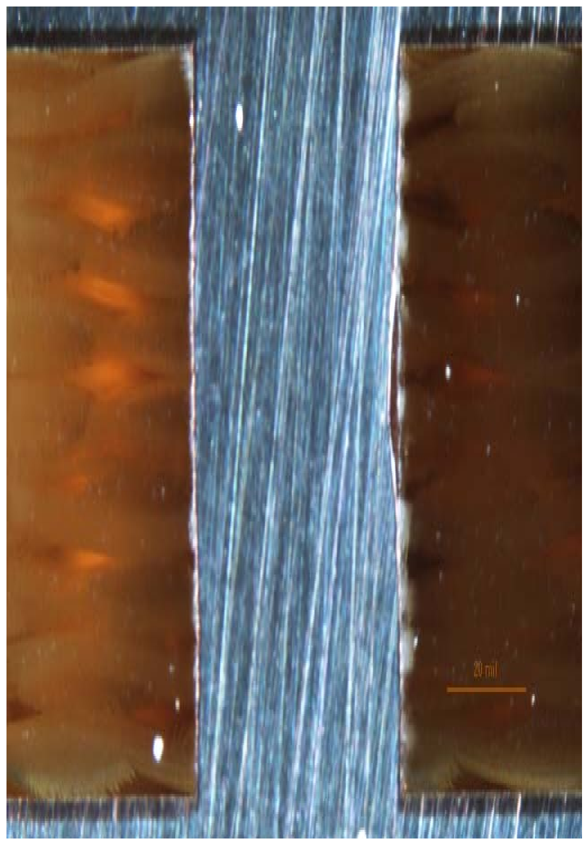
- Test specimens from each bath were subjected to thermal stress tests consisting of an oven bake out at 121° C for a minimum of six hours and a solder dip at 260° C for 10 sec., 20 sec. and 30 sec.
- Bath A failed at 30 sec.
- Bath B failed at 20 sec.
- Bath C passed all three solder dips.
- All failures were delamination of the plated copper from the dielectric in the thru hole.

Microsection Analysis of Thermal Shock Coupons

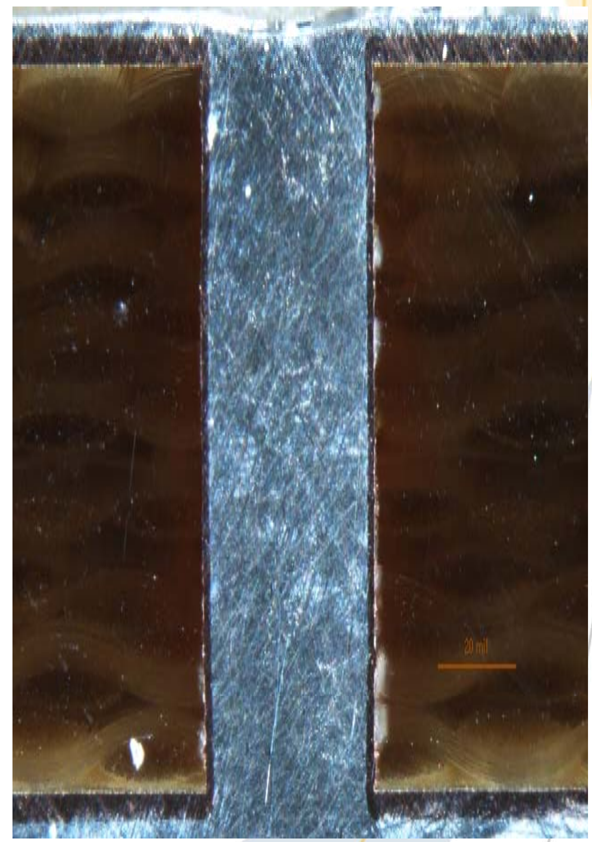
Bath A failed at 30 sec



Bath B failed at 20 sec



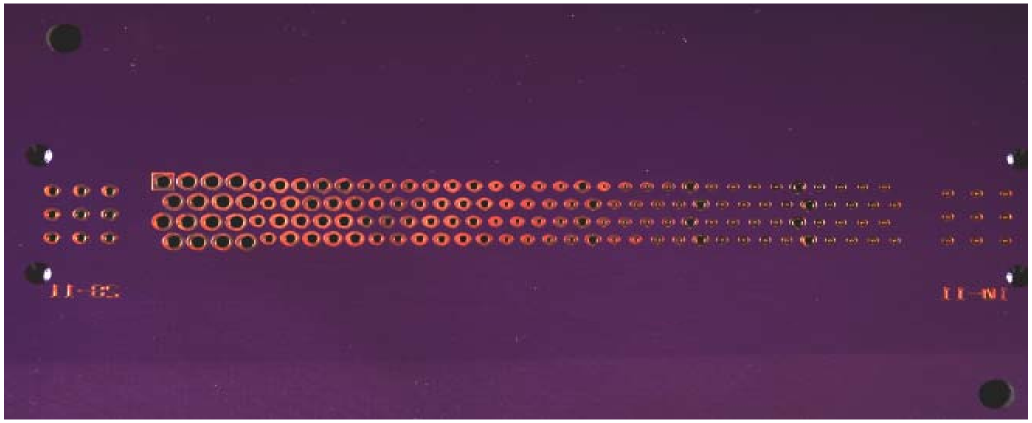
Bath C passed all three solder dips



High Aspect Ratio Through Hole Plating Test

- 91 mil thick polyimide board
- Seven hole sizes of 8, 10, 15, 20, 28, 40 and 50 mils
- Aspect ratios from 1.25:1 up to 11.37

Test Coupon



Surface to Hole Thickness Ratio

Aspect Ratio	Bath A	Bath B	Bath C
11.37:1	2.73	1.97	3.03/closed
9.1:1	2.63	1.88	2.98/closed
6.06:1	2.31	1.78	2.78/
4.55:1	1.94	1.68	2.3
3.25:1	1.79	1.62	2.11
2.27:1	1.65	1.58	1.92
1.82:1	1.55	1.43	1.82

- SHTR is determined by dividing the plating thickness on the surface of the hole by the plating thickness in the center of the hole

- The plated copper thickness in the thru holes was 1.25-1.5 mils

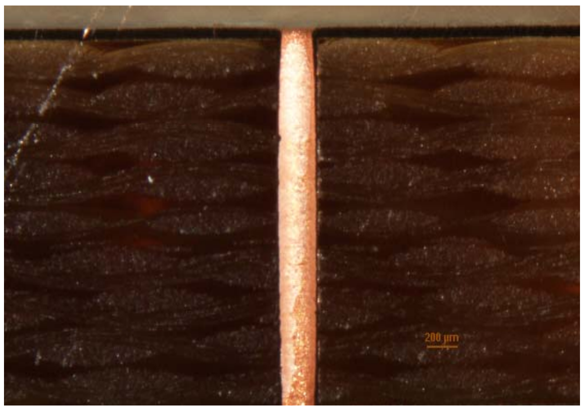
- Baths A and B reliably plated hole sizes down to 8 mils

- Bath B had the lowest SHTR

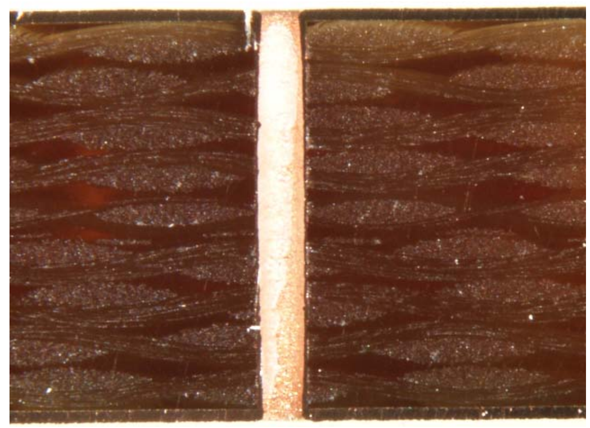
- Bath C had the highest SHTR and did not have the throwing power to deposit the 1.25 mils of copper without closing the 8 and 10 mil holes

Microsection Analysis of High Aspect Ratio Through Hole Plating Test Coupon

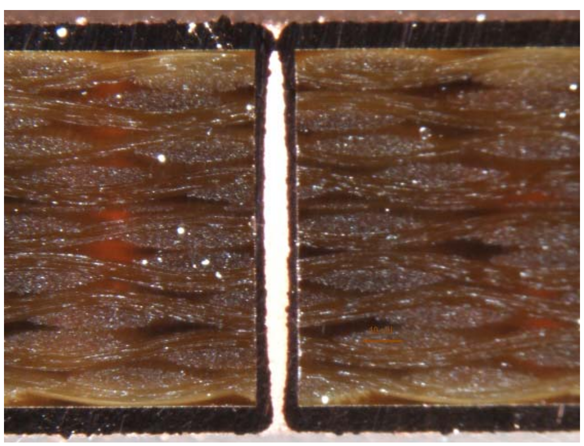
Bath B 8 mil hole



Bath B 10 mil hole



Bath C 8 mil hole



Bath C 10 mil hole

Conclusion

- It was demonstrated that the nanocrystalline deposits produced using PED with grain sizes smaller than 100nm have a lower electrical resistance and a higher hardness then polycrystalline copper deposits produced by DC plating

- The nanocrystalline deposits passed the elevated temperature of the thermal shock test and the increased dwell time of the thermal stress test

- Nanocrystalline plating process with a brightener additive exhibited a higher throwing power when plating high aspect ratio holes

- It can be concluded that nanocrystalline plating processes can be employed in the fabrication of printed wiring boards and they demonstrate superior mechanical and physical properties compared to conventional polycrystalline copper deposits