Market Forecast and Applications for 3D Packaging using Package-on-Package (PoP)

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Convergence of Product and Content Require New Manufacturing Solutions

It's an MP3 player and …

It's an e-mail terminal and

It's a camera and …

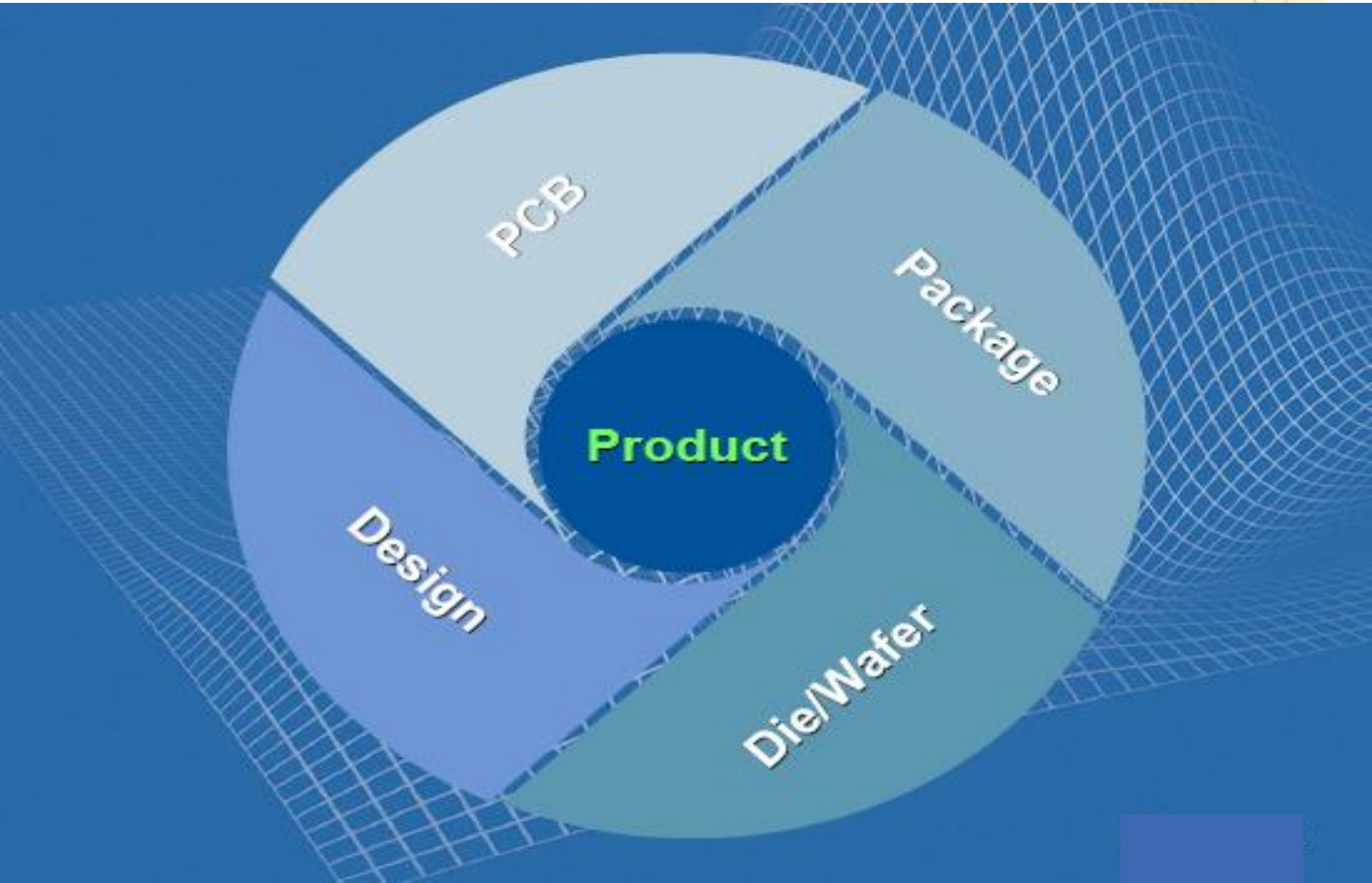
… an MP3 player, e-mail terminal, phone, camera, TV, radio, compass, game machine…

It's a TV and …

It's a game machine and …

It's a GPS compass and …

It's a radio and …

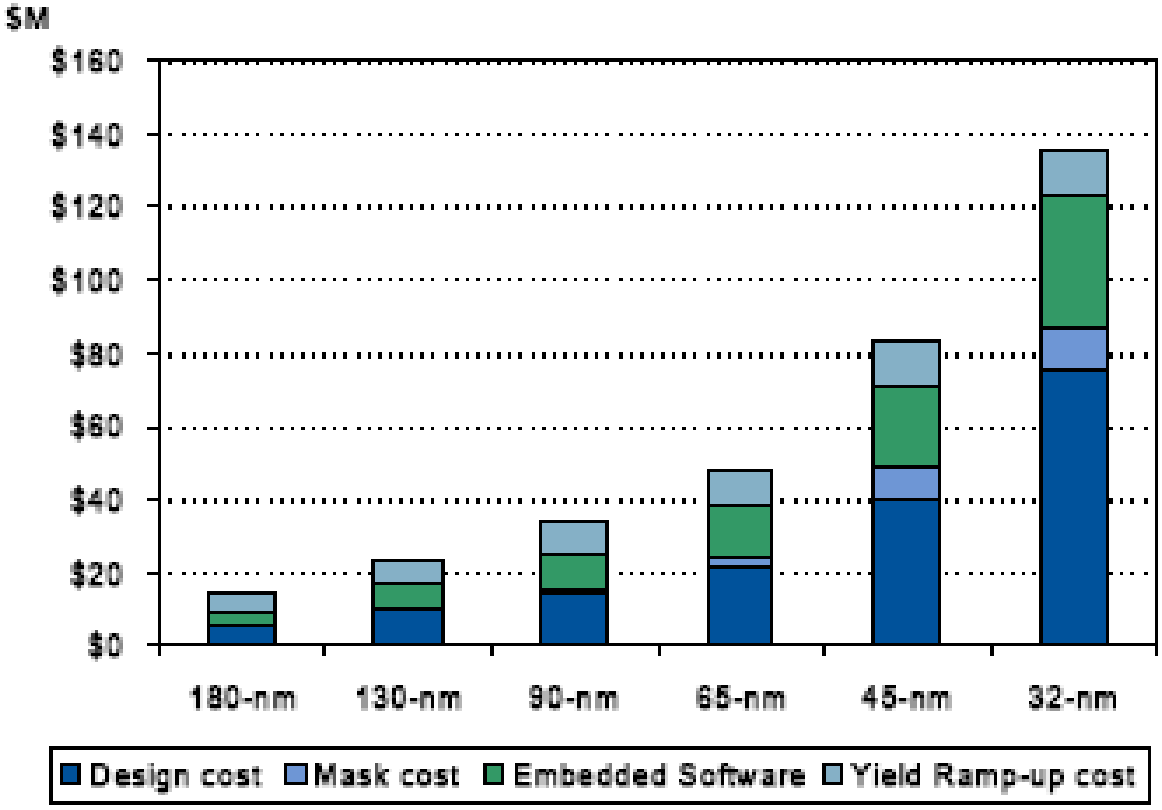

PCB
Package
Product
Design
Die/Wafer

Why 3D?

Traditional silicon integration methods take too long and are too expensive.

Design Cost/Complexity is Rising

Estimated Development Costs by Process for an advanced ASSP System-on-Chip Design



$2 Billion minimum TAM needed to justify 32nm advanced SoC design

2013 Qualifying Markets:

- Mobile Phone: $11.8B
- PC: $8.1B
- Video Games: $6.8B
- TV: $3.7B
- Set Top Box: $3.4B

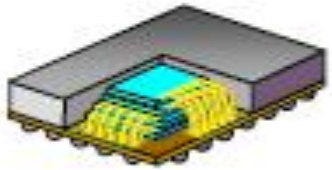
What is 3D Packaging?

- Die Stacking
- Package Stacking (POP)
- Wafer-on-Wafer
- Die-on-wafer
- Through-Silicon-Vias (TSV)

Die Stacking:

WL-CSP Technology

enables 3D, TSV, MCP & SiP



Package Stacking:

POP Technology

enables 3D, TMV, MCP & SiP

Is 3D the "Holy Grail"?

- Scaling faces significant challenges
- Going vertical provides better performance
- It's smaller
- It's cheaper

Is it the "cure all"?

Increased packing density

Reduced size - miniaturization

Faster time-to-market than SOC

Flexible wafer processing – Integration of various functions from different processes and materials

"Building-block" modular approach to design and production

It depends upon your point of view

- Round 1: Yesterday the debate was printed circuit board (PCB) vs. system-in-package (SIP).
  - 3D PCB's (multi-layer): over 40 year history
- Round 2: Today the debate is system-on-chip (SOC) vs. SIP, wafer-level package (WLP), and multi-chip package (MCP).
  - 3D packages ("piggy back" DIP): 25 year history
- Round 3: Tomorrow the debate is SOC vs. and thru-silicon vias (TSV).

3D Manufacturing Solutions: Flexible Integration

	Thru-Silicon Vias 3D TSV	*System-on-Chip* 2D SoC	*System-in-Package* 3D SiP
Cost	Good	Fair	Best
Performance	Best	Good	Fair
Power	Best	Good	Fair
Functionality	Good	Fair	Best
Time-to-Market	Good	Fair	Best

3D /SiP - Total Cost of Ownership Obstacles

Application: 3 die integration (ASIC + Combo Memory)

Design, development cycles – high cost & long time to market

- High design / development resources and risks if requirements change

Memory component and supplier selection and procurement

- Specs, procurement and inventory costs and risks
- Memory supply Terms & Conditions: wafer supply, yield and performance guarantees, lost revenue for other saleable die on wafer

Package / assembly costs

- High design / development resources, unit, tooling and capex costs

Test

- High Eng'g resources and costs, program development, sockets, handlers, load boards and hardware capex
- Yield optimization requires KGD at wafer level, but OEM DPPM requirements require final test of SiP including memory test

Finished goods

- Specs, backend cycle time, inventory and risks

Other factors influencing 3D

- Conventional scaling is approaching an area of diminishing returns; it might even be nearing the "end of the road"
- 3D applications are typically driven by cost, size, and the ability to link die designs together
- 3D applications are growing as *product life cycle* and *time-to-market* become more critical
- Future 3D applications include TSV with higher-density vias for logic+memory, logic+analog, logic+logic, logic+passive,etc.
- Expansion of 3D will be gated by total cost, manufacturing yield, availability of design tools, standardization of interconnect systems and establishment of manufacturing infrastructure

3D For Any Product – Assorted Approaches

Product and application designers have a manufacturing interconnect "tool box" for going vertical: SIP, MCP, PoP, PiP, stacked die, WLP, and TSV.

- Wire bonded packaging is cheap, but limited in density and performance.
- Flip Chip is faster and thinner than wire bonding, but difficult for multiple chip stacking,
- TSV technology will see miniaturization first, followed by increased performance and cost later.

SmartPhone: 3D and Advanced Packages

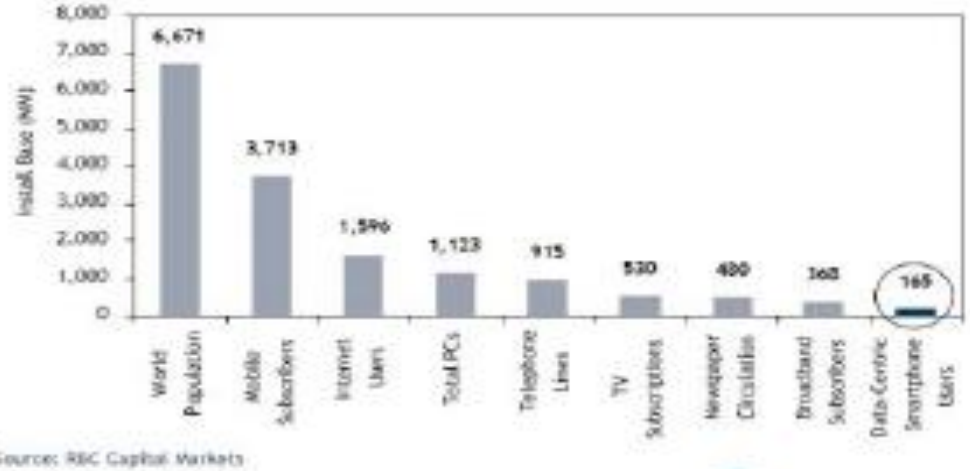
	Apple i-phone	Nokia N95	Blackberry Storm	Total
BGA's	8	12	4	*24*
DFN's	15	1	3	*19*
WLP's	10	25	14	*49*
QFN	8		4	*12*
Total	*48*	*50*	*48*	*146*

Smartphones – "one of the most attractive secular trends in technology" Credit Suisse Aug.'09

- Smartphones are the venue for convergence

- At the end of 2008 < 2.5% of the 6.671 billion people in the world had a smartphone

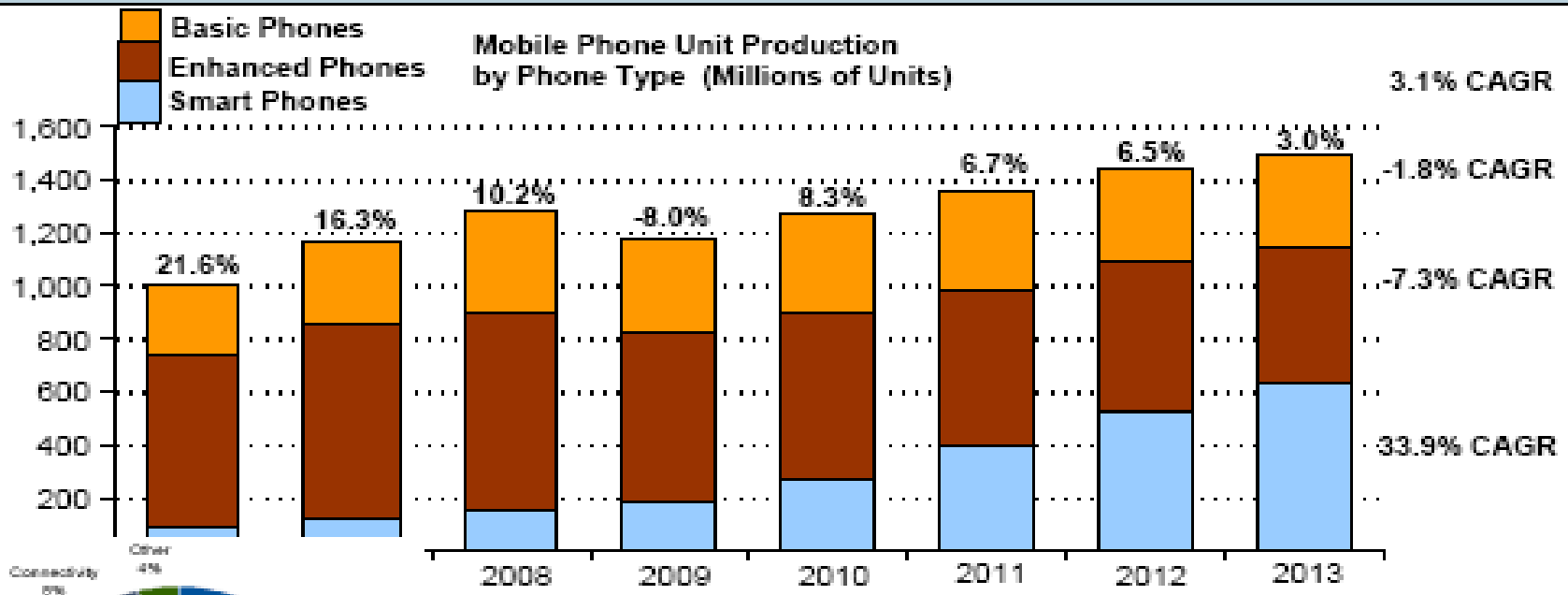
Source: RBC Capital Markets

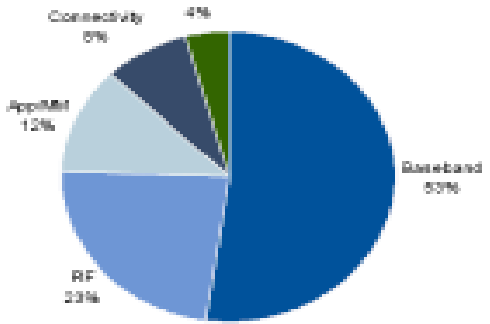


Source: RBC Capital Markets

Smartphones – The Growth Market

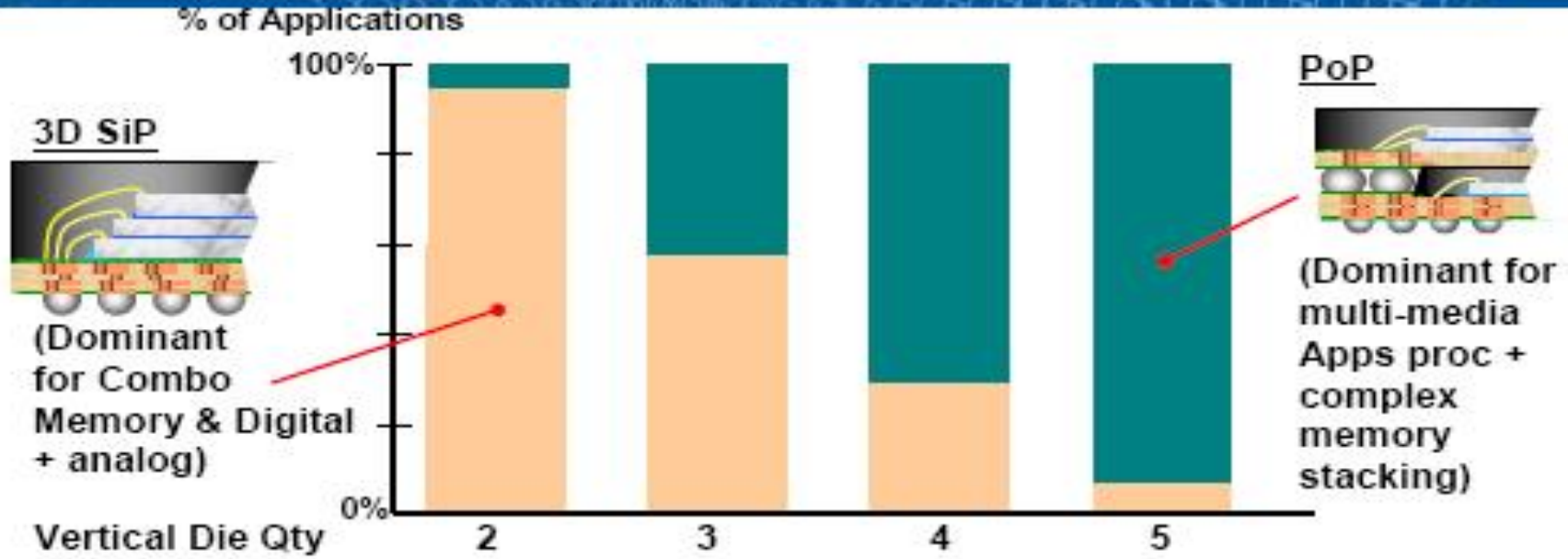
Semi TAM ($B)	43.2	46.4	44.7	38.9	41.9	47.2	49.5	49.4
Year/Year Growth	17.6%	7.4%	-3.6%	-13.0%	7.8%	12.5%	5.0%	-0.1%





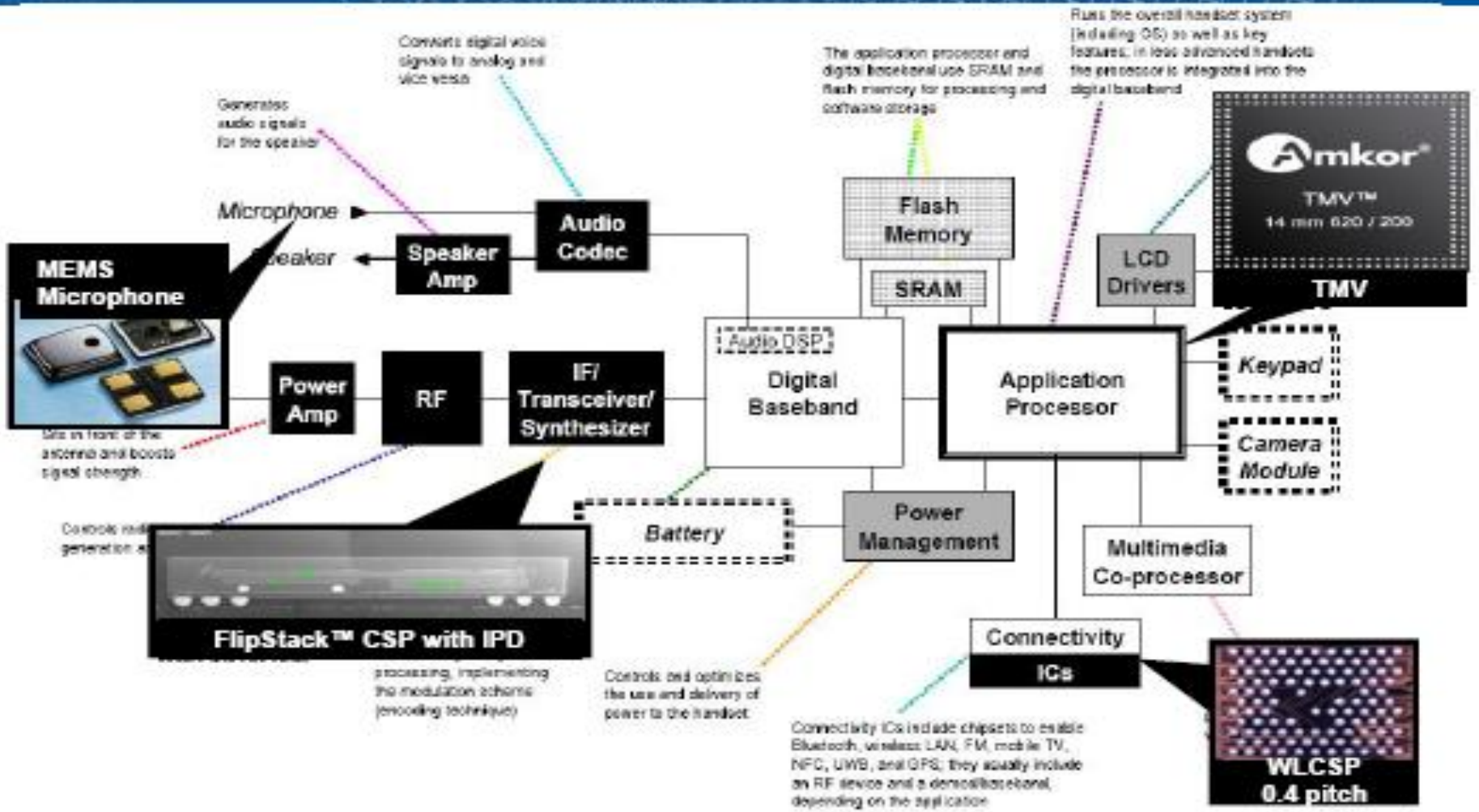
3D applications (Bband and Apps / Media uP
Represent 65% of cellphone semi content)

Die vs. Package Stack Analysis (Business / logistic factors critical to OEM & IDM)



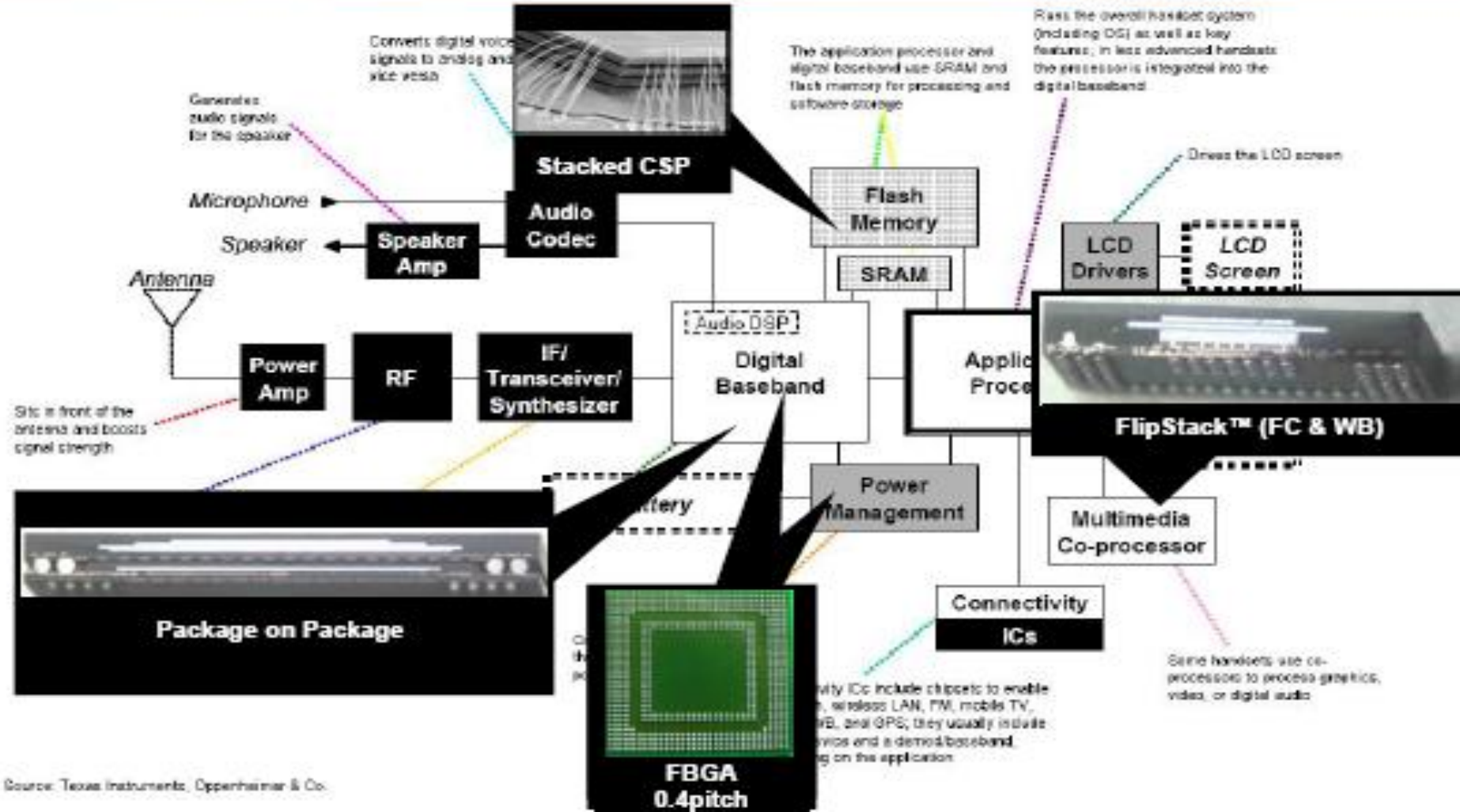
Vertical Die Qty	2	3	4	5
Cumulative Die Yield	High			Low
Die / Test Costs	Low			High
Require burn-in	No			Yes
Die/Memory Sourcing	Simple			Complex
Sourcing flexibility	No			Yes
Design flexibility	No			Yes

Smartphone - 3D and High Density Packaging



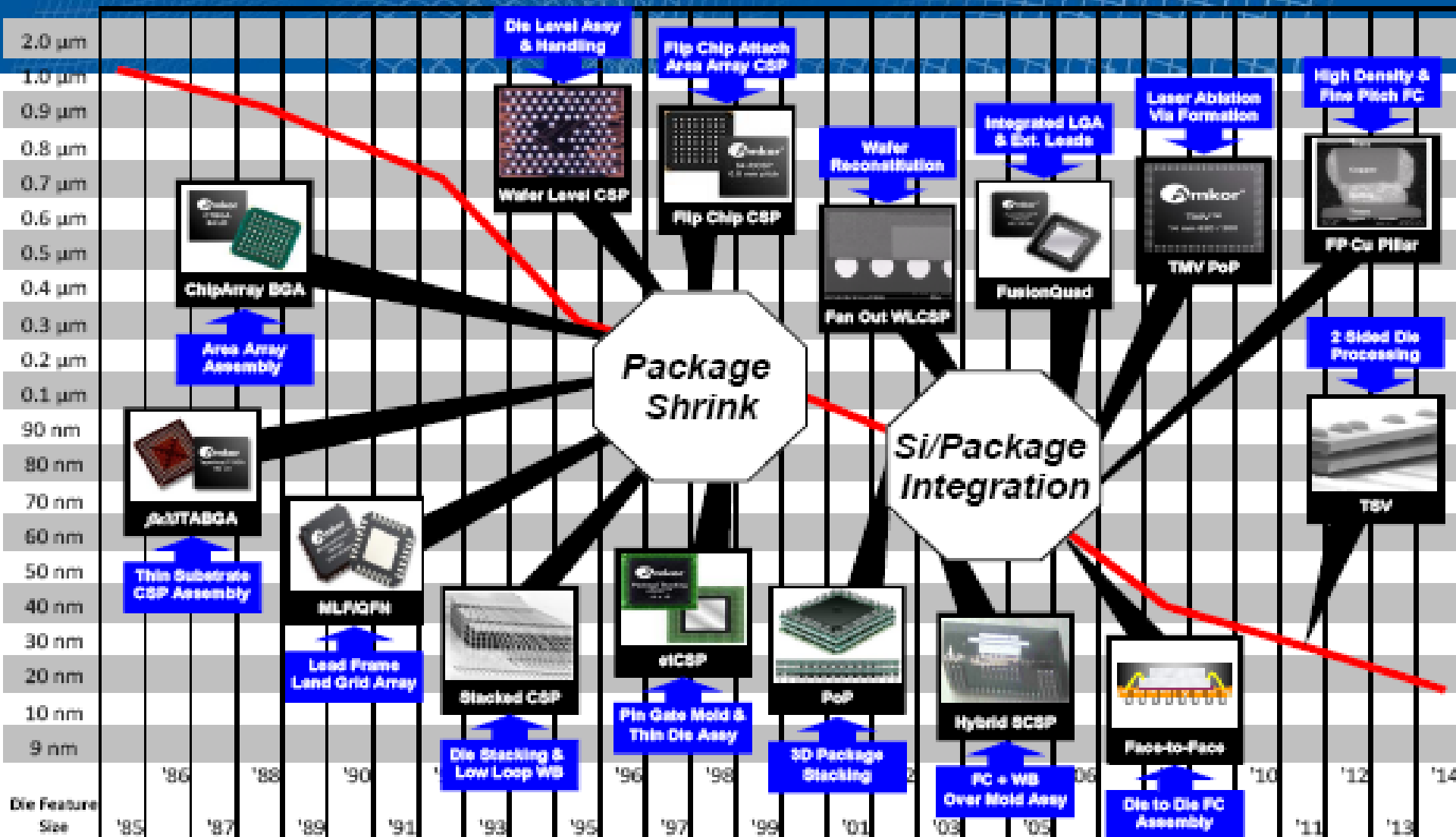
Source: Texas Instruments, Oppenheimer & Co.

Smartphone - Stacked Solutions

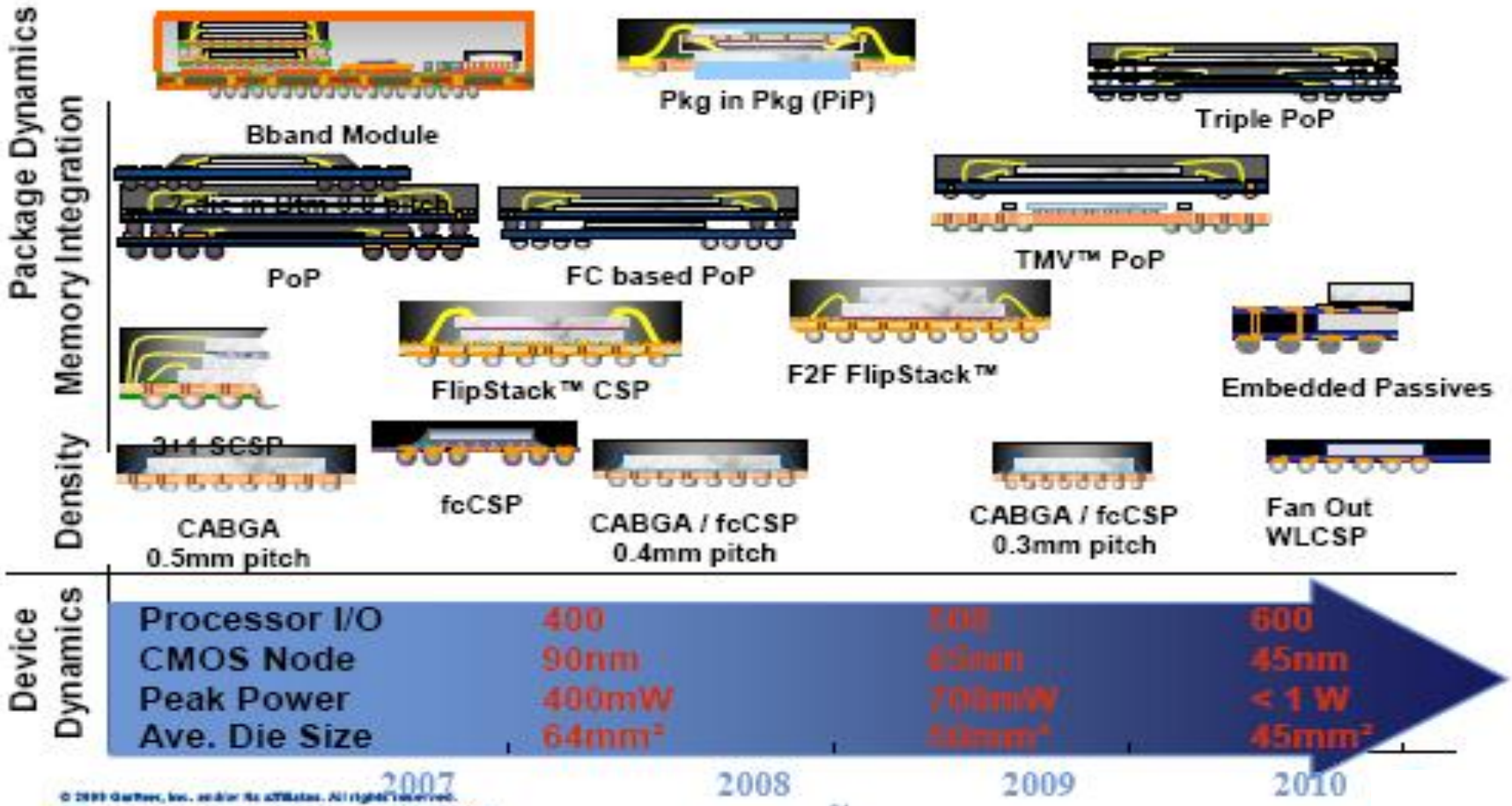


Source: Texas Instruments, Oppenheimer & Co.

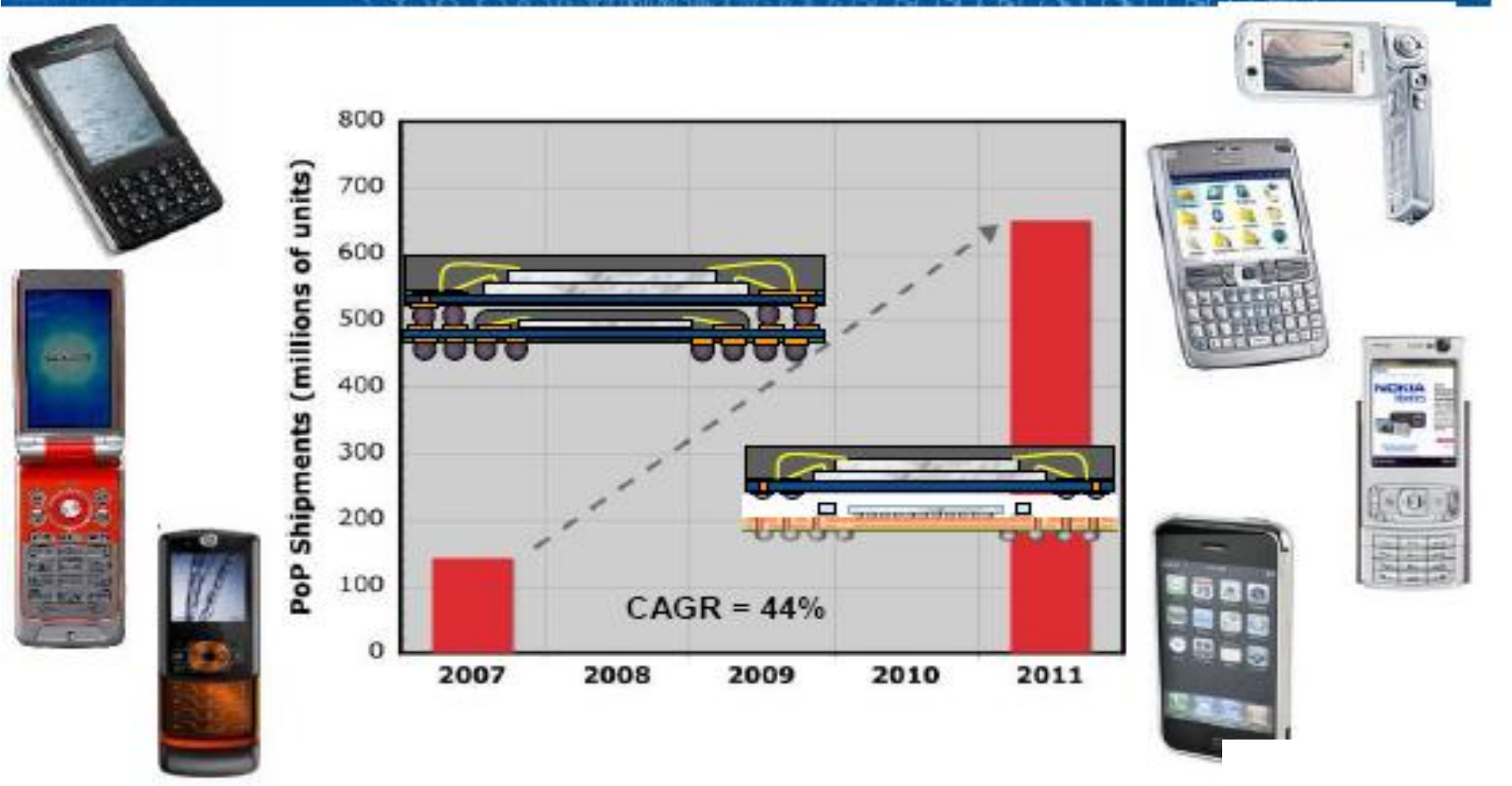
Package Evolution – µP for Mobile Products



Handheld Processor Roadmap



PoP Application Forecast



PoP – Increased Integration, Miniaturization & Performance

System Dynamics

Signal processing
- µP integration (multi core designs) - increased pin counts
- µP core speed 2 – 3X w/ each node (1GHz @ 45nm)
- Transition to FC accelerates from 65nm

Memory Interface
- Higher speed memory interface SDRAM – DDR –> LP DDR2 (533MHz)
- Wider memory bus 16 – 32
- Shared to split bus to (2 channel) architectures

Packaging Changes

- Increased pin counts with size reduction requires 0.4mm pitch top and bottom
- Warpage control with thinner / higher density PoP stacks
- Signal integrity optimization, decoupling cap integration
- Power efficiency and thermal management
- Si / pkg co-design for PoP to optimize for cost / performance

Device Dynamics

	2008	2010	2012
Processor I/O	400	500	600
CMOS Node	65nm	45nm	32nm
Peak Power	700mW	1.3W	2 W
Ave. Die Size	64mm²	50mm²	50mm²

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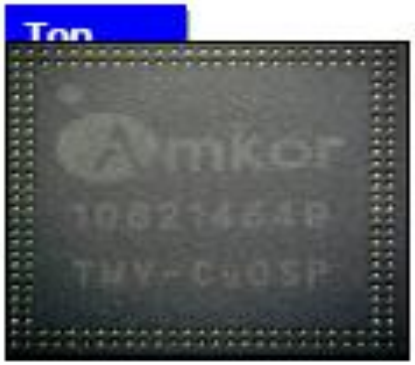
Ref: Amkor

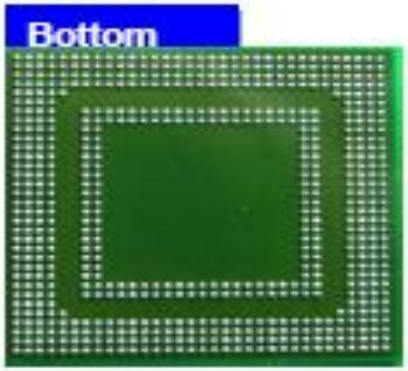
TMV™ Process – Further PoP Benefits

Enabling technology for next generation PoP requirements

1. **Improves warpage control and bottom pkg thickness**
   - Improved SMT process window expected
2. **TMV removes bottlenecks associated with memory interface**
3. **Increased die to package size ratio**
4. **Improved board level reliability**
5. **Supports Wirebond, FC, stacked die and passive integration**
6. **JEDEC mech. standards in process JC-11**

200 top Solder lands @ 0.5mm pitch



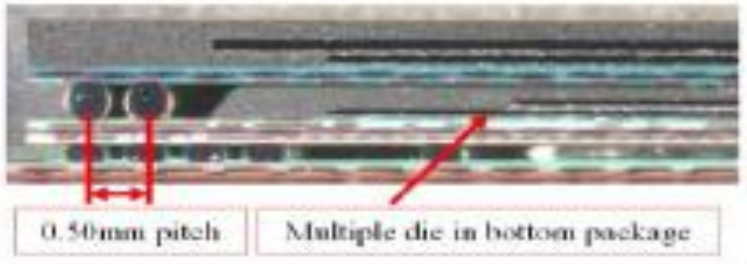


620 bottom BGAs @ 0.4mm pitch

14mm TMV test vehicle – from joint SMTAI paper w/ SEMC

TMV™ Memory Interface Scaling Benefit

- Size reduction through memory interface pitch reduction
- Baseline design: 7x7mm die, 200 I/O top package IF, 2 row perimeter



Future Directions for 3D packaging

- 3d stacking of different materials
  - GaAS with silicon for optical interconnect.
- Devices that will Drive3d
  - Systems Vs Functionality.
    - Large Memory and large logic.
    - Integration of devices from different suppliers/processors
    - Greater functionality than you can embedded
    - Performance?
      - Side by side
      - Embedded
      - Higher capacitance due to TSV
  - SSD
    - Flash, is edge connection still better
- Potentially the end of Moore's law enables 3D
- DRAM and Flash key drivers
  - Pin outs, design standards