Embedded Packaging Technologies: Imbedding Components to Meet Form, Fit, and Function

Casey H. Cooper
STI Electronics, Inc.
Madison, AL USA
ccooper@stielectronicsinc.com

Abstract
As the electronics industry moves toward smaller form and fit factors, advanced packaging technologies are needed to achieve these challenging design requirements. Current design problems are not driven by circuit design capabilities but by an inability to reliably package these circuits within the space constraints. Innovative packaging techniques are required in order to meet the increasing size, weight, power, and reliability requirements of this industry without sacrificing electrical, mechanical, or thermal performance.

Emerging technologies such as those imbedding components within organic substrates have proven capable of meeting and exceeding these design objectives. Imbedded Component/Die Technology (IC/DT®) addresses these design challenges through imbedding both actives and passives into cavities within a multi-layer printed circuit board (PCB) to decrease the surface area required to implement the circuit design and increase the robustness of the overall assembly. A passive thermal management approach is implemented with an integrated thermal core imbedded within the multi-layer PCB to which high power components are mounted directly.

This paper discusses the design methodology, packaging processes, and technology demonstrations of prototypes packaged using this technology. The various prototypes designed and manufactured using this technology will be presented.

KEYWORDS: Embedded Packaging Technology, Imbedded Components, Bare Die, Miniaturization, Form Fit and Function, 3D Assembly, Cavities, Thermal Core, Wire Bonds, Reliability, Material Characteristics, Conductive Adhesives, Hi-Rel, Multi-layer PCB

Introduction
New generations of electronics packaging technologies, using sophisticated materials and designs, enable system designers to implement their functionally complex circuits in small form and fit factors. It is through the development of new packaging materials and processes that permit increasing form, fit, and function requirements to be met repeatedly and reliably. For it is in the high reliability electronics sector that military and aerospace electronics providers continue to push the technological envelope requiring the development of innovative packaging technologies that employ new materials and assembly processes with which to enable the manufacturing of these technologically advanced designs.

Current design limitations are not driven by circuit design capabilities but by an inability to reliably package these circuits within the space constraints and meet the performance requirements. As system designers continue to integrate more capabilities into a single system, packaging engineers are tasked with the responsibility to ensure reliable electrical, mechanical, and thermal performance in the end operating environment. Innovative packaging techniques are required in order to meet the increasing form, fit, and function requirements of this industry without compromising reliability and robustness.

In recent years, the trend has been to relinquish integration in the 2D realm and move into 3D integration in order to meet the shrinking form factors sought after by all sectors of the electronics industry. 3D Integration, i.e. assembly in the Z plane, remains a very attractive alternative to component placement on and within substrates with the growing part list counts, especially as functionality/component count increases and the substrate surface area (x-y plane) decreases. Packaging technologies are being employed that integrate bare die of both actives and passives into package designs such as Multichip Modules (MCMs), System-in-Package (SiP), Chip-on-Board (COB), Wafer Level Packaging (WLP), Integrated Passive Devices (IPD) and embedded passives/actives, and emerging system-level designs such as Imbedded Component/Die Technology (IC/DT®[1]), which imbeds actives (bare die) and passives in cavities within the printed circuit board (PCB)2.

While system-level die integration packaging technologies have inherent challenges, the advantages gained from the size, weight, and power reduction and performance improvements (i.e. electrical and thermal parasitics reduction) achieved far outweigh them. Over the last 8 years, STI has completed development and has demonstrated this system-level die integration packaging technology.

In a paper presented at SMTA's Pan Pacific Conference in 2004, the features and advantages of imbedding active and passive components using these processes were presented[3]. In 2006, this unique packaging technology was patented[4] and qualified in 2008 through test and demonstration on a naval missile system[5]. Since this time, imbedded packaging technologies have enabled the miniaturization of electronics hardware that current packaging technologies, such as SMT, cannot.

Imbedded Packaging Technology Design Methodology

This unique packaging approach we have developed addresses miniaturization, thermal management, performance, reliability, and system capability requirements through innovative design guidelines and materials selection in order to meet form, fit, and function requirements. Elimination of external component packaging not only reduces circuit card assembly (CCA) size, weight, and electrical and thermal parasitics, but it enables the 3D assembly of multiple components facilitating the design integration of key subsystems, i.e. multiple CCAs, into a single high-density module.

Miniaturization is achieved fundamentally due to the elimination of external component packaging. our imbedded technology utilizes unpackaged components, known as bare die, for design with the smallest form and fit factor available. Component geometries can be reduced up to 85% through the removal of external lead frames, package substrates, and overmold encapsulants. These die are then imbedded in openings/cut-outs of the PCB, commonly referred to as cavities (see Figure 1). Imbedding die in cavities in the substrate facilitates Z-integration through imbedding die on tiers, or exposed layers, within the substrate.

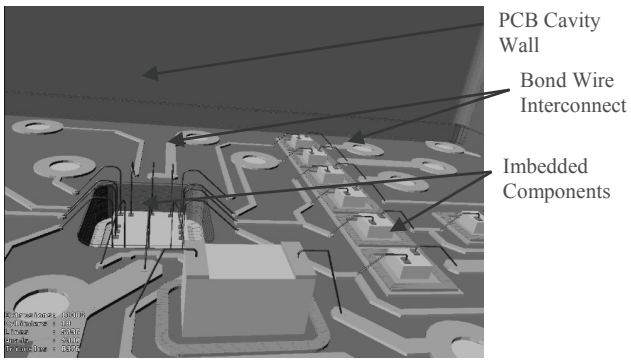


Figure 1. Active and passive components are imbedded in a cavity on a laminate substrate.

With the available real estate on the PCB provided by reduced component footprints, additional systems or capabilities can be added to an electronics assembly. System capabilities can be increased through the integration of additional features and functionality and/or redundant system within the same envelope. For example, processing architectures, such as those implemented in field programmable gate arrays (FPGAs), may be easily scaled to increase the number of processing elements (increased capability and system functionality) within the same PCB envelope due to component-level miniaturization.

Elimination of secondary packaging materials plays a significant role in the overall weight reduction achieved through imbedding unpackaged die. Interconnect materials that physically and electrically connect the integrated circuits (ICs) die to the circuitry are eliminated. In addition to the reduction in component packaging mass, there is also a reduction in the mass related to the electrical interconnect material. A significant mass savings is achieved by using wire bonds rather than solder because of the decreased volume of material per connection, as well as the lower density of typical bonding wire alloys compared to solder.

Reliability of the end product is improved not only by a reduction in interconnect material mass (translates to less applied force [F=ma] under load), but also through the increased flexibility of the electrical attachment. Through the use of wire bonding technology as the electrical interconnect process, very flexible light-weight interconnects are created. This flexibility is exploited during operation in demanding thermal and mechanical environments such as high temperature, vibration, and/or mechanical shock. In contrast to a soldered connection, which localizes the applied stress, the imbedded concept distributes the applied stress producing a more robust and rugged electronics product.

The technology also improves long-term signal reliability by eliminating unnecessary failure opportunities and utilizing reliable electrical interconnects. All first level component packaging is eliminated. This eliminates two to four possible modes of electrical failure associated with component-level packaging. Due to the removal of external packaging, electrical parasitics and thermal resistance are reduced improving overall system performance as desired in high speed, high I/O systems such as those found in missile defense systems.

Conventionally, a high power CCA would dissipate heat through convection or radiation from the component and substrate surfaces, often including package-level heat sinks or cooling fans. However, advanced handheld and miniaturized avionic applications inhibit the use of these passive and active cooling devices. Therefore, this technology provides a solution through relying on passive cooling via conduction to a single, central cooling core to remove heat from high power devices and to evenly distribute the thermal energy along the interface. Thermal resistance from junction to air is minimized through the use of thermally conductive adhesives with thin bond line thicknesses (BLT). This was demonstrated using IR thermal imaging of a prototype we developed with two imbedded power transistors and compared to a conventional through-hole transistor component (TO-32 case size), with the same amount of power applied to each. The infrared images were captured with temperature gradients/profiles as shown below. Testing of the TO-32 packaged transistor (see Figure 2) as compared to the imbedded bare die transistors mounted to the imbedded cooling core (see Figure 3) yielded an 80% reduction in localized hot spot temperature when mounted in die form directly to the cooling core. Through creative thermal management, die junction temperatures (T_J) are reduced which increases the performance and longevity of the electronic components and further increases system-level reliability.

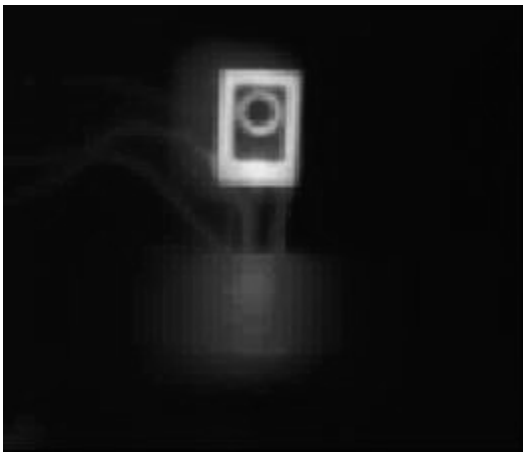


Figure 2. Through-hole transistor in TO-32 case with maximum case temperatures of 163ºC.

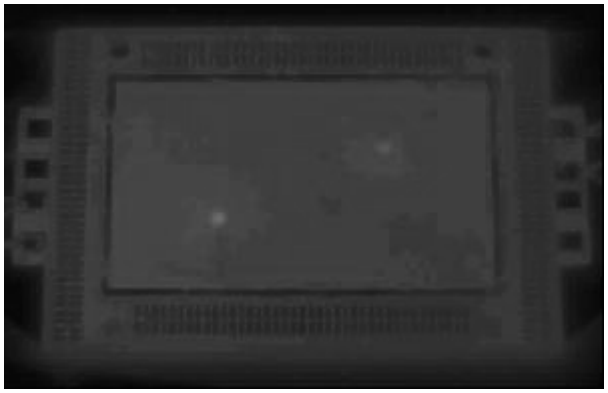


Figure 3. Two imbedded transistor die in an IC/DT® prototype with maximum junction temperatures of 32ºC.

Technology Demonstrations

We have recently completed testing of two prototype vehicles to serve as a technology demonstration of the design guidelines, materials, and manufacturing processes used to imbed passive and active devices in laminate substrates. Environmental stress testing was conducted on these prototypes to evaluate the robustness of imbedded bare die in an organic laminate substrate in conventional military and aerospace environments (harsh environments).

Test Vehicle 1

A test vehicle was designed to evaluate the effectiveness of assembly materials in harsh environments when imbedding bare die (silicon die) in organic laminate substrates. The test vehicle consisted of multiple imbedded die (Figure 4) wired to inner layer tiers for monitoring fluctuations in resistance during/after environmental testing. The imbedded test die consisted of daisy-chain components with peripheral bond pads for interconnecting to a test substrate.

Test patterns on the high temperature FR4 (HT-FR4) laminate substrate enabled in-situ resistance monitoring of the assembly during testing. A conformal coating, encapsulant, and lid were used (Figure 5) to protect the imbedded die from physical damage (handling/transportation) and the environments (ionic contamination, moisture ingression, and vibration dampening).

Test Coupon Parameters

- Substrate: 4.0 x 6.0 inch HT-FR4, laminate PCB, three tiers
- Imbedded Core: copper core, Ni/Au plating
- Die: 0.248 x 0.240 inch silicon die, daisy-chain design, peripheral wire bond pads
- Die Attach: compliant epoxy, thermally conductive, electrically insulative
- Interconnect: Al/1%Si wire
- Conformal Coating: Parylene C
- Encapsulant: silicone gel
- Lid: laminate with top/bottom copper plane layer

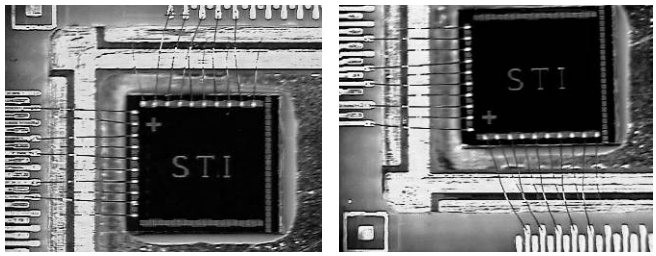


Figure 4. High-resolution images of daisy-chain die imbedded in the central cavity: upper left die (left) and lower left die (right).

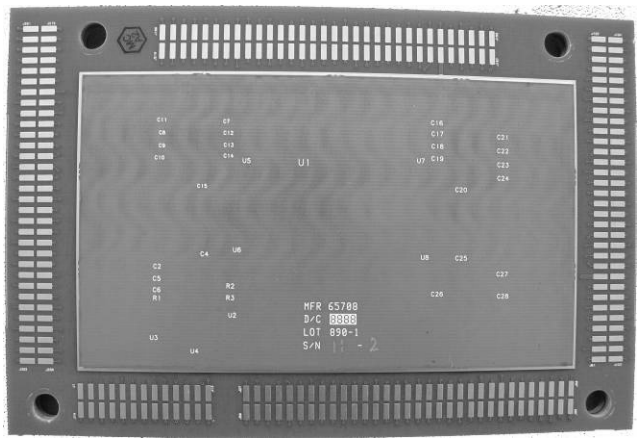


Figure 5. High-resolution image of the test coupon final assembly.

Material properties found on the technical data sheets were reviewed prior to selection of die attach, conformal coating, and encapsulant candidates to include in the test matrix. Materials were identified that minimize coefficient of thermal expansion (CTE) induced stress on the devices and interconnects and to reduce the thermal resistance between the die junctions and substrate/heat sink. Certain characteristics are desirable for all materials comprising the assembly. Materials with a glass transition temperature (Tg) outside the fielded environment range are desired in order to minimize thermomechanical stresses induced by a material's state change from glassy to rubbery. Die attaches, underfills, and encapsulants with low ionic contaminates are desired to minimize opportunities for corrosion in harsh environments. Thermal and electrical performance of the materials are equally as important in order to meet system-level performance requirements. Materials meeting the following specifications were selected to be included in the test matrix.

Thermal cycling fatigue or overstress failures are detected through alternating exposure of the assembly to extreme temperatures with short transition times between extremes. The test vehicle was placed in a thermal shock chamber to evaluate the resistance to temperature excursions of the assembly materials and process parameters used to manufacture the test vehicle. The assembly was placed on a tray that transitions from a cold chamber to a hot chamber (air-to-air) within a specified time. Test conditions were changed periodically during the thermal shock test. Test conditions included: 1000 cycles from -55°C to 85°C, 250 cycles from -55°C to 125°C, 200 cycles from -55°C to 85°C, followed by 4200 cycles from -55°C to 125°C. The test vehicle was subjected to over 175 days of thermal shock cycling.

Continuity testing was performed prior to cycling to establish a baseline resistance for each of the daisy-chains and at periodic intervals to monitor resistance fluctuations. Five daisy-chain die were imbedded within the test coupon thus providing 30 daisy-chains, equivalent to 60 wires (120 bonds), for monitoring. A 3.0 Ω increase in resistance constituted a failure with the cycles-to-failure data noted in Table 1. The first failure/high resistance bond occurred after exposure to 3000 cycles with a lapse of 1500 cycles till the second noted failure. Only 23% of the wires had failed after 5500 cycles when the test coupon was pulled from cycling.

Table 1. Thermal shock failure data for the daisy-chain test vehicles with imbedded die.

Daisy-Chain Wire Group	Cycles	Wire Group	Cycles
1	3,057	16	none
2	4,507	17	none
3	4,507	18	none
4	4,947	19	none
5	5,102	20	none
6	5,656	21	none
7	5,656	22	none
8	none	23	none
9	none	24	none
10	none	25	none
11	none	26	none
12	none	27	none
13	none	28	none
14	none	29	none
15	none	30	none

The failure data gathered from this test vehicle is indicative that the material properties selected will provide the long-term reliability solution for critical military electronics hardware. Compliant die attach adhesive enables stress relief from thermal induced stress in the silicon die-to-substrate interface while the wire bonds, coupled with a compliant encapsulant, provide the stress relief from environmental induced stress (thermal movement, mechanical shock, and vibration). This material set for packaging electronics, in conjunction with the design guidelines, enables the manufacturing of robust, reliable electronics assemblies.

Test Vehicle 2

A mixed-signal test vehicle (Figure 6) was designed and assembled to serve as a technology demonstration for the Navy's Standard Missile-2 (SM-2) program. The Navy's SM Program Office used this prototype in a flight test to support a technology demonstration of the Imbedded Component/Die Technology, validating the electrical and mechanical performance of this new and innovative electronics-packaging concept. A prototype was designed with a mix of analog and RF circuitry using imbedded design practices with wire bondable devices. The prototype circuit design was selected to demonstrate our imbedded packaging technology's capability to address miniaturization, thermal dissipation, component obsolescence, and reliability.

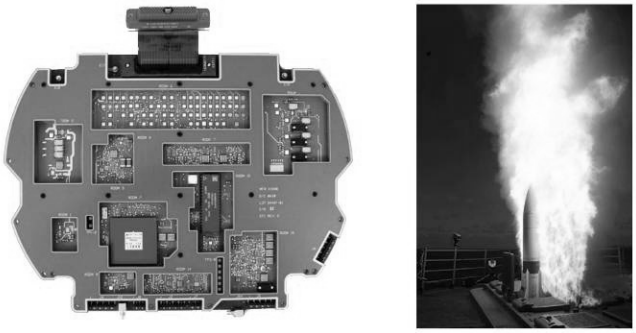


Figure 6. Mixed-signal prototype to demonstrate IC/DT[1] packaging technology's capabilities (*left*) and successful test flight of prototype on SM-2 missile (*right*).

Miniaturization objectives were largely achieved due to the ability to locate wire bondable components for the circuit. All ICs were procured as unpackaged components (wire bond face-up die), and passives with gold metallization were procured for imbedding into the prototype. Through elimination of the secondary packaging, a 66% reduction in surface area was achieved. This reduction enables the integration of future CCAs into a single assembly module (increased form, fit, and function through added capability within the same footprint).

All components, both actives and passives, were imbedded into cavities (Z-direction) in the laminate substrate. Multiple tiers were exposed in the substrate with strategic placement of components to decrease interconnect length (component-to-component bonding and component-to-substrate bonding) and address power dissipation. High-power devices were bonded with thermally conductive adhesive directly to an imbedded thermal core in the substrate. This eliminates the need for external heat sinks and lowers the devices' junction temperature, thus increasing device performance and longevity[6].

Flexible interconnects (Figure 7), such as aluminum wire bonds, were used to electrically interconnect the devices (component-to-component for point-to-point) and circuit (component-to-substrate for multi-point nodes). These flexible interconnects are able to absorb the thermal and mechanical stresses created when operating in harsh environments such as temperature and vibration/shock thus increasing robustness of the assembly. Elimination of secondary packaging, which facilitates bonding from component-to-component, decreases the number of failure opportunities in the system thus increasing overall reliability.

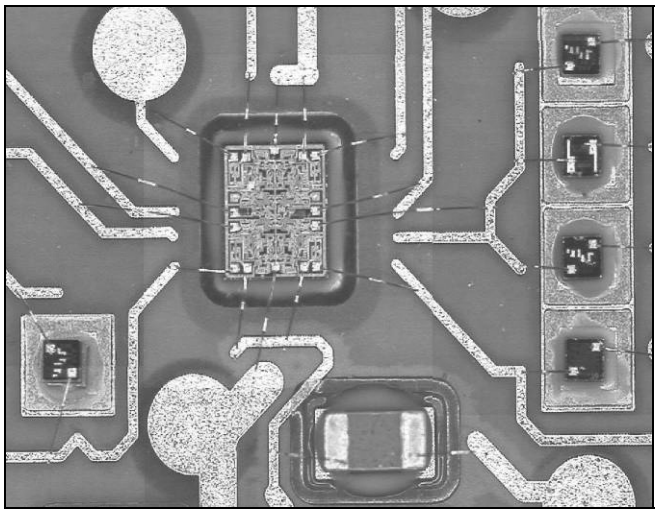


Figure 7. Wires bonded to electrically interconnect components on the prototype.

The IC/DT[1] prototype was analyzed and tested by SM-2 prime contractor Raytheon Missile Systems, which approved the prototype as flight hardware. This included finite element analysis (FEA) design modeling and prototype qualification testing per standard legacy performance requirements and overstress test requirements (extended temperature, humidity, vibration testing). In October 2007, the prototype's performance and robustness were demonstrated through a successful SM-2 flight test[5], thus advancing the packaging technology to TRL 8 status (TRL 8 Definition: Technology has been proven to work in its final form and under expected conditions. Examples include developmental test and evaluation of the system in its intended weapon system to determine if it meets design specifications[7].)

IMBEDDED PROTOTYPES

Since these early prototypes, the packaging technology has evolved to include not only wire bond components but also flip chip and standard surface mount devices (SMDs). With increasing processing levels and faster speeds, the need to incorporate a variety of first-level packages in an imbedded prototype is required. As many high-bandwidth processors have moved to area array style connections in high count fine-pitch bump arrays, there is an even greater need to address miniaturized connections to minimize electrical parasitics (improved performance) while also minimizing thermal parasitic (performance and long-term reliability).

Therefore, several prototypes have emerged using the packaging technology to address higher processing requirements within a smaller form factor using passive thermal management. One such prototype integrates eight flip chip field programmable processor arrays (FPPAs) and associate memory and decoupling/filter capacitors onto a single, high density substrate. This high-density FPPA array interposer may then be stacked and/or imbedded into other substrates (see Figure 8) to achieve the total number of processing elements (PEs) needed to achieve the processing power level required. Using the

imbedded packaging technology thus allows the overall size, weight, and power (SWAP) system design objective to be achieved.

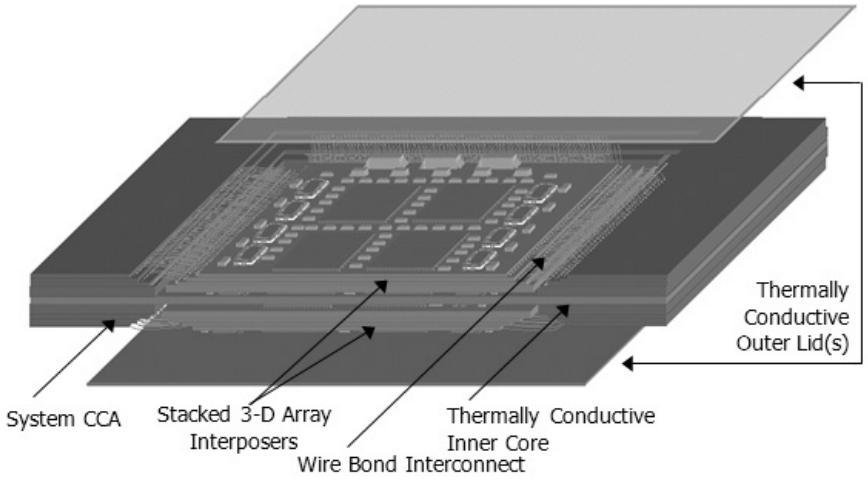


Figure 8. FPPA array interposers imbedded into a system board in a 3D array.

For a cost-driven prototype solution, imbedding die with SMD components is an attractive alternative. Both face-up die and standard soldered components may be integrated to provide a low-cost solution to meet form, fit, and function. Care is given to the proximity placement of face-up die to SMD components in order to avoid manufacturing issues. Process order of assembly and cleanliness are also critical issues than can provide challenges to the packaging designer. An example prototype of wire bonded die integrated in multiple cavities with soldered SMDs is shown in Figure 9.

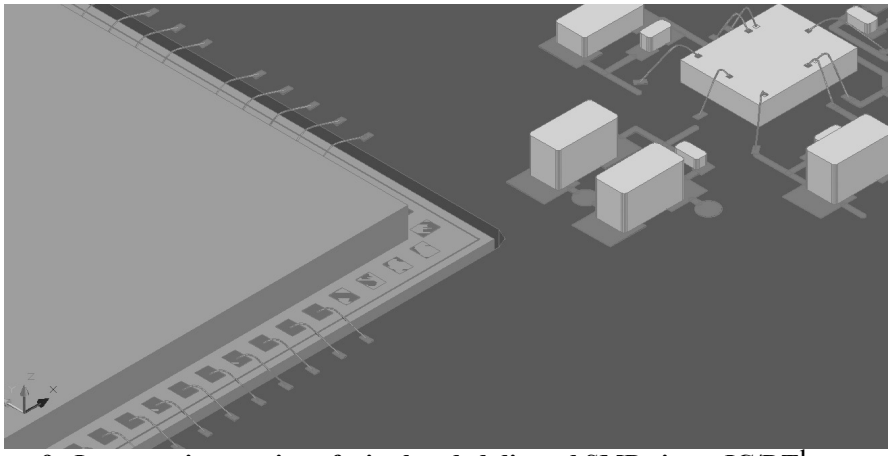


Figure 9. Low-cost integration of wire bonded die and SMDs in an IC/DT[1] prototype.

CONCLUSION

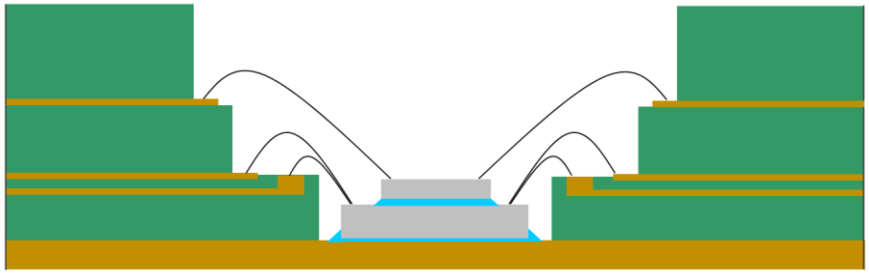
It is through the development of new materials and processes, i.e. packaging technologies, that have enabled the electronics industry to continue placing leap-ahead technology in the hands of consumers. The embedded packaging technology presented in this paper, Imbedded Component/Die Technology, is just one example of how leading-edge technologies can help system designers meet their size, weight, and power (SWAP) requirements in a cost-effective and reliable manner. Although imbedding components brings unique design and fabrication challenges over conventional technologies such as SMT, the prototypes presented are a demonstration that imbedding components in single-cavity and multi-cavity designs is both feasible and reliable. The testing of the two test vehicles demonstrated that this technology is a robust packaging technology for use in products that must operate in harsh environments. The first two test vehicles discussed in this paper have proven that the design guidelines, materials, and process parameters used to manufacture imbedded assemblies are capable of withstanding temperature, humidity, and shock stresses. Lastly, the recent prototypes designed and tested are a testament to the ability of packaging technologies to adapt to meet the toughest form, fit, and function requirements without sacrificing electrical, mechanical, or thermal performance.

ACKNOWLEDGEMENTS
The findings of this study could not have been accomplished without the support of the STI Microelectronics Lab under the direction of Mark McMeen. The author would like to acknowledge the efforts of Jonnie Johnson and David Robinson for support of the design, assembly, and test of the imbedded prototype assemblies.

REFERENCES
[1] STI Electronics, Inc. “Imbedded Component/Die Technology (IC/DT®)" U.S. Trademark Registration Number 3377731. 5 February 2008.
[2] Greig, Bill, “New (?) and Emerging (?) Technologies”, Advanced Packaging, July 2002.
[3] Hatcher, Casey, “Imbedded Component/Die Technology: An Innovative Packaging Solution for High Reliability,” *Pan Pacific Microelectronics Symposium*, February 2004.
[4] Raby et al. "Imbedded component integrated circuit assembly and method of making same." U.S. Patent 7,116,557. 3 October 2006.
[5] STI Electronics, Inc. "STI Electronics’ IC/DT Prototype Completes Successful SM-2 Flight Test." Press Release. Release October 12, 2007.
[6] Santarini, Michael, “Thermal Integrity: A Must for Low-Power-IC Digital Design”, EDN, September 2005.
[7] “Appendix B: Technology Readiness Level (TRL) Descriptions”, Retrieved May 5, 2008, from the NASA SBIR Web Site: http://sbir.nasa.gov/SBIR/sbirsttr2007/solicitation/appendix_B.pdf

Advanced Packaging Technologies

Imbedding Components for Increased Reliability



Casey H. Cooper

ccooper@stielectronicsinc.com

STI Electronics, Inc. ● www.stielectronicsinc.com

Outline

- Introduction
- Technology Description
- Technology Demonstrations
  - Test Vehicle 1
  - Test Vehicle 2
- Imbedded Component Prototypes
- Conclusion

Introduction

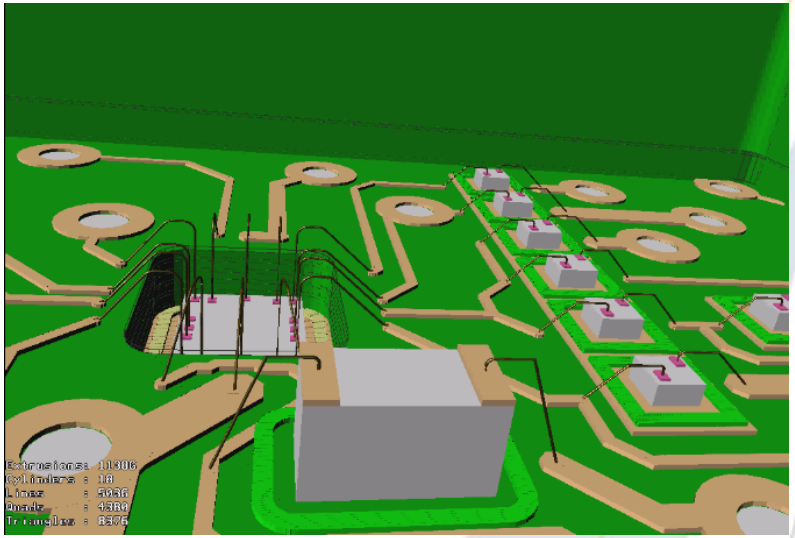
- Electronics Industry Objective
  - Improved **form**, **fit**, and **function**
- Key Requirements
  - Increased Capability
  - Reduced Size
  - Reduced Weight
  - Increased Reliability

Introduction

- Miniaturization through 3D Integration
  - MCM
  - SiP
  - COB
  - IC/DT®

Technology Description

- Imbedded Component/Die Technology (IC/DT®)
  - Enables the manufacturing and assembly of smaller, lighter, and more technologically advanced high density CCAs through imbedding unpackaged components in a 3-D laminate substrate with integrated thermal management.



Technology Description

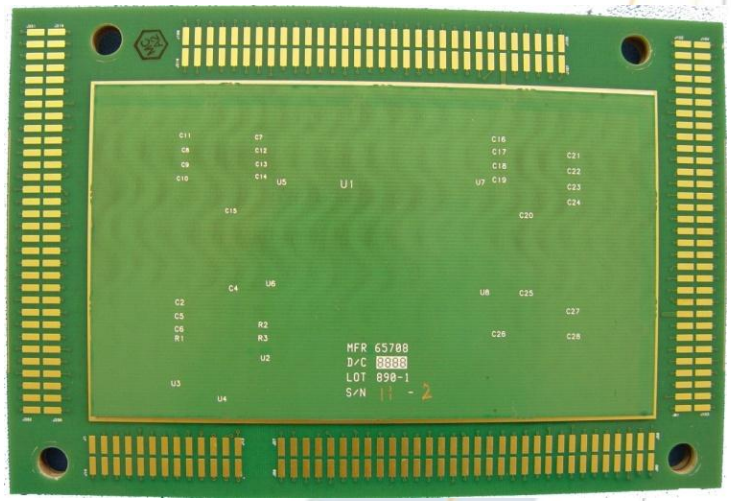
- Design Objectives:
  - Meet form factor requirements
    - Utilize smallest form and fit factor components, i.e. flip chip, bare die
    - 3-D component placement
  - Improve robustness/reliability
    - Low modulus die attach adhesive
    - Flexible wire bond electrical interconnect
  - Integrated thermal management design
    - Eliminate external cooling devices
    - Inner thermally conductive core layer and lid

Technology Prototypes

- Test Objective
  - To demonstrate the design guidelines, materials, and manufacturing processes used to imbed passive and active devices in a laminate substrate.
- Test Vehicles
  - TV1: Daisy-Chain Test Pattern
  - TV2: Mixed-Signal Prototype

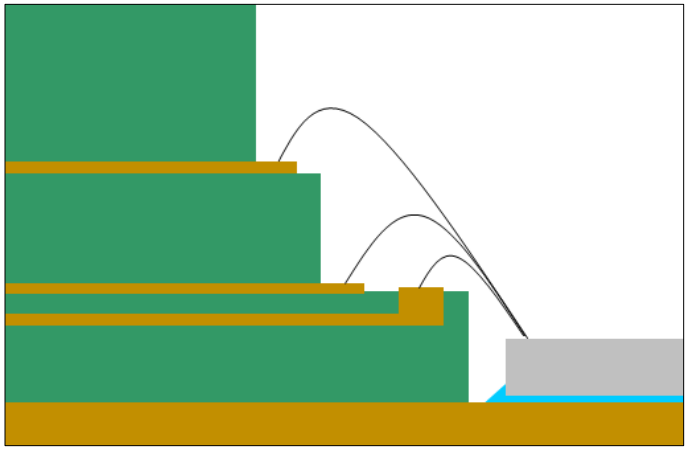
Test Vehicle 1

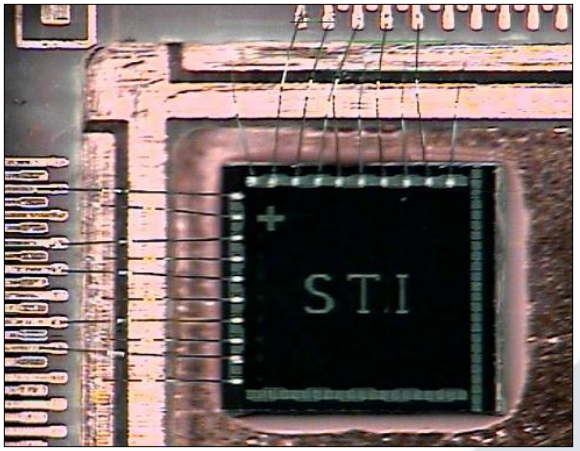
- Daisy-chain Test Pattern Configuration
  - Imbedded die cavity design
  - Multi-tier wire bonding
  - Imbedded thermal core
- Environmental Stress Testing
  - Thermal Shock
    - -55° C to 85° C
    - -55° C to 125° C



Test Vehicle 1

- Daisy-chain Test Pattern Configuration
  - 0.248in x 0.240in silicon die
  - Al/1%Si bond wire
  - Compliant die attach adhesive





Material Properties

- Key Material Properties
  - Glass Transition Temperature (Tg)
  - Coefficient of Thermal Expansion (CTE)
- Other Critical Material Properties
  - Cure Temp
  - Material Purity
  - Voiding
  - Moisture Absorption
  - One-part System

Test Vehicle 1

- Thermal Cycle Fatigue Failures
  - 1000 cycles from - 55°C to 85°C
  - 250 cycles from - 55°C to 125°C
  - 200 cycles from - 55°C to 85°C
  - 4200 cycles from - 55°C to 125°C

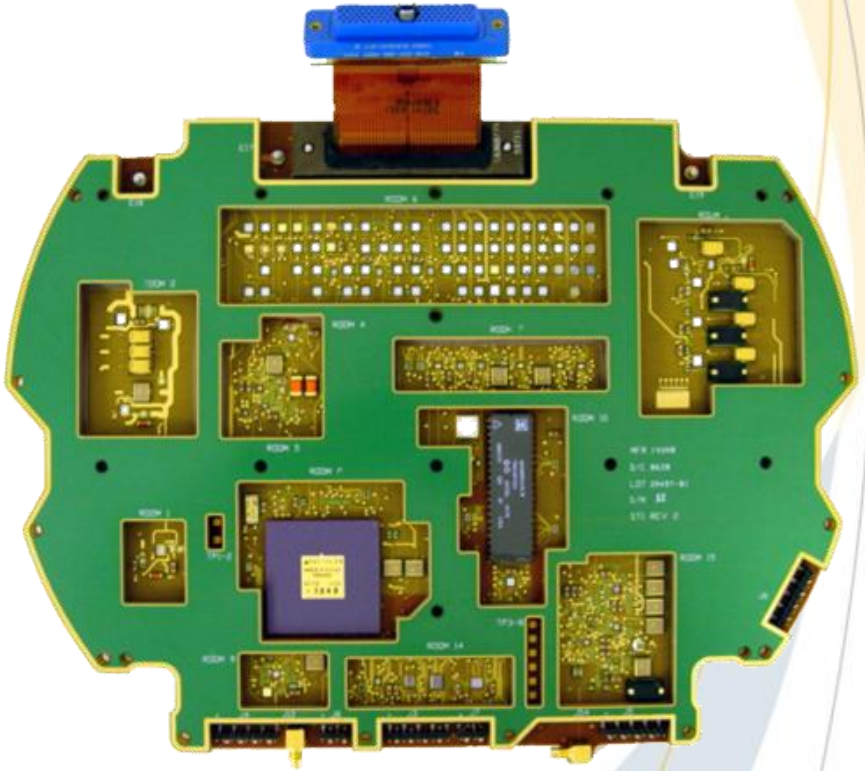
Daisy-Chain Wire Group	Cycles	Wire Group	Cycles
1	3,057	16	none
2	4,507	17	none
3	4,507	18	none
4	4,947	19	none
5	5,102	20	none
6	5,656	21	none
7	5,656	22	none
8	none	23	none
9	none	24	none
10	none	25	none
11	none	26	none
12	none	27	none
13	none	28	none
14	none	29	none
15	none	30	none

Test Vehicle 2

- Mixed-Signal Prototype
  - Redesign of a Navy Standard Missile-2 CCA using IC/DT® design practices
  - Included a mix of analog and RF circuitry
- Redesign Objective
  - To support a technology demonstration of the IC/DT® packaging technology, validating the electrical and mechanical performance of this new and innovative electronics-packaging concept

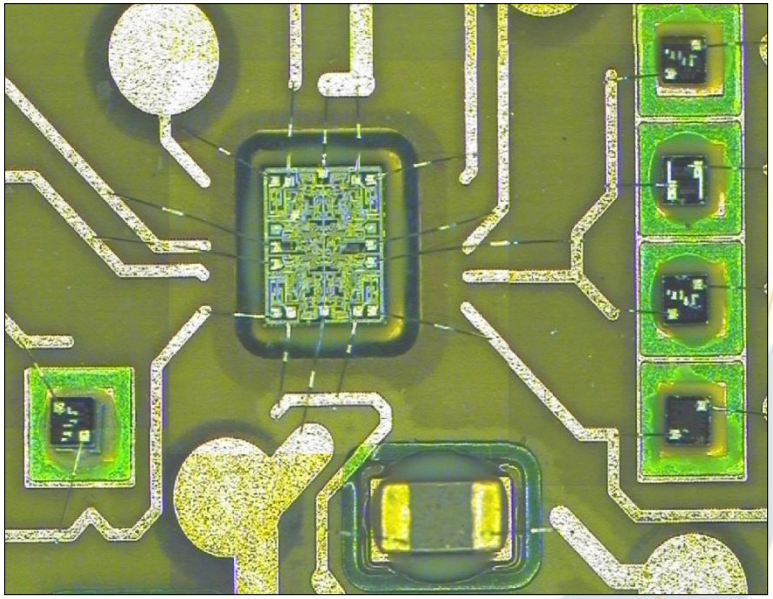
Test Vehicle 2

- Demonstrate ability to address:
  - Miniaturization
  - Component Obsolescence



Test Vehicle 2

- Demonstrate ability to address:
  - Thermal Dissipation
  - Reliability
  - Component Obsolescence
  - Chip-to-Chip Inteconnectivity



Test Vehicle 2

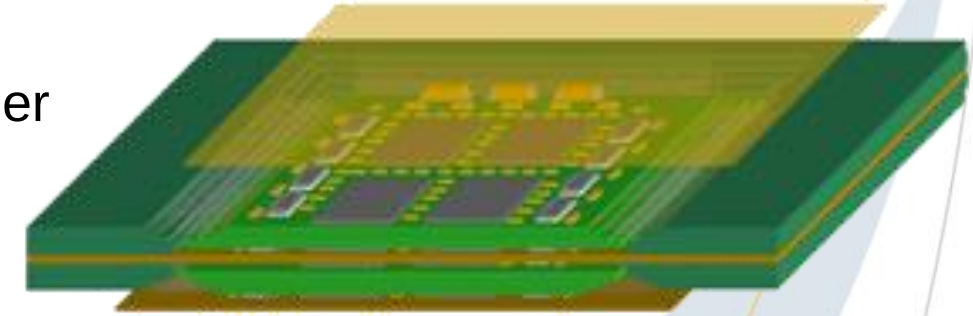
- Testing and Analysis:
  - FEA Design Modeling
  - IR Thermography
  - Standard Legacy Performance Qualification Tests
    - Extended Temp
    - Humidity
    - Vibration & Shock
- Flight Test
  - Oct 2007 Successful Test

Imbedded Prototypes

- IC/DT® Design Adaptation
  - To create a low cost, highly integrated small form factor assembly.
- Imbedded Prototypes
  - TV3: High-density Flip Chip & Wire Prototype
  - TV4: Multi-cavity SMD & Wire Prototype

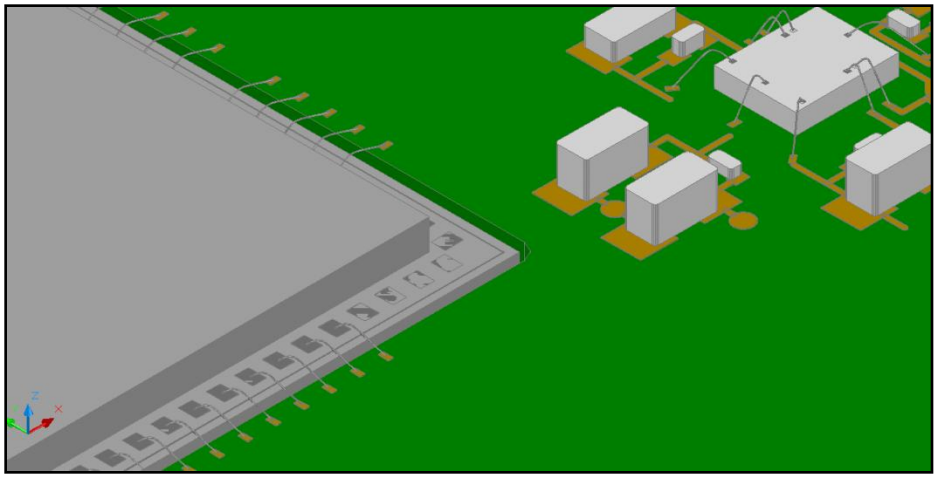
Test Vehicle 3

- Daisy-chain Test Pattern Configuration
  - High I/O Flip Chip
  - Wire Bond Die
  - SMDs
- Imbedded into Multi-Tier Cavity
  - Wire Bond Interconnect
    - GND Bond Tier
    - PWR (multi) Bond Tier
    - I/O Bond Tier



Test Vehicle 4

- Mixed-Signal, Low-Cost Configuration
  - Wire Bond Die
  - SMDs
- Imbedded into Multi-Tier Cavities
  - Wire Bond Interconnect



Conclusion

- Testing demonstrated that the IC/DT® is a robust packaging technology for use in harsh environments.
- Imbedded Prototypes
  - TV1: Daisy-Chain Prototype
    - Survived over 3000 cycles of thermal shock exposure
  - TV2: Mixed-Signal Prototype
    - Bench tested to meet flight qualification performance specifications
  - TV3: High-density Flip Chip & Wire Prototype
  - TV4: Multi-cavity SMD & Wire Prototype

Acknowledgements

- Many thanks to the efforts of Jonnie Johnson and David Robinson of the STI Microelectronics Lab