# Design To Manufacturing Standards

**Dieter Bergman, IPC**

# Design To Manufacturing Standards

**What's Now**
**What's New**
**What's Next**

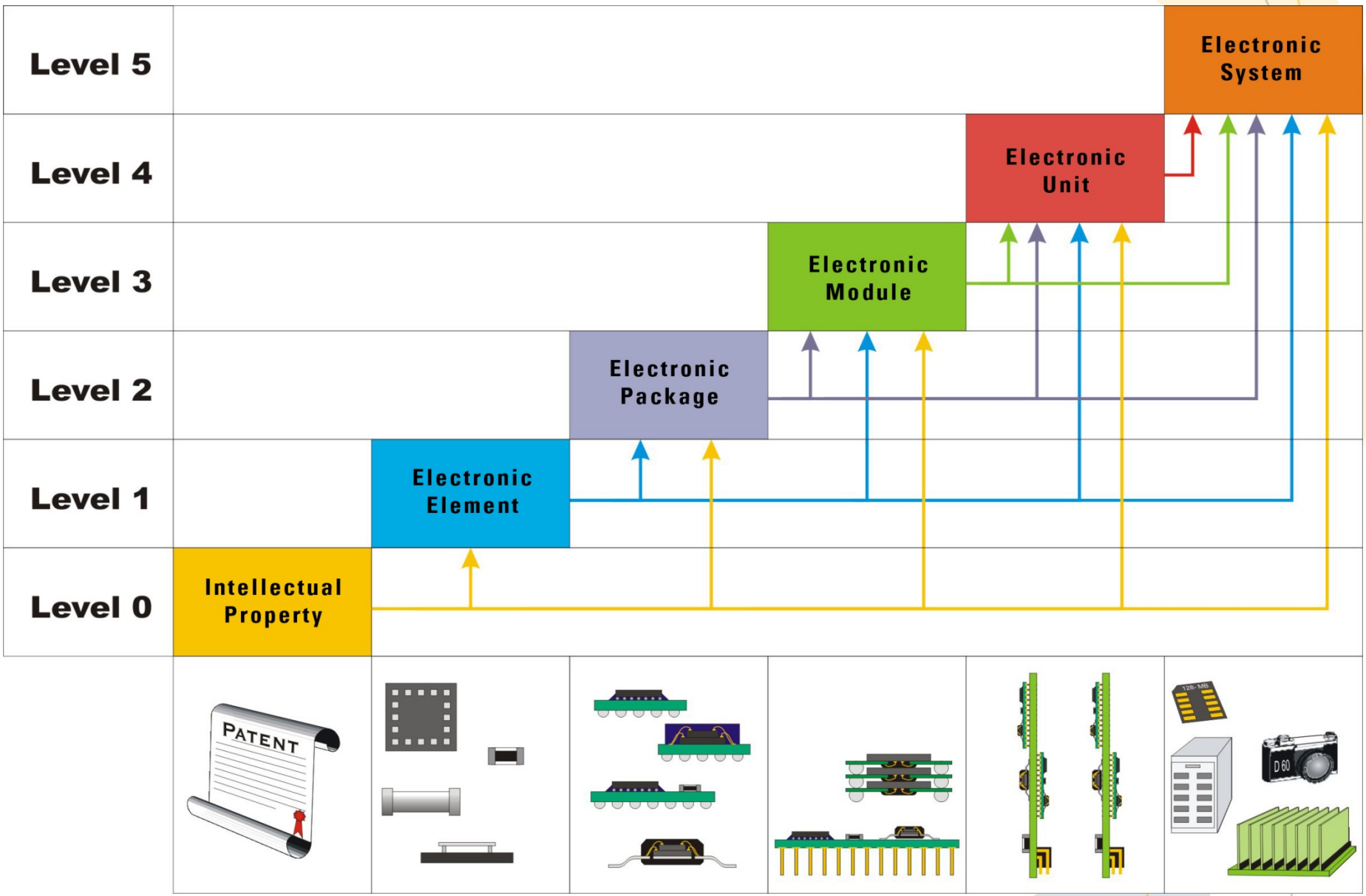
# Design to Manufacturing

- The “Design to Manufacturing Issues” cover an insight into all the concerns that must be considered as a new product is being introduced into the market place.
- The trade-offs and risk assessment are important in order to validate a path that can lead to a successful implementation for not only a single release, but for the entire product life cycle.
- Topics that must be considered are many and should address how they affect the development, prototype final production and product maintenance

# Discussion Topics

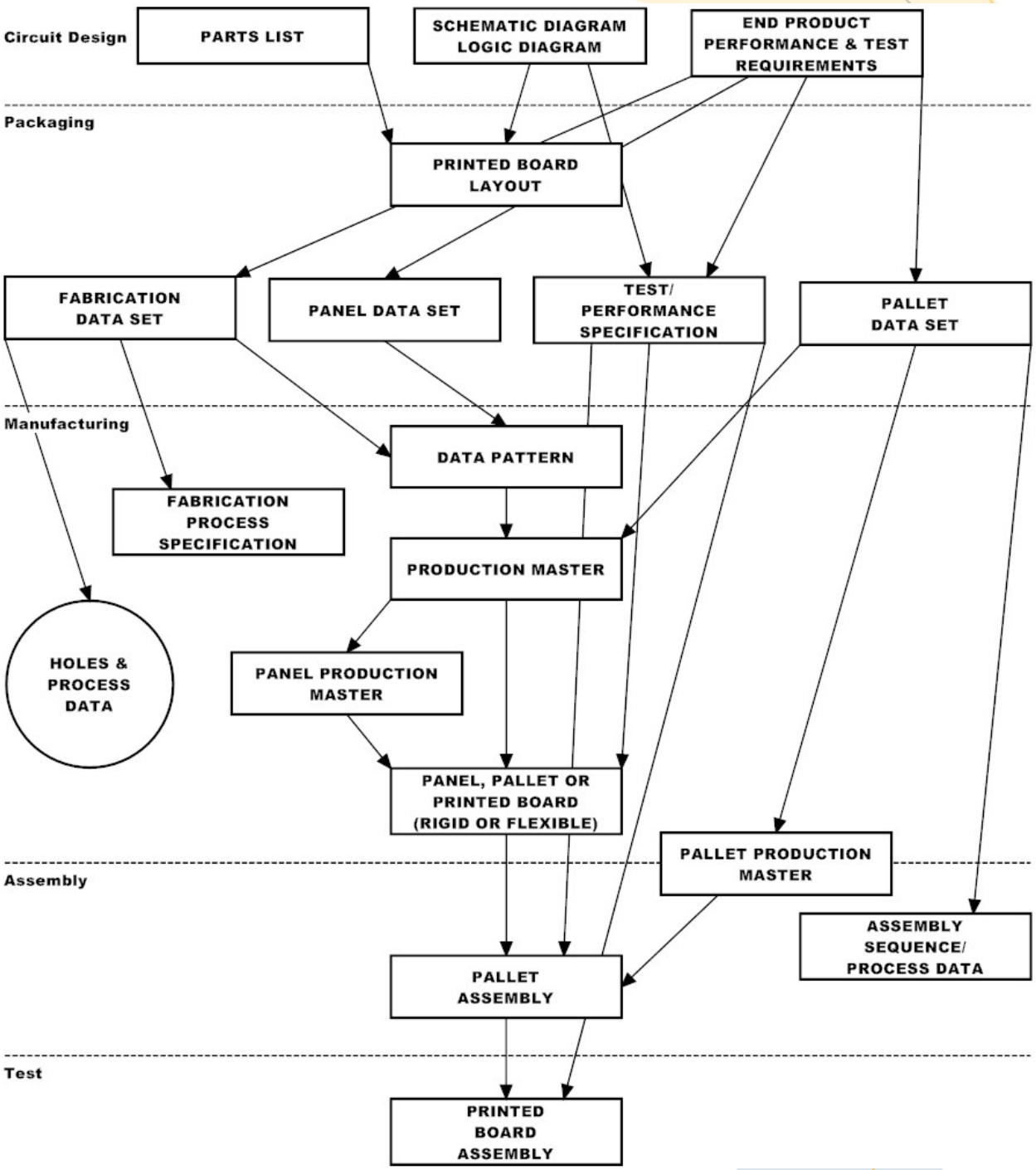
- The Information Process
- Knowing the jargon (terms & definitions)
- Defining the requirements
- Expansion of Documentation standards
- Document Grade and Completeness
- Relationship of CAD/CAM Data Standards
- Feed back mechanisms (archiving)
- Future activity

# Hierarchical Partitioning



## *Information Transfer*

- Circuit
- Packaging
- Manufacturing
- Assembly
- Test



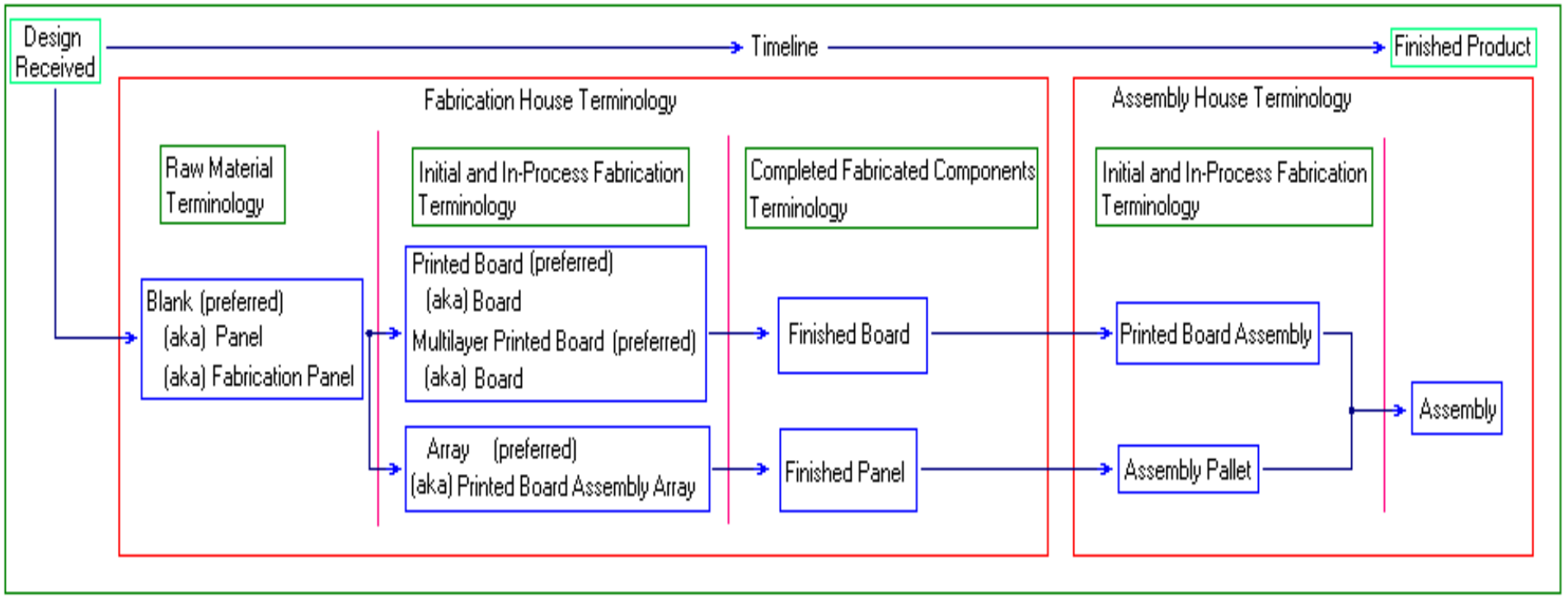
# Data Sets

- Each section is related and portions are interchanged between manufacturing disciplines in order to move the product through the various stages of manufacturing, maintenance and upgrading functions.
- Since the information is multi-faceted, each combination of documents is referred to as a data set.
- All five data sets make use of the generic requirement standard (IPC-2611) and the archiving standard (2611-1). The five data sets, and additional standards needed, are:
    - Electronic Data Set (2612, 2612-1, 2617, 2618)
    - Design Data Set (IPC- 2613, 2617, 2618)
    - Fabrication Data Set (IPC- 2614, 2615, 2617, 2618)
    - Assembly Data Set (IPC-2616, 2617, 2618)
    - Testing Data Set (IPC-2617)

# Terms and Definitions

Usage of IPC-T-50 Terminology During the PCB Fabrication and Component Population at an Assembly House

Flow Diagram



- **Blank *** **41.1339**

  An unprocessed or partially processed piece of base material or metal- clad base material, that has been cut from a sheet or panel, that has the rough dimensions of a printed board. (See also ‘‘Panel.’’)
- **Panel *** **41.1463**

  A rectangular sheet of base material or metal-clad material of predetermined size that is used for the processing of one or more printed boards and, when required, one or more test coupons. (See also ‘‘Blank.’’)
- **Fabrication Panel**

  A rectangular sheet of base material or metal-clad material of predetermined size that is used by a printed board manufacturer for the processing of one or more printed boards and, when required, one or more test coupons. (See also ‘‘Blank.’’)
- **Board *** **60.0118**

  see ‘‘Printed Board,‘‘ and ‘‘Multilayer Printed Board.’’
- **Printed Board *** **60.1485**

  The general term for completely processed printed circuit and printed wiring configurations. (This includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex base materials.)

- **Multilayer Printed Board *** **60.1227**

  The general term for a printed board that consist of rigid or flexible insulation materials and three or more alternate printed wiring and/or printed circuit layers that have been bonded together and electrically interconnected.
- **Finished Board**

  see “Printed Board”
- **Finished Panel**

  A rectangular sheet of base material or metal-clad material of predetermined size that is used for the processing of one or more printed board designs and, when required, one or more test coupons which is extracted from the fabrication panel to deliver to the customer or to the next level of fabrication. (see Assembly Pallet)
- **Assembly*** **80.1327**

  A number of parts, subassemblies or combinations thereof joined together. (Note: This term can be used in conjunction with other terms listed herein, e.g., ‘‘Printed Board Assembly’’)
- **Printed Board Assembly*** **80.0911**

  The generic term for an assembly that uses a printed board for component mounting and interconnecting purposes.
- **Array*** **22.0049**

  A group of elements or circuits arranged in rows and columns on a base material.

- **Printed Board Assembly Array**

  A group of assemblies, all of the same design, arranged in rows and columns on a panel.
- **Assembly Pallet**

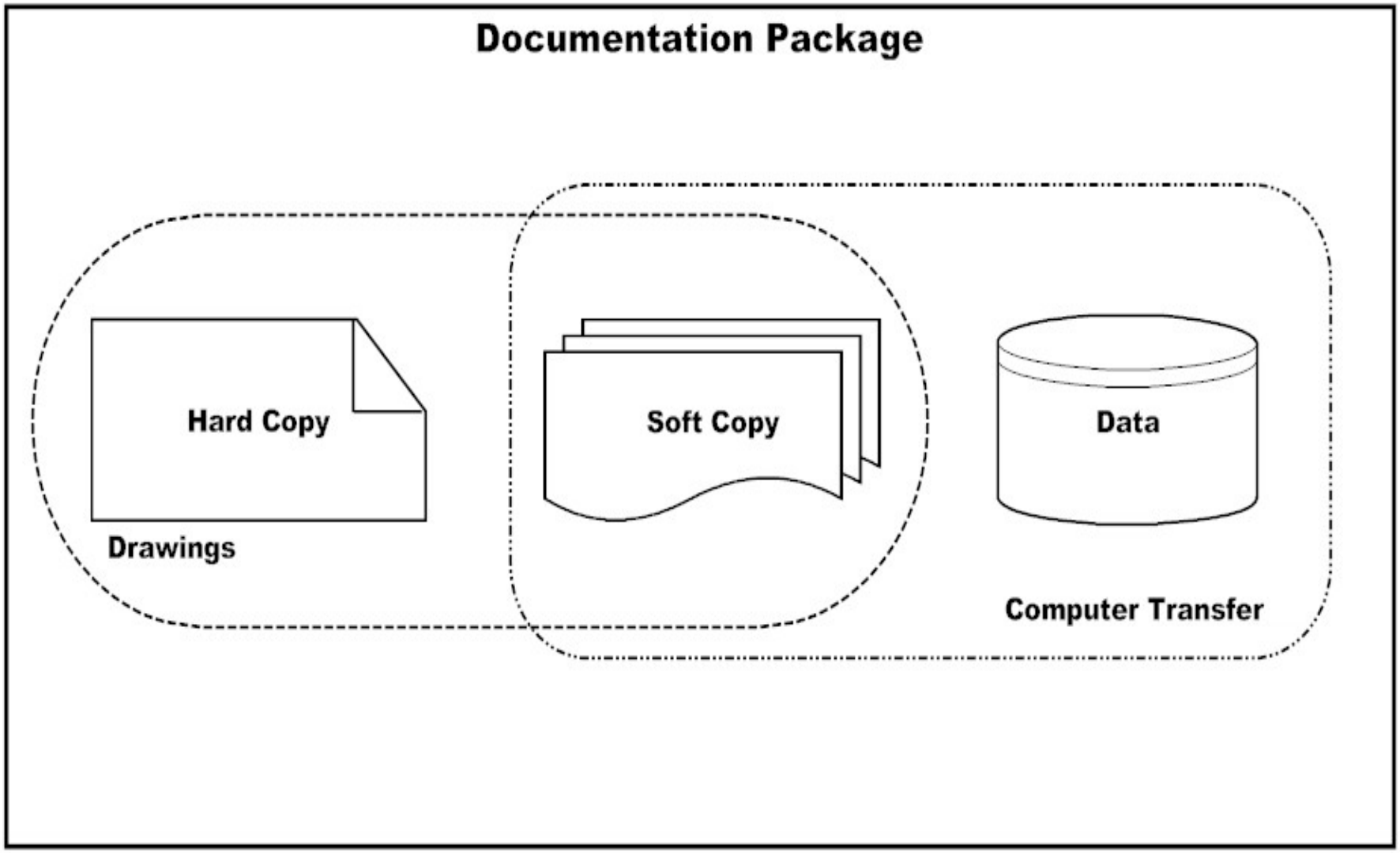
  The generic term for the assembly that uses a finished panel, as delivered from the board fabricator, of the same or different designs, for element and circuit component mounting and attachment to the board interconnections layers. The board arrangement on the pallet may be random or in the form of an array; the pallet may also include coupons for testing.

# ***Data***

- Intelligent information that may be used directly by machine in order to accomplish a particular manufacturing event.

# Drawings

- Hard or Soft copy (example pdf etc.) which requires human interpretation.
- Formatting criteria applies only to this type of documentation.


Documentation Package
Hard Copy
Drawings
Soft Copy
Data
Computer Transfer

# Computer Transfer

- The term “drawing” can be provided in either hard or soft copy; where soft copy is a bitmap in an electronic format.
- The goal is to remove all forms of paper, another term for computer transfer methodology embodies the two methods of providing information that is sent via internet or electronic computer transfer.
- This may also be accomplished with soft copy or data; soft copy requires human interpretation, data requires machine execution

# Documentation Series IPC-2610

***IPC-2611*** - Generic Requirements for Electronic Product Documentation

***IPC-2612*** - Sectional Requirements for Electronic Diagramming Documentation (Schematic and Logic Descriptions)

***IPC-2613*** - Sectional Requirements for Electrical, Mechanical and Discrete Wiring Part Descriptions Documentation (specification control, source control, wire harness and cabling)

***IPC-2614*** - Sectional Requirements for Board Fabrication Documentation (Printed Circuit board Description Including Embedded Passives)

***IPC-2615*** - Sectional Requirements for Dimensions and Tolerances

***IPC-2616*** - *Sectional Requirements for Assembly Documentation* (electronic printed board and module assembly descriptions)

***IPC-2617***- *Sectional Requirements for Board and Assembly Testing* (electrical, environmental, HAST, HALT, etc. test)

***IPC-2618*** -Sectional Requirements for Bill of Material Documentation (Complete Listing of Parts, Materials, & Procurement Documents)

# IPC-2610 Classification

- **Grade A**
  - All hard copy; completeness 1,2 and 3
- **Grade B**
  - Mixed hard copy and electronic data, completeness 1, 2 and 3
- **Grade C**
  - All electronic data, completeness 1, 2, and 3

Documentation Package
Grade Requirements

| A | B | C |
|---|---|---|
| 60-90% Hard Copy (Drawings) | 0-60% Hard Copy (Drawings) | 0-40% Soft Copy (Drawings) |
| | 10-60% Soft Copy (Drawings) | 40-100% Maximum Data |
| 10-40 % Minimal Data | 10-80% Nominal Data | |

# Completeness Criteria

| Name | Full | Design | | | Fabrication | | | Assembly | | | Test | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 |
| Hierarchical layer/stack instance files | Y | N | Y | N | N | N | N | N | N | N | N | N | N |
| Hierarchical conductor routing files | Y | N | Y | N | N | N | N | N | N | N | N | N | N |
| BOM (Components and Materials) | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | N | Y | Y |
| AVL (Components and Materials) | Y | N | Y | Y | N | Y | Y | Y | Y | Y | N | N | Y |
| Component Packages | Y | Y | Y | Y | N | N | Y | Y | Y | Y | N | Y | Y |
| Land Patterns | Y | N | Y | Y | N | N | Y | N | Y | Y | N | Y | Y |
| Device Descriptions | Y | Y | Y | Y | N | N | N | N | N | Y | N | N | Y |
| Component Descriptions | Y | Y | Y | Y | N | N | N | Y | Y | Y | N | Y | Y |
| Soldermask; Solder Paste Legend Layers | Y | N | N | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| Drilling and Routing Layers | Y | N | N | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| Documentation Layers | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| Net List | Y | Y | Y | Y | N | Y | Y | N | Y | Y | Y | N | Y |
| Outer Copper Layers | Y | N | N | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| Inner Layers | Y | N | N | Y | Y | Y | Y | N | Y | Y | N | N | Y |
| Miscellaneous Image Layers | Y | N | Y | Y | N | Y | Y | N | Y | Y | N | Y | Y |
| DFX Analysis | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |

# Grade & Completeness

| | A | B | C |
|---|---|---|---|
| **1** | Napkins | PDF/Word<br>Design Stats<br>PowerPoint | Formatted data file, Gerber |
| **2** | Paper Plots | Gerber / NC Drill | D-356,<br>Partial IPC-2580 |
| **3** | Mylar<br>Paper<br>Tape | Gerber<br>NC Drill<br>Formatted Drawings | IPC-2580<br>CAD DB<br>ODBX |

# Minimum Drawing Requirements

The documentation of a printed board assembly consists of several drawing and data types that are included or referenced in the documentation package.

Not all drawings or data are supplied to the fabricator or to the assembly company; however, the designer must have a good understanding of the minimum information necessary to convey the design intent.

# Minimal Documentation

The **IPC-D-325** defines three types of documentation packages. These are:

**Class A:** Minimal Documentation

- Usually used for internal use and consists primarily of a copy of the layout and artwork in hard copy or NC format.
- The information requires a great deal of coordination between the design and manufacturing disciplines.
- Notes on the layout convey much of the needed information.
- Class A documentation requires the use of a manufacturer that can produce a functional product from the information supplied.

2611 Grade: A1, **B1** or C1

# Moderate Documentation

**Class B:** Moderate Documentation

- Includes a complete board description without information as to the manufacturing allowances that are included in the design.
- The parts list and assembly drawing are also supplied to the assembler.
- CAD data on conductor routing describes the interconnectivity of the circuit and is used by the manufacturer to derive electrical test data. A schematic, logic diagram, or net list may also be supplied.
- Class B documentation requires working with a manufacturer and assembly company that has a strong CAD/CAM background and an understanding of what the designer expects.

2611 Grade: A2, **B2** or C2

# Full (Complete) Documentation

**Class C:** Full Documentation

- This includes a complete procurement package that may be sent to multiple suppliers with each producing an identical part.
- The data, as a minimum, the master drawing, the assembly drawing, bill of material (BOM), schematic or logic diagram, test specs, artwork in hard copy and electronic form, and an electronic description of the design.
- In addition, a panel layout may also be included, especially if the assembly is to be built in panel format.
- The tooling features are defined and located and manufacturing allowances included in the design are identified.

2611 Grade: A3, **B3** or C3

# Need for Intelligent Data Transfer

Highly organized, integrated, related, clear

IPC-2581, GenCAM, EDIF, AP210, IPC-D-350
EDA DBs, Alg, Men, RR, ...
CAM DBs, GenCAD, PDW, FATF, ODB++

Flat, vague assumptions which need additional data to interpret requirements

BOMs, CPLs, Netlists
Gerber, drill
Plots... HPGL, PS, PDF, ...
Phone calls, paper

# ***What's Involved in the Documentation Package***

- Fabrication Drawings
- Assembly Drawings
- Bill of Materials
- Schematic or Logic Diagrams
- Wiring Diagrams
- Specification Control Drawings
- Electronic Data
- Mechanical Drawings

# 2611- Order of Precedence

The order of precedence, from top to bottom as follows, **shall** prevail:

- The procurement contract
- An approved documentation package (supplemented by an approved deviation list, if applicable)
- Company specific manufacturing standard
- The 261X standard
- Other applicable documents

The 2611 standard represents the generic requirements for electronic product documentation. The details of documentation requirements are contained in the specific part of the IPC-2610 series of standards. Each standard has a specific focus and **shall** be used, as appropriate, to describe a particular part of the electronic product details.

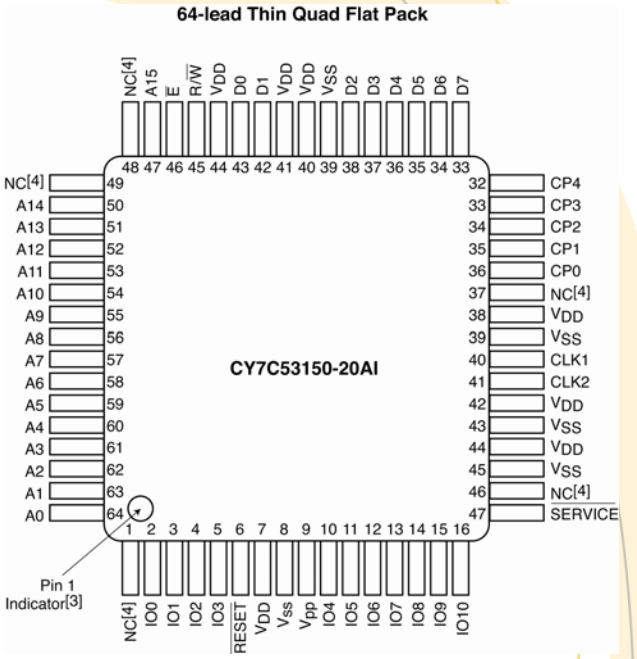
# 2612 - Schematic Completeness

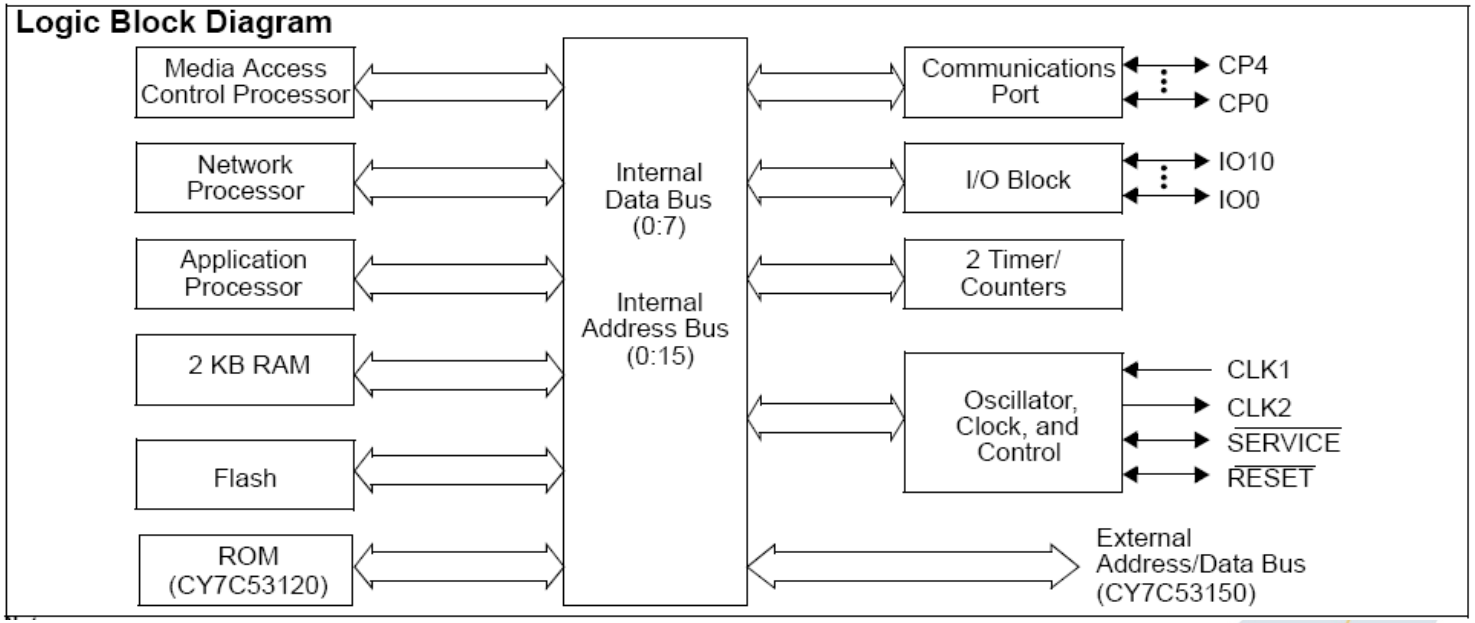
| Description | Mode 1 | Mode 2 | Mode 3 |
|---|---|---|---|
| Symbol and function | Y | Y | Y |
| Circuit Flow | N | Y | Y |
| Signal Names | N | Y | Y |
| Critical Circuit Identification | N | N | Y |
| Critical Signal Identification | N | Y | Y |
| Reference designator Assignment | N | Y | Y - Left to right preferred |
| Off sheet reference assigned | N | Y | Y |
| Component Indexing | N | N | Y |
| Fixed Pin and Gate Assignment | N | N | Y |
| Symbol Pin Number indication | N | N | Y |

# 2612 Net Attribute Descriptions

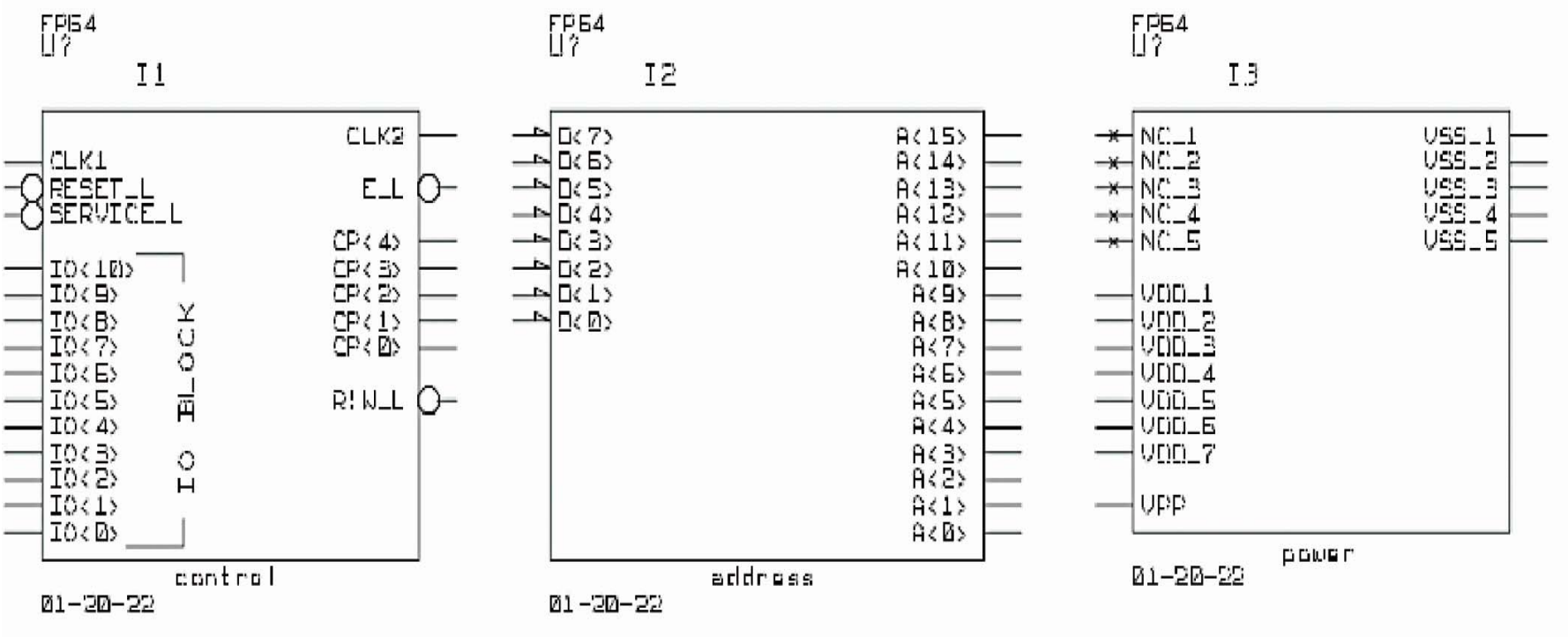
- Net attribute “SL” could be used to indicate a short net length for component placement purposes (e.g. this attribute will be placed on the net connecting a clock output to its’ series terminating resistor).
- Net attribute “CI” could be used to indicate routing on a controlled impedance layer.
- ECL pin attributes “S”, “L”, and “T” will be used to indicate source, load, and termination and will drive “ECL” style net routing (i.e. the route will have the “S” and “T” pins as it’s end points, and the “L” pins will be through routed with no net stubs, or minimal length net stubs if required for device fanout).
- Pin attributes “B” and “3” could be used to indicate bidirectional, load or a source, while the “3” indicates a three state condition, either a source (high or low) or be turned off. Bidirectional programmable logic pins could use the attributes “BS” or “BL” to signify the final state after the logic is initialized is either a source or a load.
- A net will usually contain no more than one pin with an “S” attribute. Two “T” attribute pins may be used in the case of Thevinin terminations.
- Net attribute “C” could be used to identify nets constrained in some other fashion, which will be documented with a schematic note.

# Part and Functional Diagram Conversion 2612-1

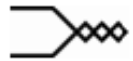


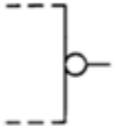
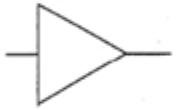
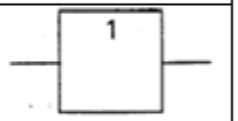
# 2612-1 Logic Representation



# General Discrete Symbols

| | | | |
|---|---|---|---|
| Attenuator, Fixed |  | A fixed **attenuator** is an electronic device that reduces the amplitude or power of a signal without appreciably distorting its waveform. Attenuators are usually passive devices made from resistors. The degree of attenuation is fixed. | |
| Attenuator, Variable |  | An variable **attenuator** is an electronic device that reduces the amplitude or power of a signal without appreciably distorting its waveform. The degree of attenuation is continuously adjustable, or incrementally adjustable. | |
| Crystal, Piezoelectric |  | A piezoelectric crystal is a device that has the ability to generate an electrical response to a mechanical stress | |
| Delay Line |  | A delay line symbol a device where the input signal reaches the output of the device after a known period of time has elapsed. |  Alternate |
| Directional Coupler |  | Directional couplers are passive devices used in the field of radio technology that couple parts of the transmission power in a transmission line by a known amount out through another port. |  Alternate |
| Thyristor |  | A thyristor a solid state semiconductor device with four layers of alternating N and P-type material which acts as a switch. | |
| Thermocouple |  | A thermocouple is a device that is a temperature sensor and can also be used to convert thermal differences to electrical potential. |  Alternate |

# Logic and Truth Tables

| | | |
|---|---|---|
| Integrated Circuit |  | A general integrated circuit symbol represented as a rectangle that can serve to describe various logic functions related to the principles identified in sections 7.2 through 7.8. |
| Negated Input |  | The external 0-state shown by the negated input symbol produces the internal 1 state. Note: the connection line may be drawn through the negation symbol |
| Negated Output |  | The internal 1-state shown by the negated output symbol produces the external 0- state. Note: the connection line may be drawn through the negation symbol |
| Inverter |  | The inverter is a logic device that has an output opposite of the input. The inverter performs an opposite function of a rectifier. |
| Buffer |  | The general symbol for a buffer without a specially amplified output. The output stands at its 1-state if and only if the input stands at its 1-state   |
| Exclusive-Or Gate |  | An exclusive-or gate implements exclusive disjunction where a HIGH (1) output results if one and only one of the inputs is HIGH (1). If both inputs are LOW (0) or HIGH (1) a LOW (0) output results. |
| And Gate |  | An And Gate implements logical conjunction. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input is HIGH, a LOW (0) output results. |

| Input | | Output |
|---|---|---|
| A | B | A, X, or B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

| Input | | Output |
|---|---|---|
| A | B | A And B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

# Reference Designators

| | |
|---|---|
| **A** | separable assembly |
| **AR** | amplifier |
| **AT** | attenuator; isolator |
| **B** | blower, motor |
| **BT** | battery |
| **C** | capacitor |
| **CB** | circuit breaker |
| **CN** | capacitor network |
| **CP** | connector adapter, coupling |
| **D or CR** | diode |
| **D or VR** | breakdown diode |
| **DC** | directional coupler |
| **DL** | delay line |
| **DS** | display, lamp, light emitting diode |
| **E** | terminal |
| **F** | fuse |
| **FD*** | fiducial |
| **FL** | filter |
| **G** | generator, oscillator |
| **GN** | general network |
| **H** | hardware |
| **HY** | circulator, directional coupler |
| **J** | most fixed of connector pair, jack |
| **K** | contactor, relay |
| **L** | coil, inductor, bead, ferrite bead |
| **LS** | loudspeaker, buzzer |
| **M** | meter |
| **MG** | motor-generator |
| **MH*** | mounting hole |
| **MK** | microphone |
| **MP** | mechanical part |
| **P** | most movable of connr pair, plug |
| **PS** | power supply |
| **Q** | transistor |
| **R** | resistor |
| **RN** | resistor network |
| **RT** | thermistor |
| **S** | switch |
| **T** | transformer |
| **TB** | terminal board, terminal strip |
| **TC** | thermocouple |
| **TP**** | test point, In-circuit test points |
| **TZ** | transzorb |
| **U** | inseparable assembly, IC pkg |
| **V** | electron tube |
| **VR** | voltage regulator |
| **W** | wire, cable, cable assembly |
| **X** | socket, fuse holder, lamp holder |
| **Y** | crystal, magnetostriction osc |
| **Z** | miscellaneous |

# Fabrication Requirements

| Characteristics | Requirements |
|---|---|
| Board Details | 1. The type, size and shape of the printed board and all tolerance requirements.<br>2. Dielectric separation between layers.<br>3. Bow and twist allowances.<br>4. Overall board thickness requirements including tolerances. |
| Materials | 1. Type, Class and Grade of material, including color if applicable.<br>2. Electrical properties of the material i.e. permittivity, loss tangents<br>3. Plating and coating material(s) type and thickness(es).<br>4. Marking inks or paint and permanency.<br>5. Embedded component materials |
| Hole Details | 1. The size, location and tolerances for all holes.<br>2. The plating requirements for all holes.<br>3. The hole cleaning requirements including if etchback is required or permitted. |
| Conductor Definition | 1. Shape and arrangement of both conductor and non-conductor patterns on each layer of the printed board. 2. Conductor width and spacing on the finished printed board.<br>3. Dimensions and tolerances for critical pattern features which may affect circuit performance.<br>4. Conductor layer identification starting with the primary side, the next conductive layer **shall** be Layer 2. (For assemblies with components on both sides the most complex or densely populated side **shall** be Layer 1.) |
| Embedded Components | Formed passive component requirements<br>Formed active component requirements<br>Inserted passive component requirements (including BOM information and assembly instructions)<br>Inserted active component requirements (including BOM information and assembly instructions) |

# Fabrication Requirements

| Characteristics | Requirements |
|---|---|
| Marking | 1. Printed board identification marking.(may include Bar Code)<br>2. Printed board revision (may include layer Rev identification)<br>3. Size, shape and location of reference designation and legend marking, if required.<br>4. Traceability marking and/or date code and serial number (when required).<br>5. Location and size requirements for fabricator's I.D., UL, ESD marking and cage code.<br>6. Appropriate material marking requirements perJ-STD-609. |
| Processing Conditions | 1. Processing allowances that were used in the design of the printed board, including but not limited to:<br>a. Conductor width allowance [LMC and MMC]<br>b. Conductor spacing allowance [LMC and MMC]<br>c. Land/hole fabrication allowance [LMC and MMC]<br>d. Solder mask or cover layer registration allowance [DTP]<br>e. Layer to layer registration requirements<br>2. Applicable processing specifications.<br>3. Location of quality conformance coupons or circuitry. |
| Design Concepts | 1. Maximum rated voltage (maximum voltage between two non-connected adjacent conductors with the greatest potential difference).<br>2. Identification of testing and test point locations (when applicable).<br>3. Modular grid system(s) used and application (component placement, test points, etc.):<br>a. Metric grid smallest increments. Inch based grid smallest increment |
| Documentation | 1. Terms used on the Fabrication data set **shall** conform to this standard and IPC-T-50.<br>2. Notes either included on the first sheet(s) or location of notes specified on the first sheet(s) |

NOTES

| Note Type Category [Note code] | Completeness | | | Comments |
|---|---|---|---|---|
| | Mode 1 | Mode 2 | Mode 3 | |
| **Specification Reference [SR]** | | | | |
| Design Specifications [d] | O | O | M | |
| Performance Specifications [p] | M | M | M | |
| Quality Control Specifications [q] | O | M | M | |
| Material Specifications [m] | O | O | M | |
| Restrictive Material Identification [r] | O | O | O | |
| Electronic Data Formats [e] | O | M | M | |
| Internal Company Specifications [c] | O | O | O | |
| International Specifications [i] | O | O | O | |
| Unique Specifications References [u] | O | O | O | |
| **Quality Requirements [QR]** | | | | |
| Minimum acceptability [a] | M | M | M | |
| Workmanship Requirements [w] | M | M | M | |
| Modification and Repair [m] | O | M | M | |
| Coupon and Delivery Requirements [c] | O | O | M | |
| Process Control Reporting [p] | O | O | M | |
| Test Requirements [t] | O | O | M | |
| Unique Quality Assessment Requirements [u] | O | O | O | |
| **General Material [GM]** | | | | |
| Metallic Heat Sink Foil/Film [h] | O | O | O | |
| Non-Organic Materials [c] | O | O | O | |
| **Rigid Material [RM]** | | | | |
| Core Base Material [b] | M | M | M | |
| Prepreg Material [p] | O | O | M | |
| Reinforcement Materials [r] | O | O | M | |
| Copper Foil [c] | M | M | M | |
| Unique Rigid Board Material [u] | O | O | O | |
| **Flexible Material [FM]** | | | | |
| Core Base Material [b] | O | O | M | |
| Adhesive Material [a] | O | O | M | |
| Cover Layer Material [c] | O | O | M | |
| Copper Film [f] | O | O | M | |
| Unique Flexible Material [u] | O | O | O | |

NOTES

| Note Type Category [Note code] | Completeness | | | Comments |
|---|---|---|---|---|
| | Mode 1 | Mode 2 | Mode 3 | |
| **End Product Physical Descriptions [EP]** | | | | |
| Hole from/to descriptions [f] | M | M | M | |
| HDI layer Structure [h] | O | M | M | |
| Edge Definition Requirements [e] | O | O | M | |
| Board from Panel Excising [p] | O | M | M | |
| Board X out allowance [x] | O | O | M | |
| Via Fill or Tenting strategy [v] | O | O | M | |
| Etchback and desmear requirements [d] | O | O | M | |
| Flexing (to install or continuous) [f] | O | O | O | |
| Unique End Product Physical Descriptions [u] | O | O | O | |
| **Tolerance Variation Details [TV]** | | | | |
| Printed Board Peripheral [p] | O | M | M | |
| Printed Board Thickness [t] | O | M | M | |
| Printed Board Bow and Twist [b] | O | M | M | |
| Hole/Feature Location [l] | M | M | M | |
| Hole/Feature Size [s] | M | M | M | |
| Dielectric Separation [d] | O | O | M | |
| Electrical Variation [e] | O | M | M | |
| Conductor and Space [c] | M | M | M | |
| Impedance Variations [i] | O | O | M | |
| Unique Tolerance Variation Details [u] | O | O | O | |
| **Embedded Components [EC]** | | | | |
| Formed components [f] | O | O | M | |
| Inserted components [i] | O | O | O | |
| Unique Embedded Components [u] | O | O | O | |
| **Electrical Test Requirements [ET]** | | | | |
| Open and short testing (Continuity) [o] | M | M | M | |
| Hi Pot testing [h] | O | O | M | |
| Maximum rated Voltage [v] | O | M | M | |
| Conductor Impedance testing [i] | O | O | O | |
| Dielectric withstanding voltage [d] | O | O | M | |
| Highly Accelerated Stress Testing [s] | O | O | O | |
| Burn in Requirements [b] | O | O | M | |
| Cleanliness Testing [c] | O | M | M | |
| Environmental screening tests [e] | O | O | M | |
| Thermal stress testing [t] | O | M | M | |
| Unique Electrical Test Requirements | O | O | O | |

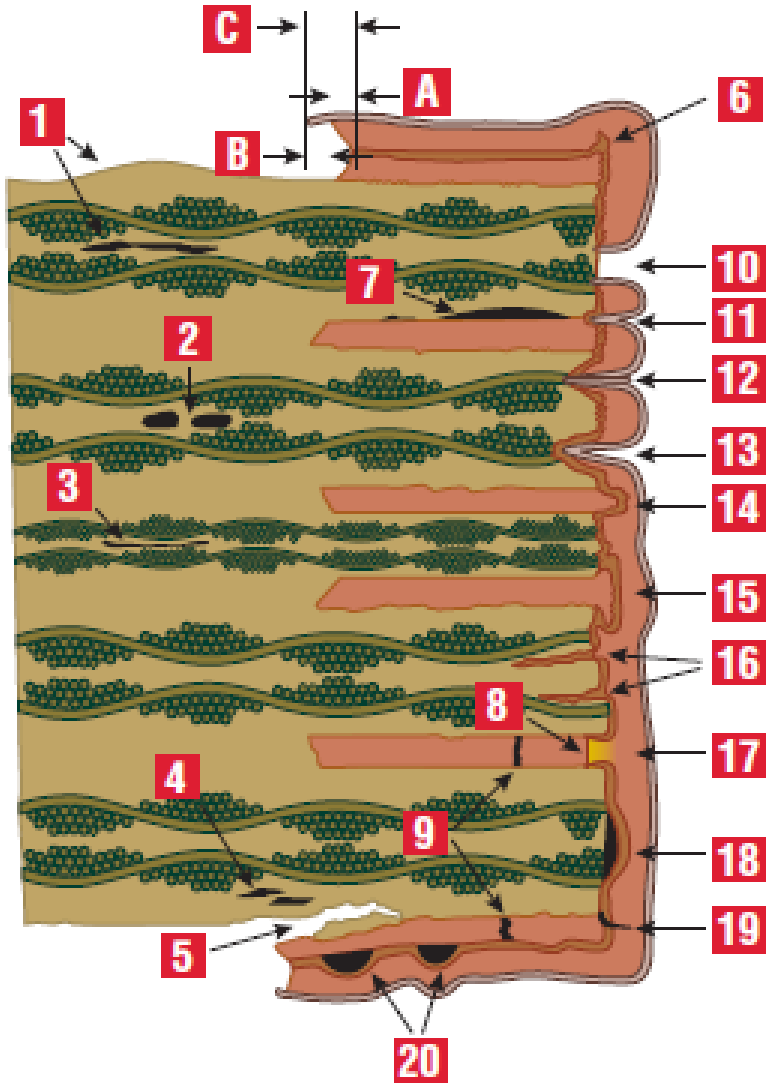
NOTE EXAMPLES

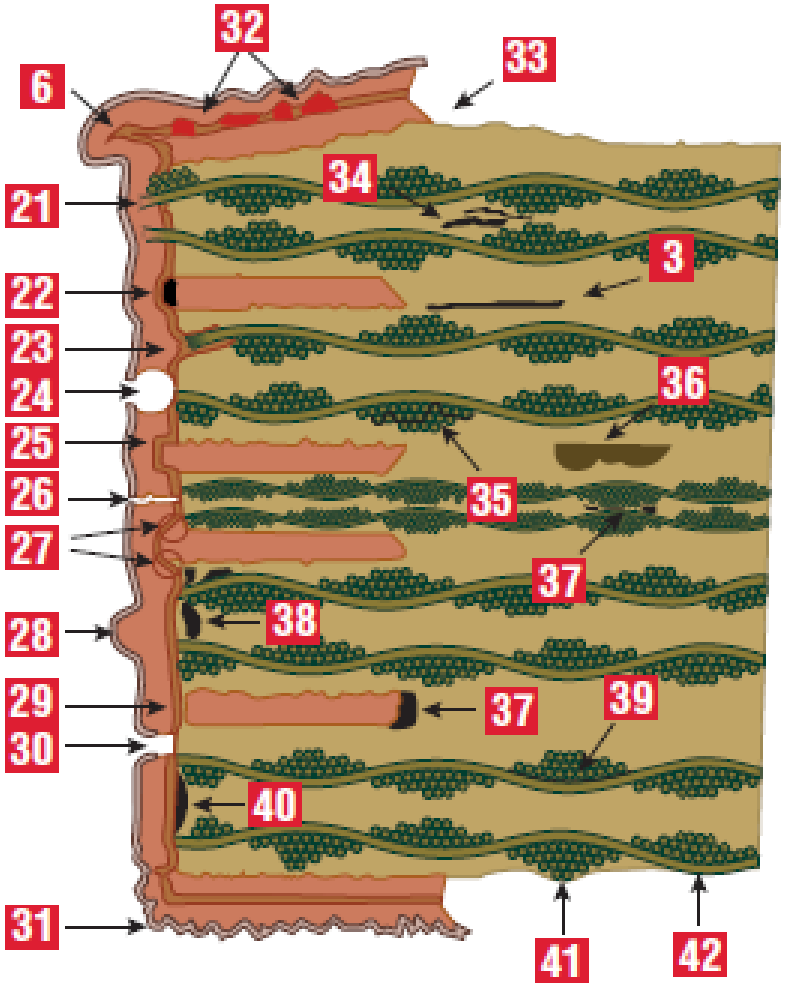
| Note ID | Descriptions | Comments |
|---|---|---|
| **RMp** | **Rigid Material Requirements – Prepreg Material** | |
| RMp1 | Laminate and prepreg shall be in accordance with IPC-4101/24. Refer to layer stack for copper foil weights. | |
| RMp2 | Laminate and Prepreg (B-stage) shall be in accordance with IPC-4101/23 or IPC-4101/24. Material must meet UL 94V-0 flammability rating. FR-406 material with a Tg of 170° or greater is recommended. | |
| RMp3 | Core FR-408, prepreg 1080 and prepreg 2116 shall be in accordance with IPC-4101. Minimum glass transition temperature (Tg) of 170°C required. See layer detail. | |
| RMp4 | Material shall be in accordance with IPC-4101/25, plastic sheet, type GF base material, glass base preimpregnated (B-stage), Tg rating: 140 to 160°C. | |
| RMp5 | Laminate and Prepreg (B-stage) to be in accordance with IPC-4101/23 or IPC-4101/24. Material must meet UL 94V-0 flammability rating. FR406 material with a Tg of 170° or greater is recommended. | |
| **RMr** | **Rigid Material Requirements – Reinforcement Materials** | |
| RMr1 | Reinforcement next to board surface shall be woven E glass, style 1080 per IPC 4412. | |
| RMr2 | A minimum of two layers of reinforcement woven E glass material shall be provided between all copper layers. | |
| RMr3 | | |
| RMr4 | | |
| RMr5 | | |
| **RMc** | **Rigid Material Requirements – Copper Foil** | |
| RMc1 | Copper foil **shall** be in accordance with IPC-4562/x, Quality classification 3. | |
| RMc2 | If foil lamination is used, copper foil shall be in accordance with IPC-4562/3, Quality classification 3. | |
| RMc3 | Copper foil to be in accordance with IPC-4562. Unless otherwise specified, all copper weight for inner signal layers to be 18µm (0.5 oz). Inner plane layers to be 35 µm (1 oz.). For outer layers 53µm (1.5 oz). Copper weight is to be considered "finished". | |

# 2614-Hole Schedule Example

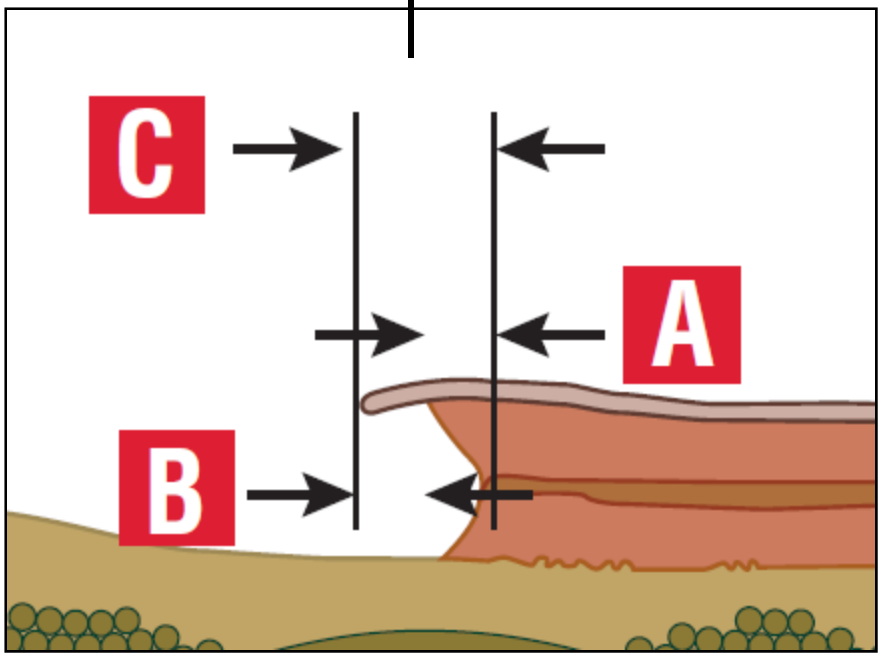
| Hole Schedule (All units are in millimeters) | | | | |
|---|---|---|---|---|
| **Symbol** | **Diameter** | **Quantity** | **Plating** | **Design Diameter** |
| A | 3.68 – 3.50 | 10 | Non - Plated | 3.70 |
| B | 3.18 – 3.00 | 3 | Non – Plated | 3.25 |
| C | 2.90 – 2.72 | 4 | Non – Plated | 2.95 |
| ◊ | 1.5 | 2 | Non - Plated | 1.55 |
| ● | 1.0 | 13 | Plated | 1.05 |
| ▶ | 0.9 | 31 | Plated | 0.95 |
| ▲ | 0.7 | 70 | Plated | 0.75 |
| □ | 0.6 | 244 | Plated | 0.65 |
| ▪ | 0.4 | 38 | Plated | 0.45 |
| ■ | 0.33 – 0.00 | 636 | Plated | 0.35 |
| Tolerance on diameter of single numbered holes are ± 0.05 | | | | |

# Hole Characteristic Descriptions

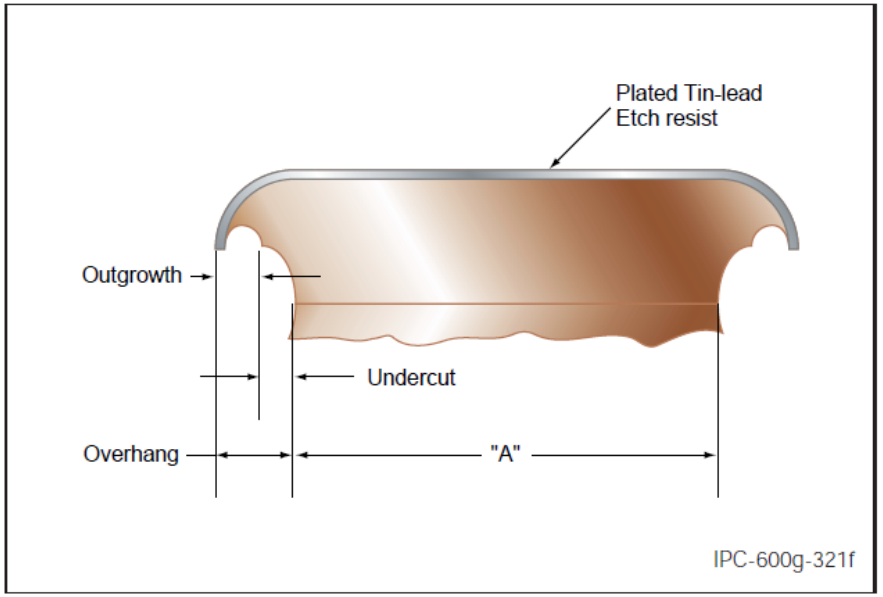


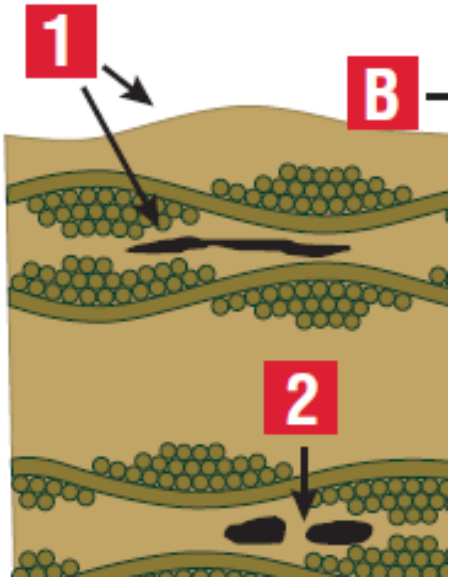



# You've got to know the Jargon



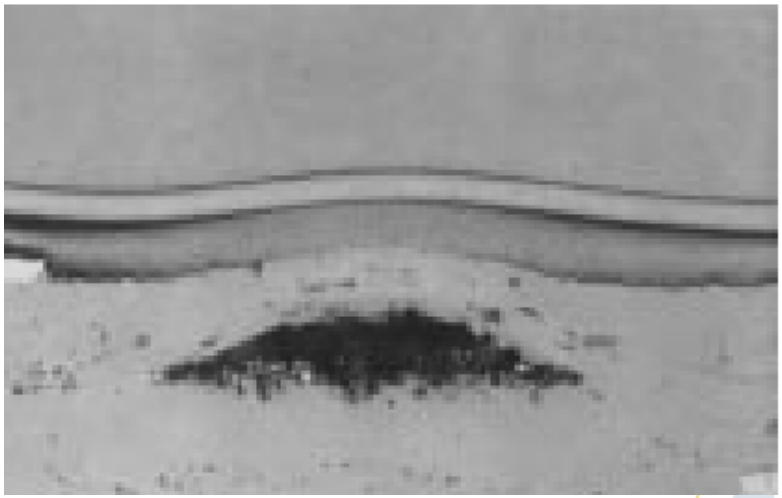

**A Undercut** – Add line to show where
**B Outgrowth** – Extend line to B
**C Overhang** - OK



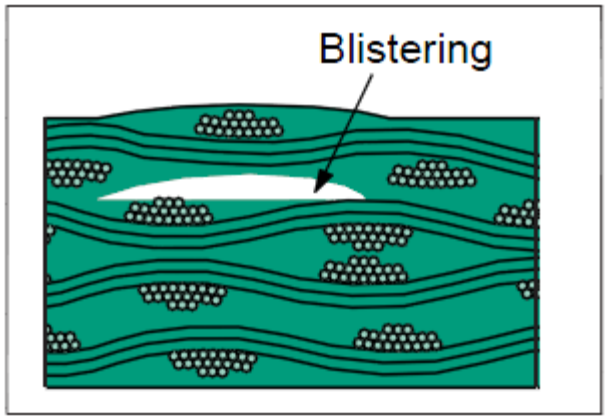


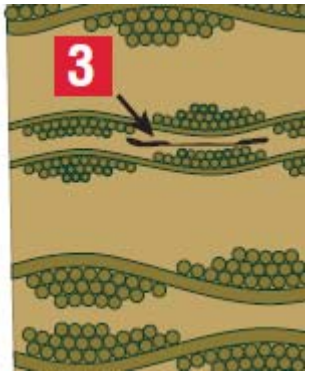

**1 (Resin) Blistering** – Remove second arrow and change the void color between layer 1 and 2 glass fiber. Reduce the resin above the glass underneath the bubble of raised resin. See sketch

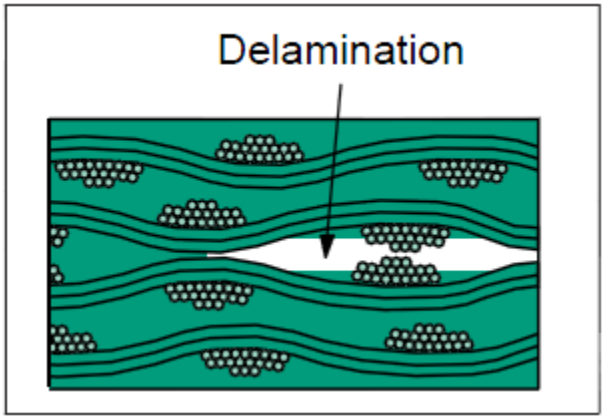
**2 Laminate Void** – OK no change



**Blister:** Delamination in the form of a localized swelling and separation between any of the layers of a lamination base material, or between base material and conductive foil or protective coating.

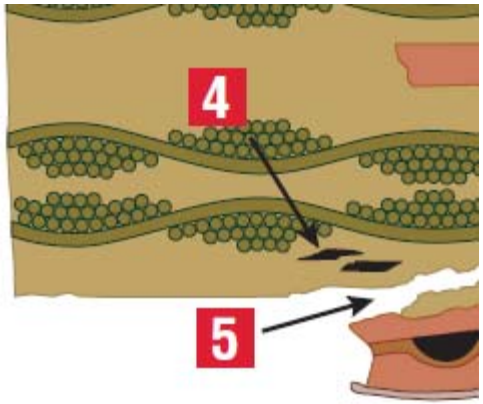





**Delamination:** A separation between plies within a base material, between a material and conductive foil, or any other planar separations within a printed board.

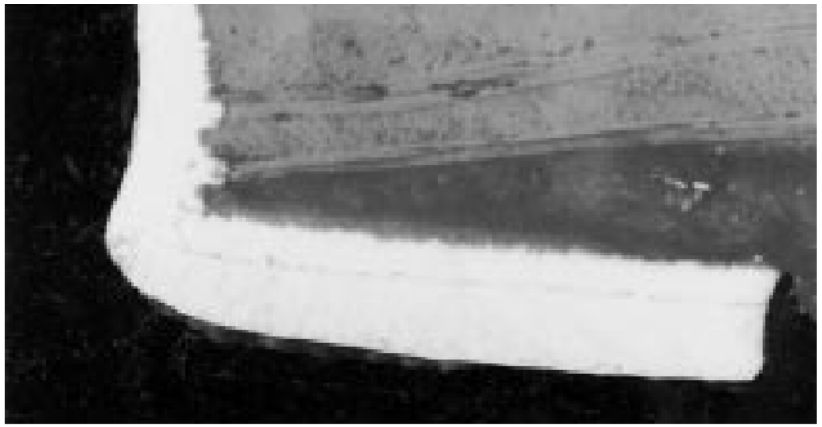
**3 (Resin) Delamination** – improve graphic see illustration

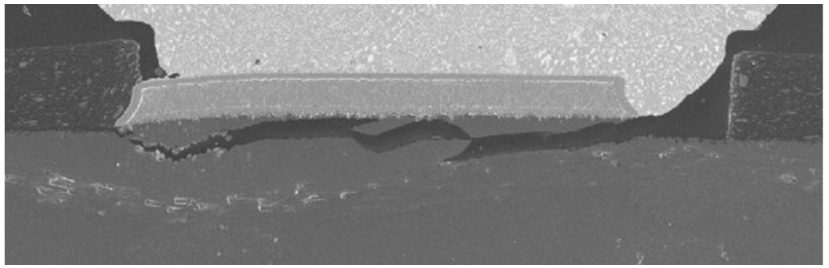



**4 Lifted Land Crack** - Remove 4 and resin void in picture. Add a land and make crater

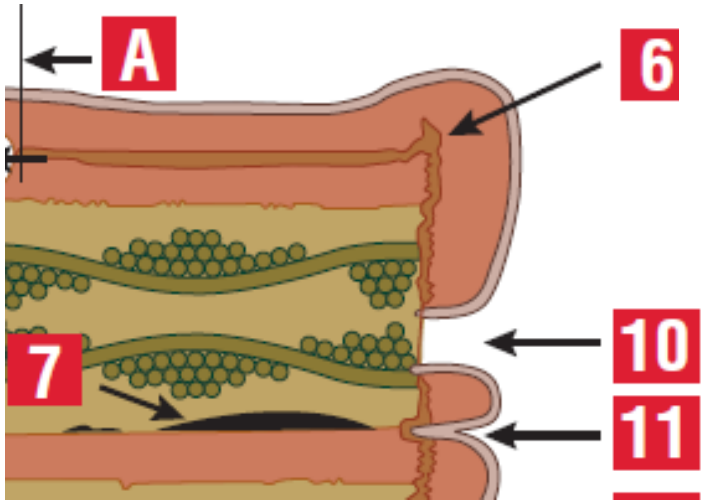
**5 Pad Lifting** change name to "Lifted Land Crack" the example shows the resin cracking

This is lifted land – no resin under land

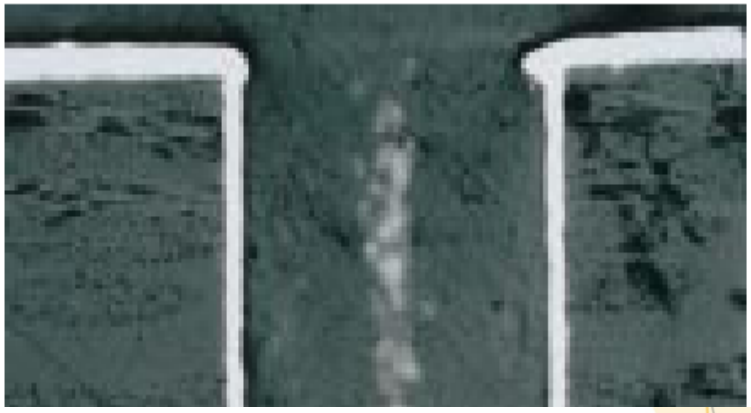




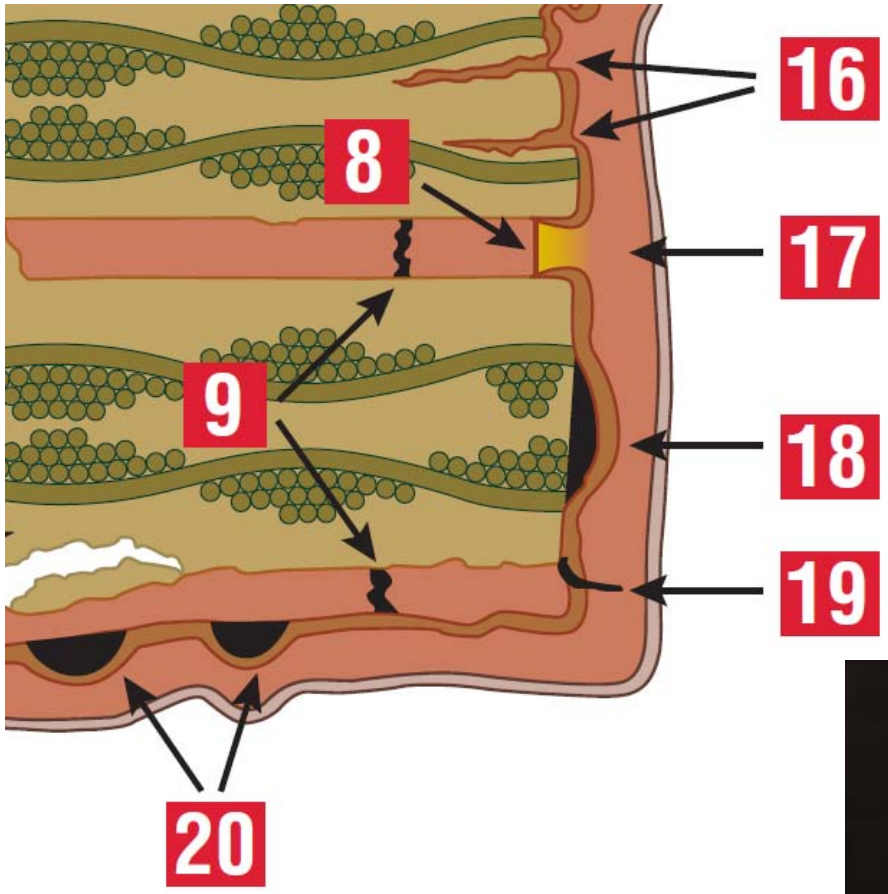
This is Pad Cratering. Usually at a land







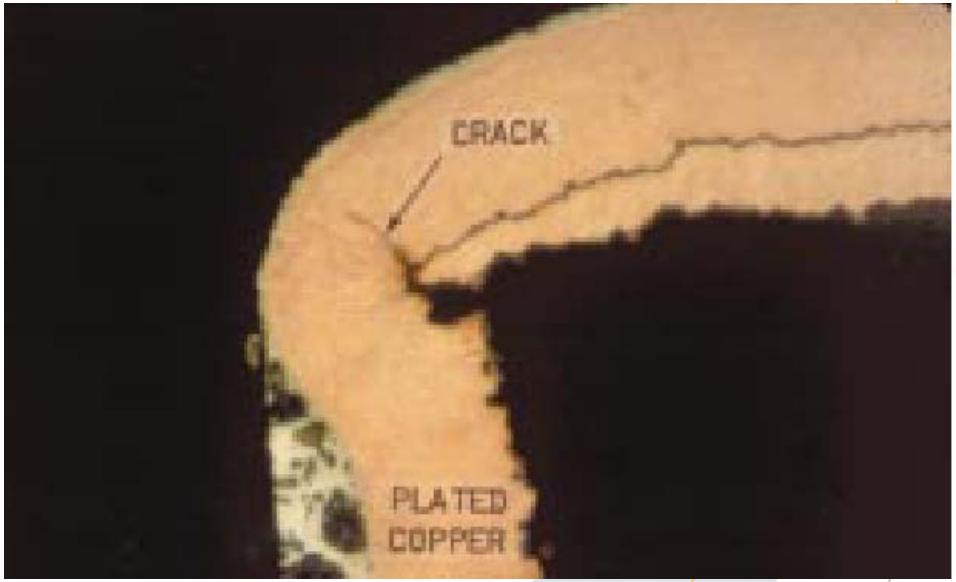
**6 Burr** on left is OK right is burr but not produced by drill should have different number. Burr was raised and the pushed into hole during scrubbing.
**7 Pink Rin**g –not pink ring laminate is not attached to copper – show Bond treatment removed by dark line on copper eliminated at far end. Re-title. Bond enhancement removed – “Pink Ring”

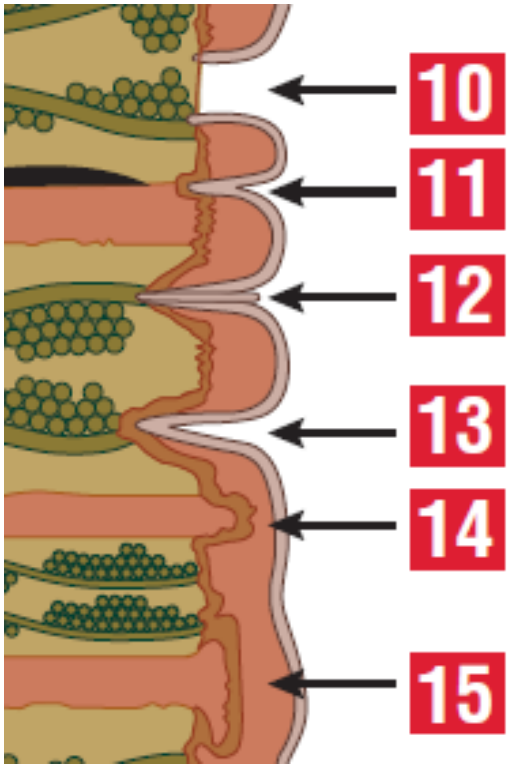



**8 Negative Etchback -** OK
**9 Foil Crack** – Cracks OK

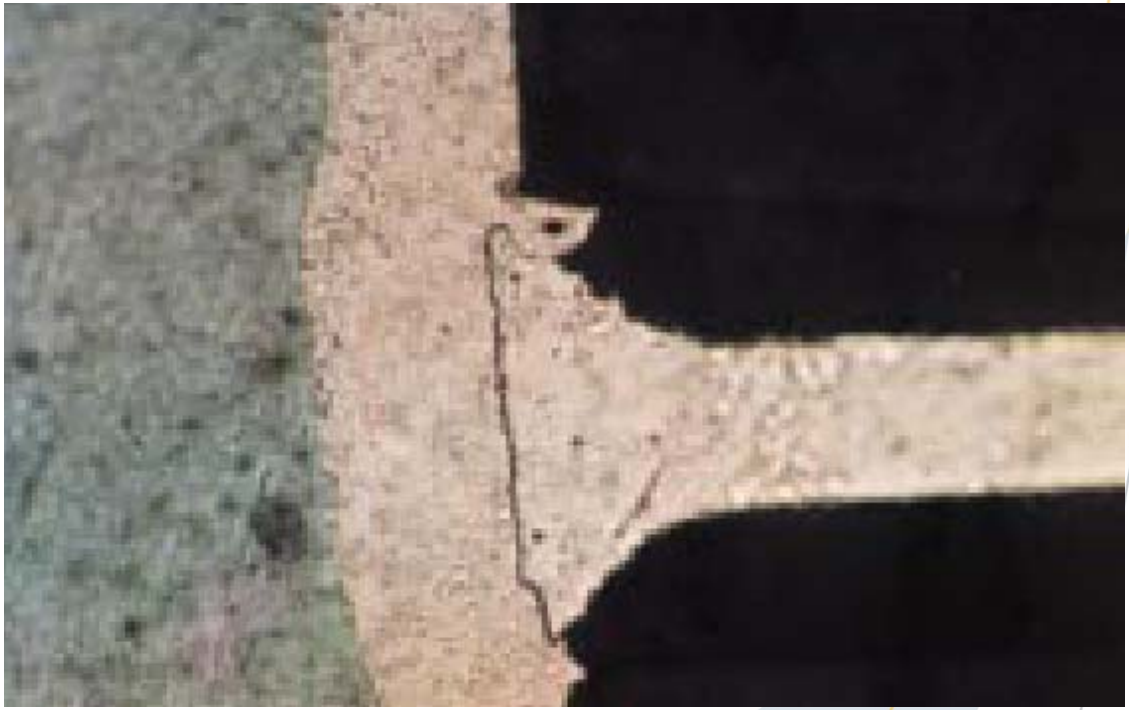
**16 Drilling Cracks** – change to "Drill Wall Tear"
**17 Innerlayer Burning (ICD)** – Remove or rename
**18 Hole Wall Pull Away** – OK
**19 Corner Crack** – Move crack to corner
**20 Blistering** – change to Copper Plating Blisters

***Corner Crack***

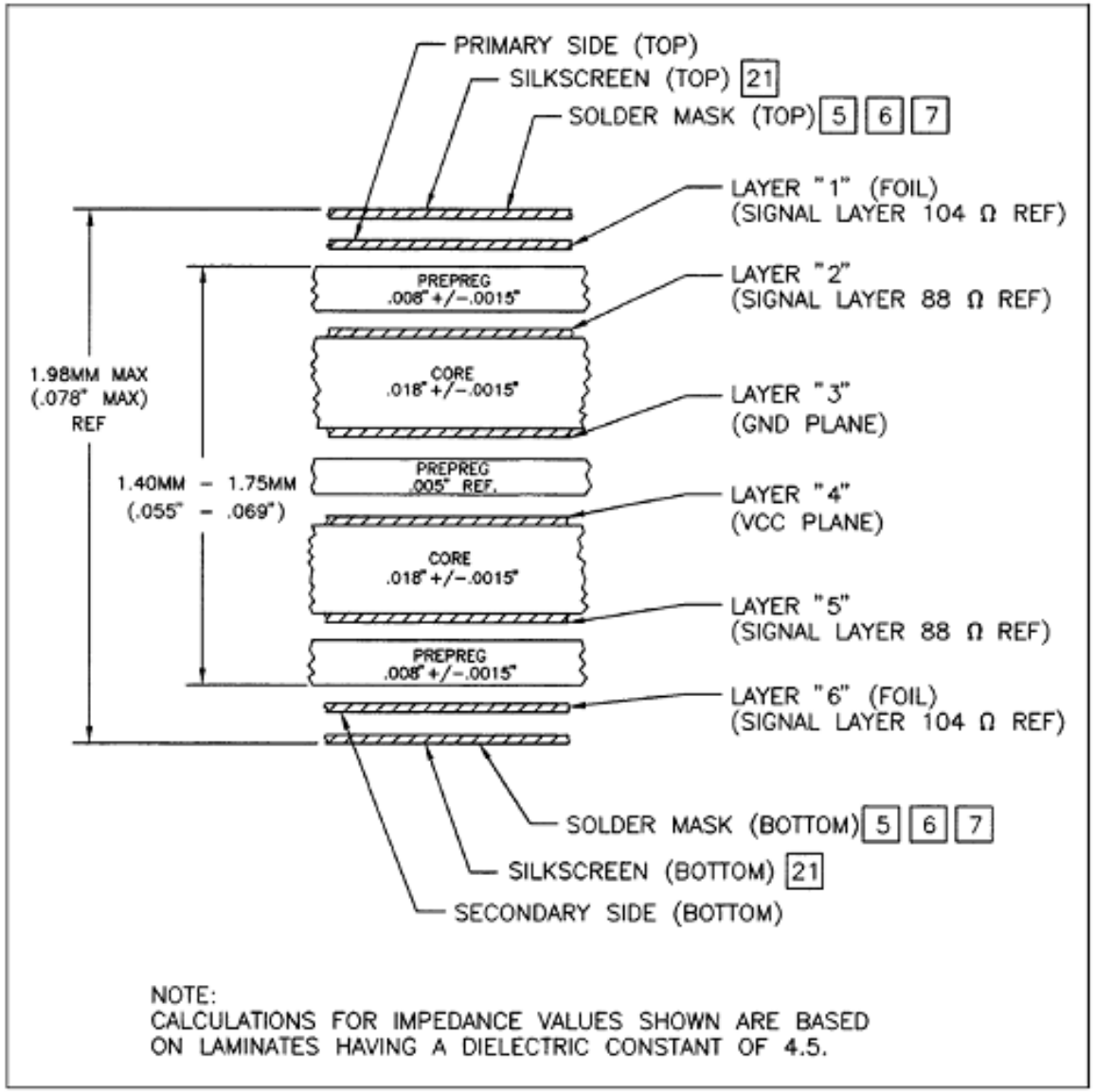




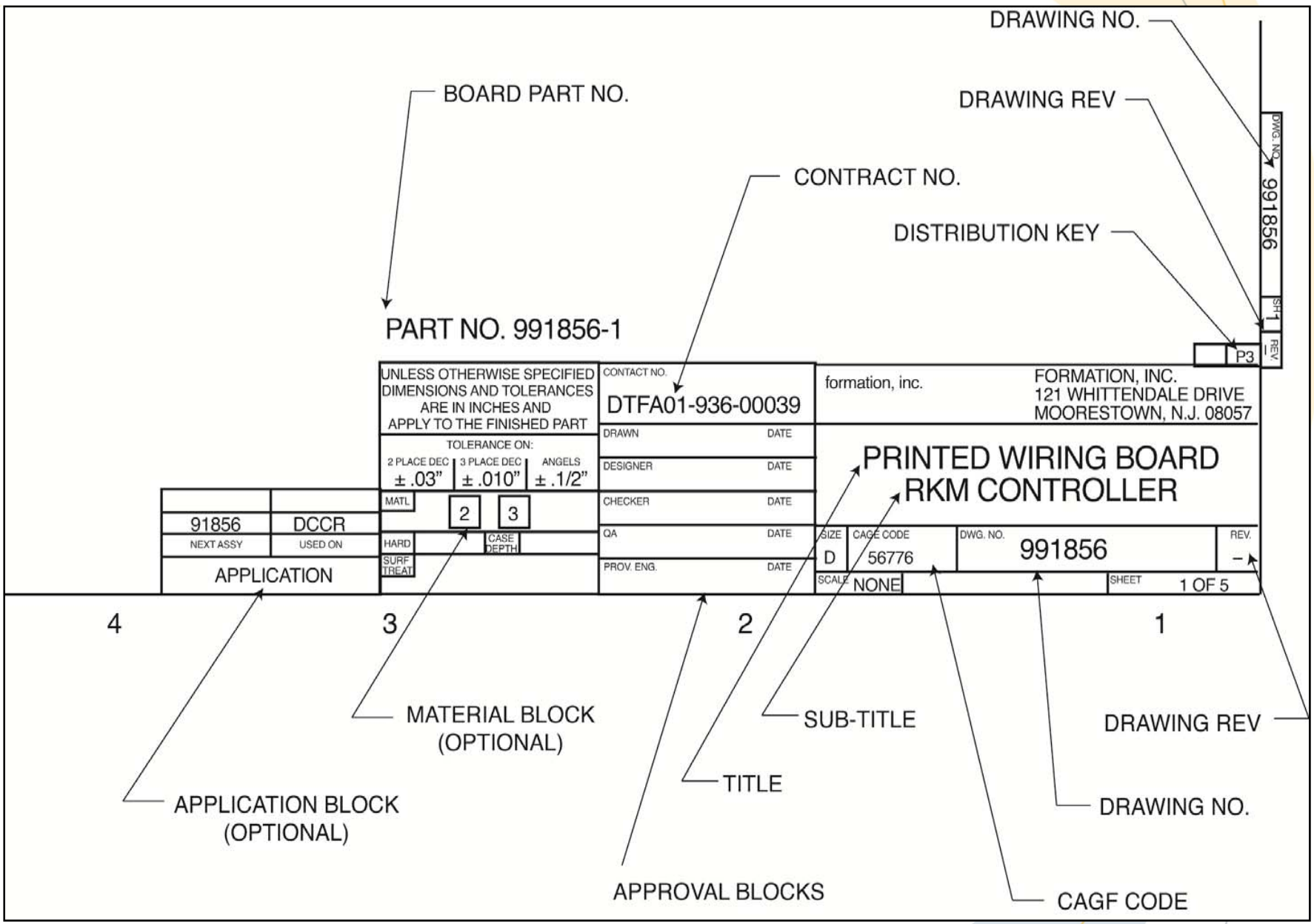

**10 Void (PTH)** – to “Hole Plating Void”
**11 Wedge Void** –to “Plating Nodule”
**12 Glass Void** –to “Glass Fiber Void”
**13 Microvoid (Glass)** – change to “Glass Bundle Void”
**14 Arrow Heading** – change to “Severe Etchback”
**15 Nail Heading** - OK



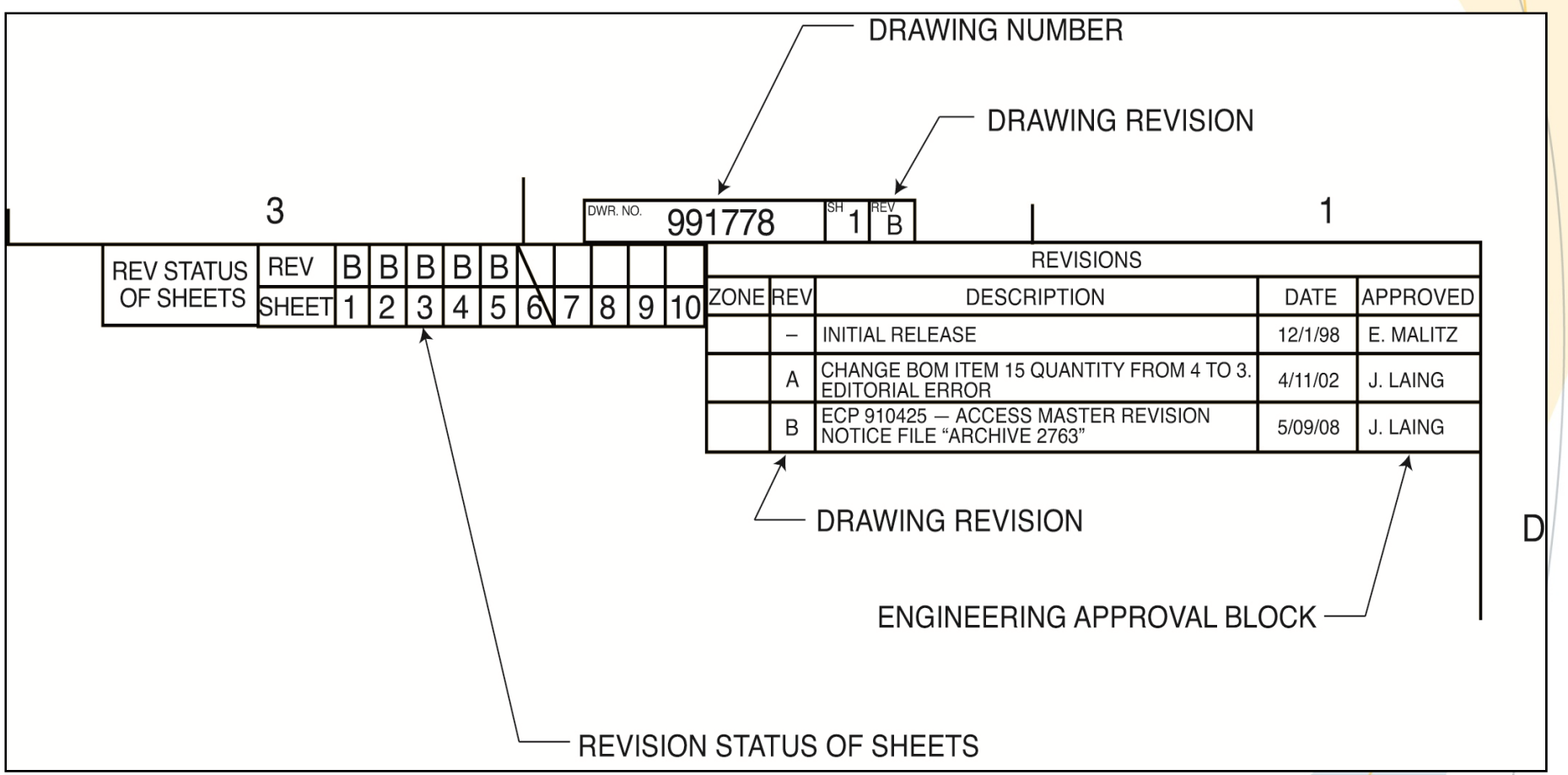
# Cross Section Example



# Title Block


DRAWING NO.
BOARD PART NO.
DRAWING REV
CONTRACT NO.
DISTRIBUTION KEY
PART NO. 991856-1
DWG. NO. 991856
SH 1
REV. –
P3
UNLESS OTHERWISE SPECIFIED DIMENSIONS AND TOLERANCES ARE IN INCHES AND APPLY TO THE FINISHED PART
TOLERANCE ON:
2 PLACE DEC ± .03"
3 PLACE DEC ± .010"
ANGELS ± .1/2"
CONTACT NO.
DTFA01-936-00039
DRAWN DATE
DESIGNER DATE
CHECKER DATE
QA DATE
PROV. ENG. DATE
formation, inc.
FORMATION, INC.
121 WHITTENDALE DRIVE
MOORESTOWN, N.J. 08057
PRINTED WIRING BOARD
RKM CONTROLLER
MATL
2
3
HARD
CASE DEPTH
SURF TREAT
91856
NEXT ASSY
DCCR
USED ON
APPLICATION
SIZE D
CAGE CODE 56776
DWG. NO. 991856
REV. –
SCALE NONE
SHEET 1 OF 5
4
3
2
1
APPLICATION BLOCK (OPTIONAL)
MATERIAL BLOCK (OPTIONAL)
APPROVAL BLOCKS
TITLE
SUB-TITLE
DRAWING REV
DRAWING NO.
CAGF CODE

# Revision Information



# 2611-Revision Identification

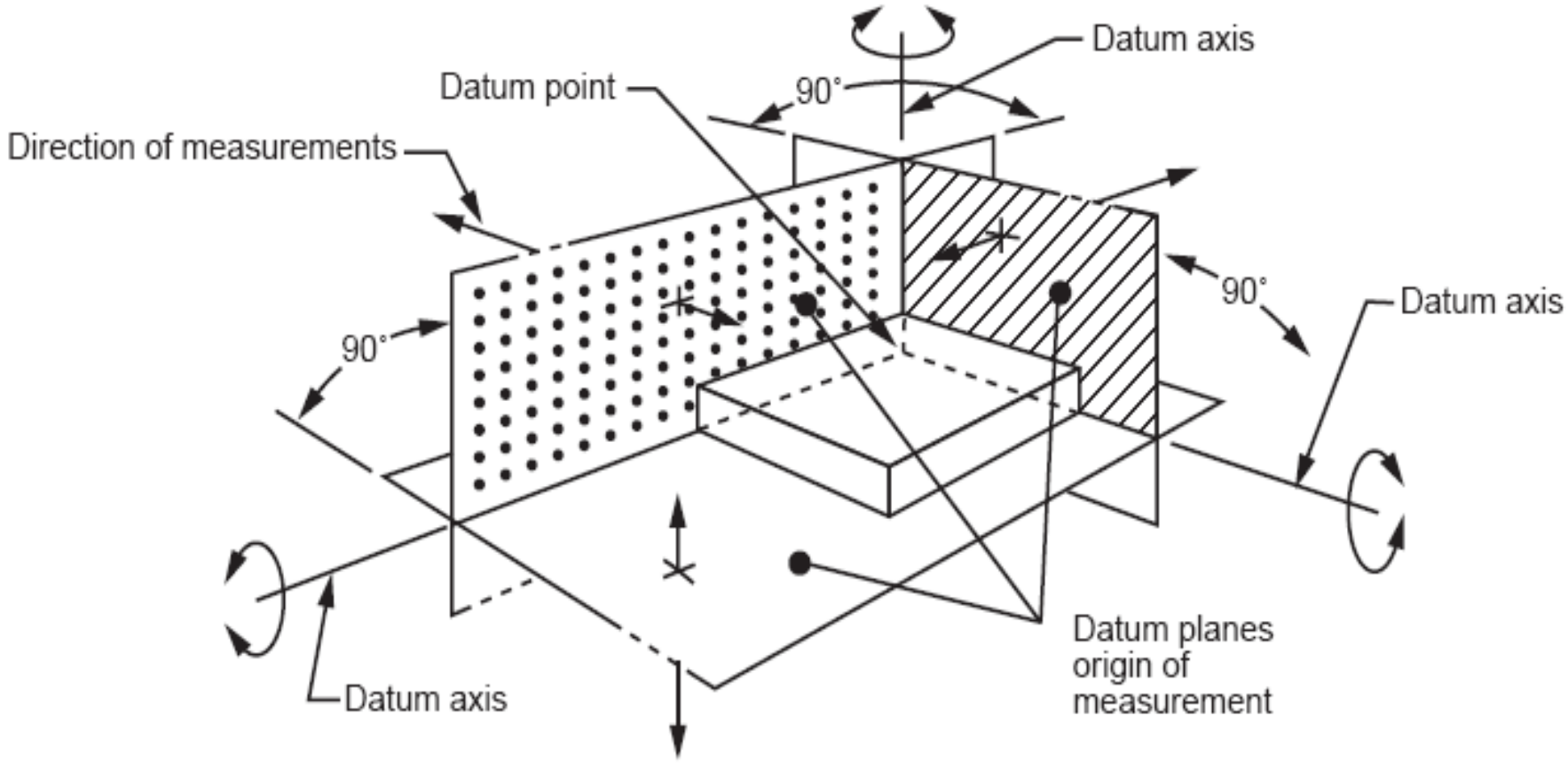
Quite often it becomes necessary to release hard copy or electronic documentation as well as data files in a preliminary or prototype state. Since it is desirable to maintain revision level control during this stage, either of the following methods is suggested (see Table 3-1).
Method #1  This method starts out with:
Proto Release number 1 uses Revision “+A” for the first release;
Proto Release number 2 uses Revision “+B” for the second release;
Proto Release number 3 uses Revision “+C” for the third release, etc.

Method #2  This method is very similar to method number#1, except this method starts out with:
Proto Release number 1 uses Revision 1 for the first release;
Proto Release number 2 uses Revision 2 for the second release;
Proto Release number 3 uses Revision 3 for the third release, etc.

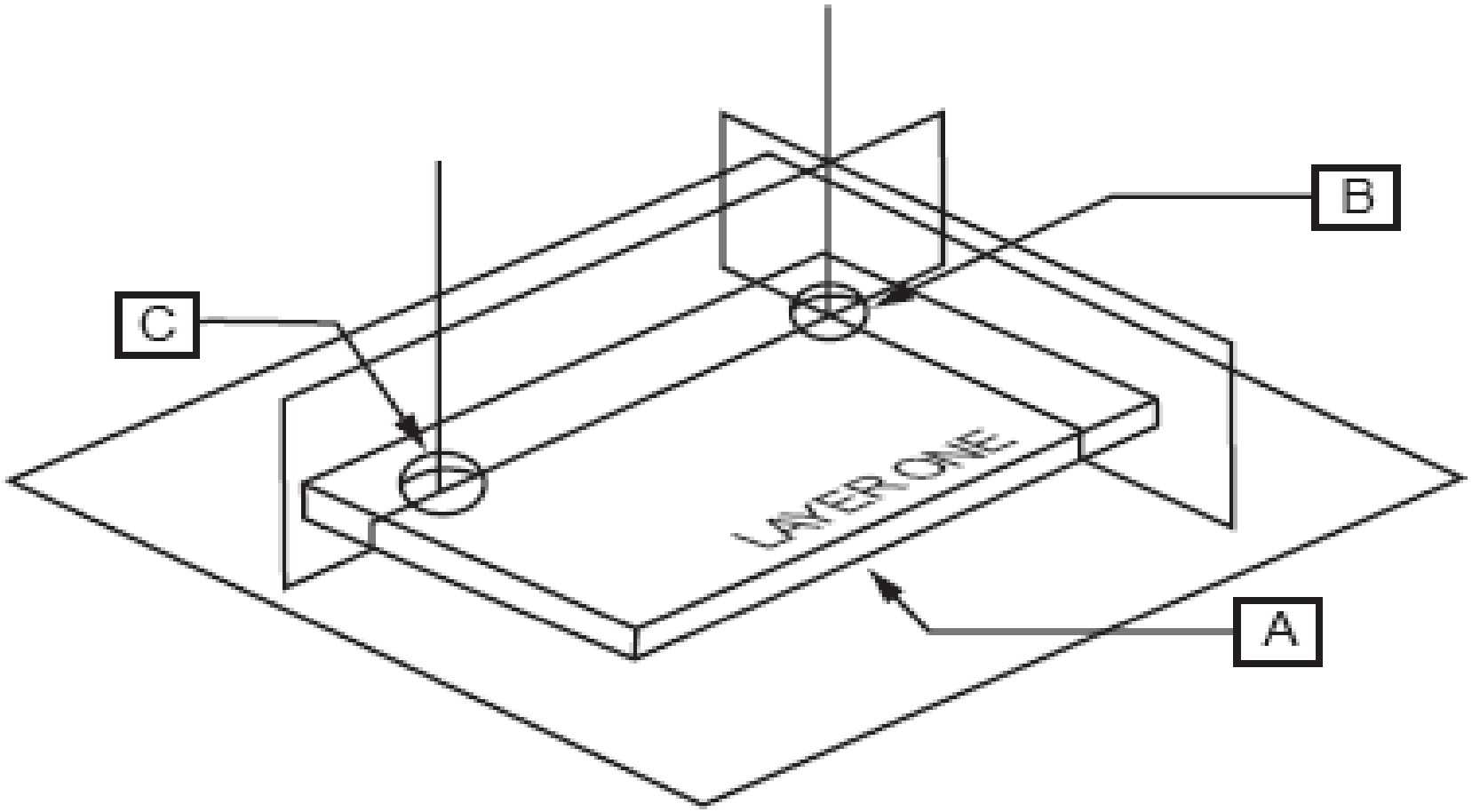
# Detail Requirements

Verification of compatibility with specifications, master drawings and patterns, and the specific manufacturing facilities and processes used, are the responsibility of the supplier. The printed board procurement documentation **shall** be prepared in accordance with the applicable design specifications. The supplier **shall** ensure that the end-product board meets the requirements of the printed board procurement documentation.

# Datum Reference Frame to Printed Board Relationship



# Datum Reference Frame to Printed Board Relationship

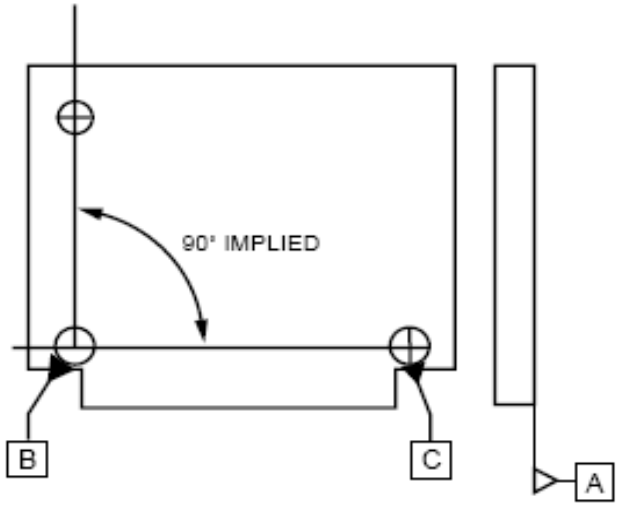



IPC-2615

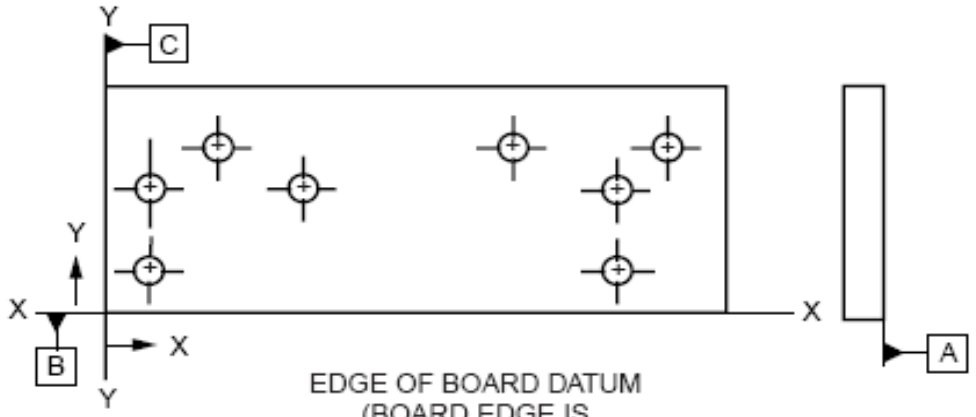
# Minimum Requirements for Master Drawing

Features of the board are used to locate the datum planes. The backside of the board is the feature that establishes the primary plane. Secondary and tertiary planes can established using holes, symbols, or fiducials or board edges. It is preferred to use the features critical to mounting the board in its final package to establish datum planes.

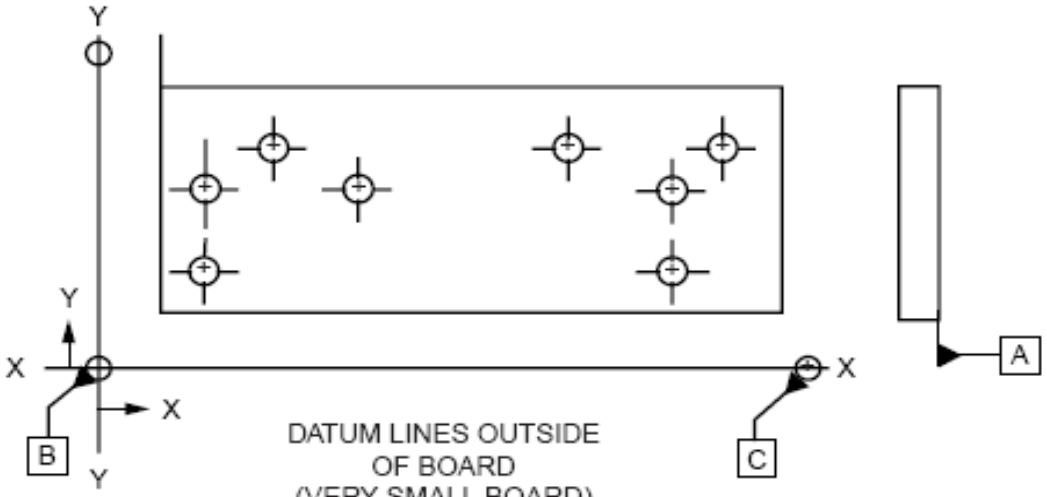
# Datum Identification Examples




DATUM LINES WITHIN BOARD
(MOUNTING HOLES MAY BE USED)




EDGE OF BOARD DATUM
(BOARD EDGE IS
CRITICAL TO MOUNTING)




DATUM LINES OUTSIDE
OF BOARD
(VERY SMALL BOARD)

# Relationship 2610 to 2580

As an example when defining fabrication information the relationship between the IPC-2614 and the IPC-2584 provides the mechanism for description/data between design and manufacturing. Both generic standards use the concepts of table 3-1 to define the information needs.

| Name | Fabrication | | | Comment and Standard Reference |
|---|---|---|---|---|
| | 1 | 2 | 3 | |
| Component Packages * | - | - | O | Elements indicated in this sectional standard, according to cardinality of IPC-2581 and any restrictions contained in the following paragraphs of this standard<br><br>*Although Component Packages and Land Patterns are further defined in IPC-2586, and Net Lists are further defined in IPC-2587, their XML schemas are repeated in this standard. |
| Land Patterns * | - | - | O | |
| Solder mask, Legend Layers | M | M | M | |
| Drilling and Routing (Tooling) Layers | M | M | M | |
| Net List (Soft tooling) * | O | M | M | |
| Outer Conductive Layers | M | M | M | |
| Inner Conductive Layers | M | M | M | |
| Board Construction | M | M | M | |

| Standard Hierarchy | | | |
|---|---|---|---|
| ***CAD-CAM Format IPC-2580 Series*** | ***General Description*** | | ***Documentation IPC-2610 Series*** |
| **IPC-2581** | *Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology* | *Generic Requirements for Electronic Product Documentation* | **IPC-2611** |
| **IPC-2582** | *Implementation of Administrative Methods for Manufacturing Data Description* | *Electronic Diagramming Documentation* (Schematic and Logic Descriptions) | **IPC-2612**<br>**IPC-2612-1** |
| **IPC-2583** | *Implementation of Design Characteristics for Manufacturing Data Description* | *Electrical, Mechanical and Discrete Wiring Part Descriptions Documentation* | *IPC-2613* |
| **IPC-2584** | *Implementation of Printed Board Fabrication Data Description* | *Board Fabrication Documentation* | **IPC-2614** |
| *IPC-2585* | | *Printed Board Dimensions and Tolerances* | **IPC-2615** |
| **IPC-2586** | *Implementation of Printed Board Assembly Products Manufacturing Data Description* | *Assembly Documentation* | **IPC-2616** |
| **IPC-2587** | *Implementation of Printed Board and Assembly Testing* | *Board and Assembly Testing* (Electrical and Environmental test) | **IPC-2617** |
| **IPC-2588** | *Implementation of Part List Product Data Description* | *Bill of Material Documentation* | **IPC-2618** |

# Data Transfer Series IPC-2580

***IPC-2581*** - Generic Requirements for Printed Board Assembly Products Manufacturing Description Data & Transfer Methodology

***IPC-2582*** - Sectional Requirements for Implementation of Administrative Methods for Manufacturing Data Description

***IPC-2583*** - Sectional Requirements for Implementation of Design Characteristics for Manufacturing Data Description

***IPC-2584*** - Sectional Requirements for Implementation of Printed Board Fabrication Data Description

***IPC-2585*** - Sectional Requirements for (Un-assigned )

***IPC-2586*** - Sectional Requirements for Implementation of Assembly Data Description

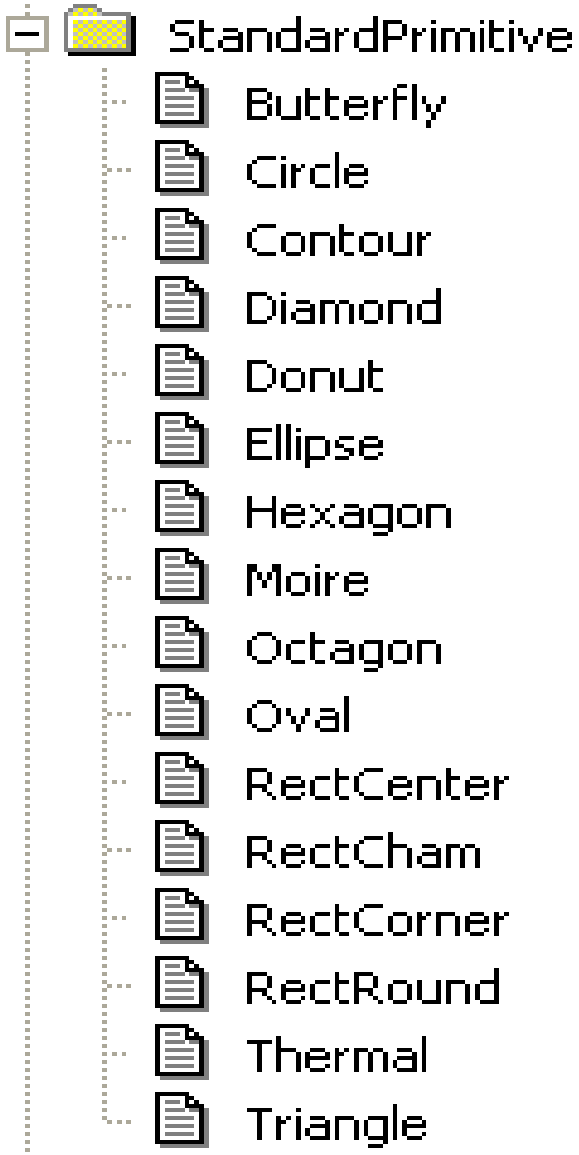
**IPC-2587**- Sectional Requirements for Implementation of Board and Assembly Testing Data description

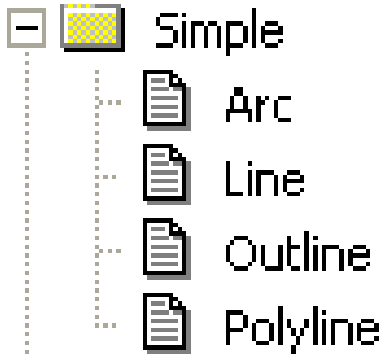
***IPC-2588*** -Sectional Requirements for Implementation of Part List Product Data Description

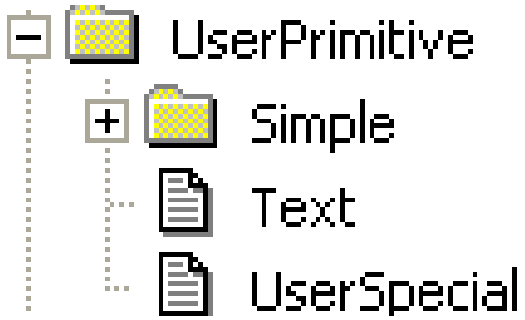
# Electronic Data Transfer IPC-2581

- Data extraction from CAD
- CAM step and repeat plus process tolerance inclusion
- Design file review (Pad Stacks) versus layered data
- Assembly information tied to CAD libraries
- Provide updated viewer to industry
- Provide Gerber to 2581 converter

# Standard and User Dictionaries




**All Dictionary elements are Substitution Groups**

# XML Example

```
<ROUTES>
 <GROUP11 route_group_id="route1" >
  <ROUTE net_name="CPU_PAGE_12_U23_3" net_class="SIGNAL" >
   <PATH layers_ref="lay1:1" linedesc_ref="prim4:signalwidth" >
    <POLYLINE >
     <STARTAT4 start_xy="(1200,1420)" />
     <LINETO4 end_xy="(1200,1600)" />
     <LINETO4 end_xy="(1320,1600)" />
     <LINETO4 end_xy="(1320,1815)" />
     <LINETO4 end_xy="(1460,1815)" />
    </POLYLINE>
   </PATH>
   <VIA via_name="TV1" padstack_ref="pad1:100Chips"
       access_desc="NOPROBE" xy_ref="(1460,1815)" />
  </ROUTE>
  <ROUTE net_name="C3" net_class="CLK" >
   <PATH layers_ref="lay1:1" linedesc_ref="prim4:signalwidth" >
    <POLYLINE >
     <STARTAT4 start_xy="(1300,1400)" />
     <LINETO4 end_xy="(1200,2200)" />
    </POLYLINE>
   </PATH>
   <TESTPAD testpad_name="p106_2" padstack_ref="pad1:100Chips"
         access_desc="NOPROBE" xy_ref="(1200,2200)" />
</ROUTES>
```

# XML is Human Readable

```
<EntryStandard id = "Diamond1">
      <Diamond width = "10.40" height = "6.20"/>
</EntryStandard>

<EntryStandard id = "Diamond2">
      <Diamond width = "6.00" height = "8.60"/>
</EntryStandard>

<EntryStandard id = "Donut1">
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</EntryStandard>

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</EntryStandard>

<EntryStandard id = "Donut3">
     <Donut shape = "SQUARE" outerDiameter = "6.8" innerDiameter = "5.0"/>
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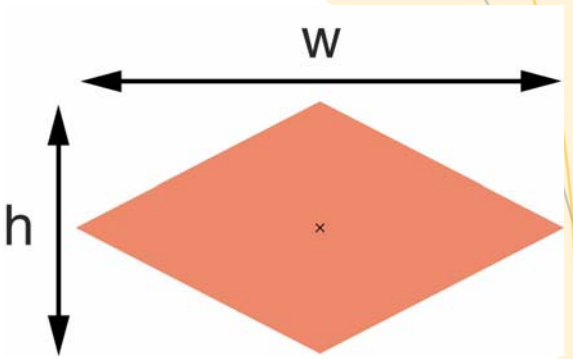
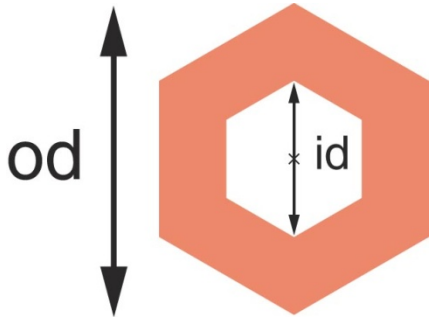
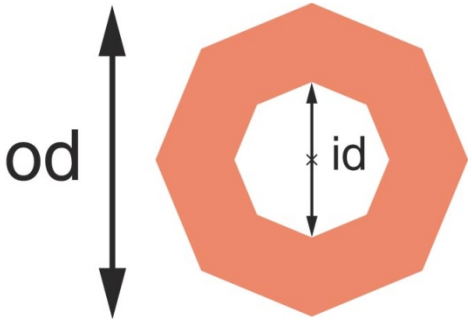
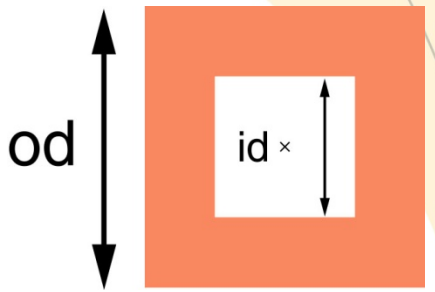
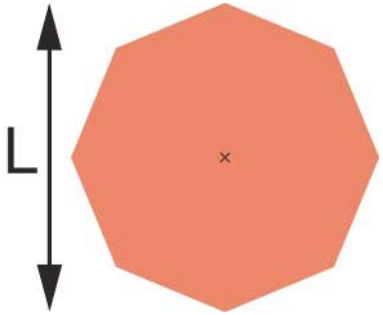


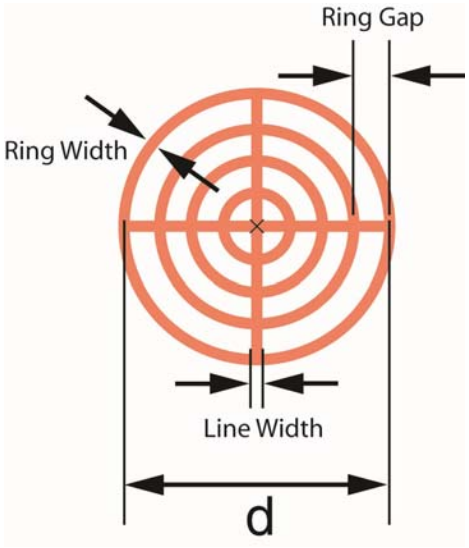
# Other Standard Primitives

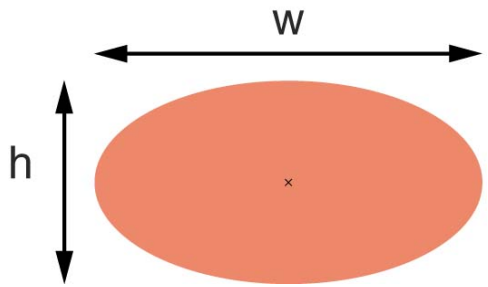


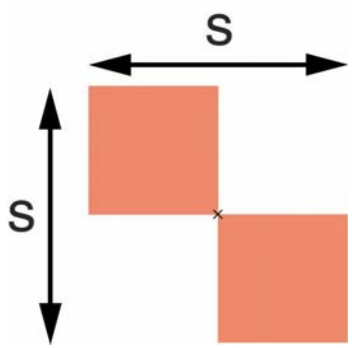



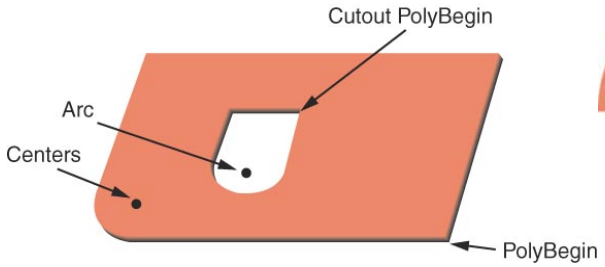



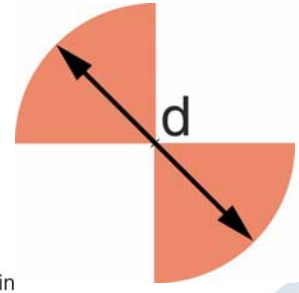



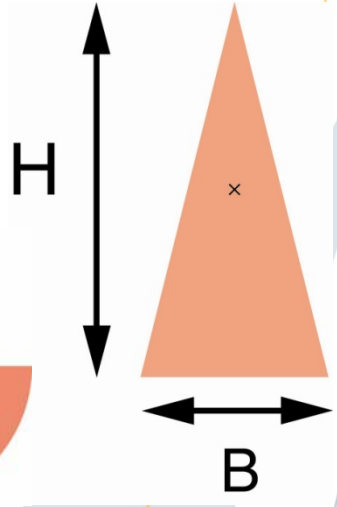



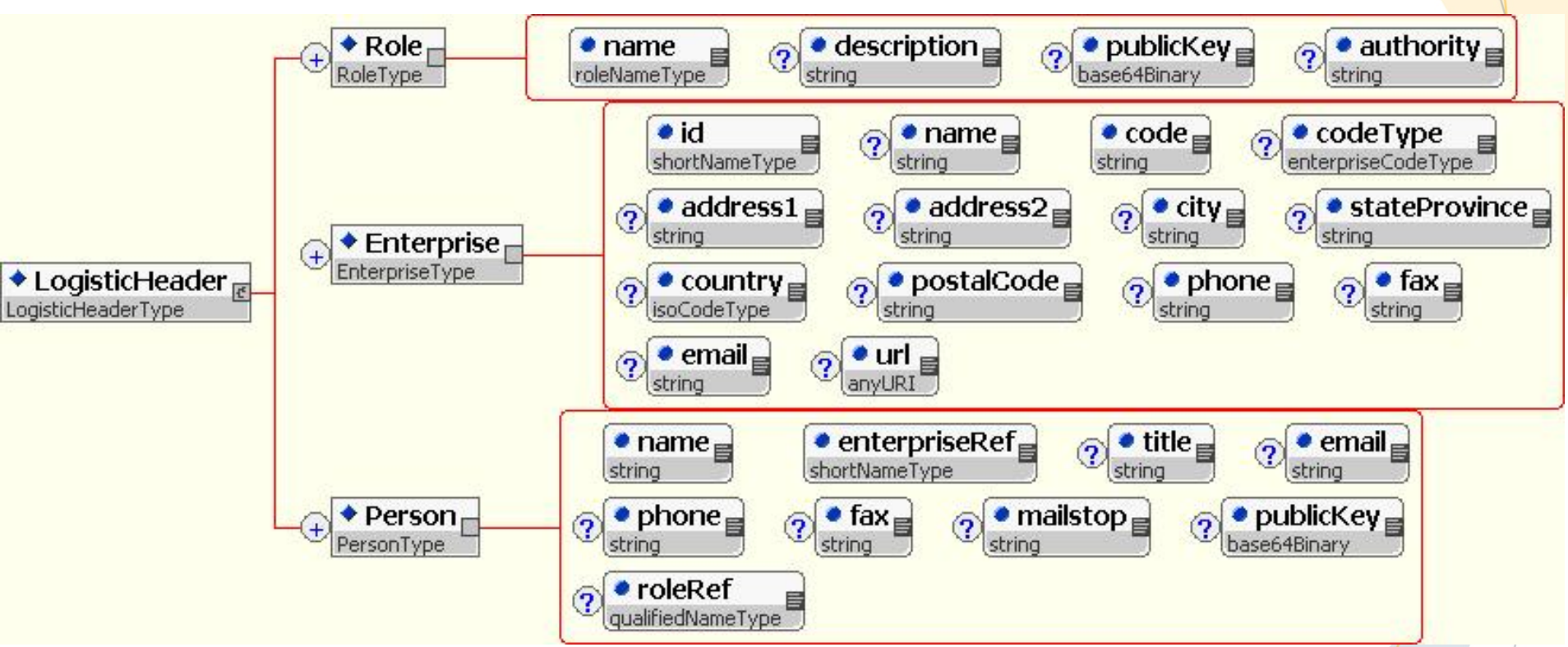



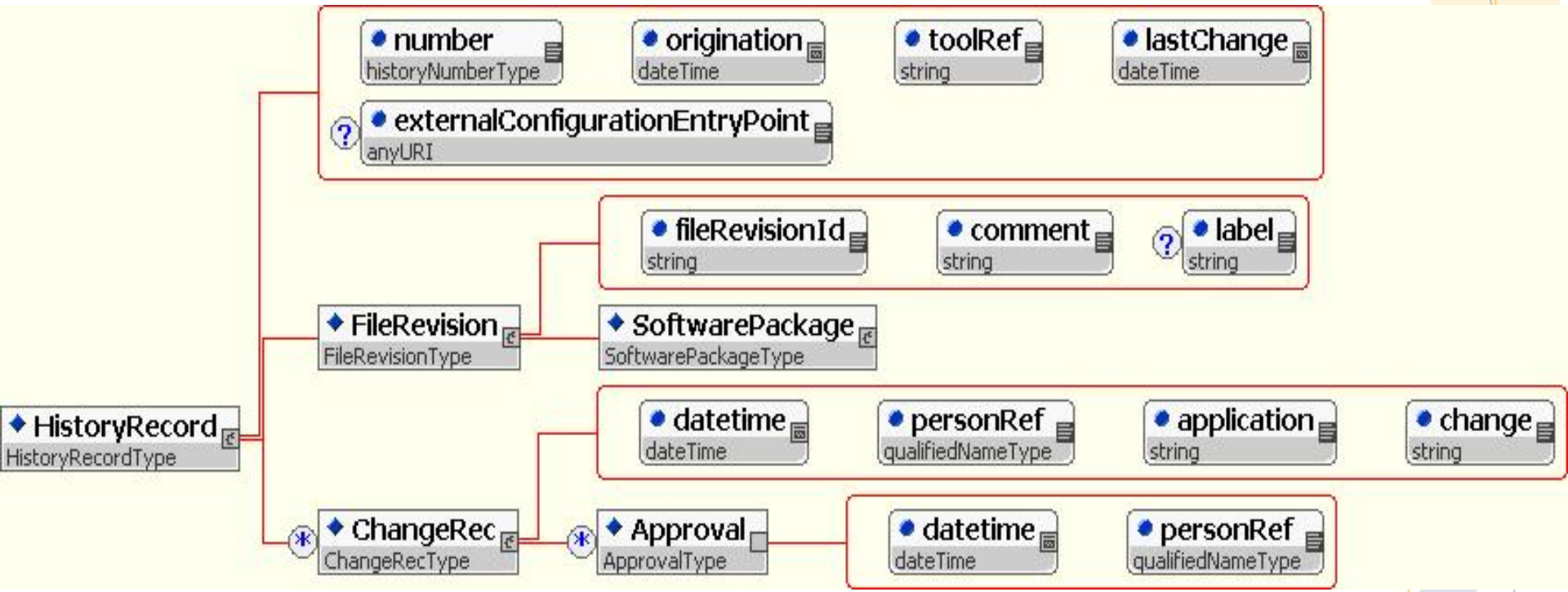



# Logistic Header



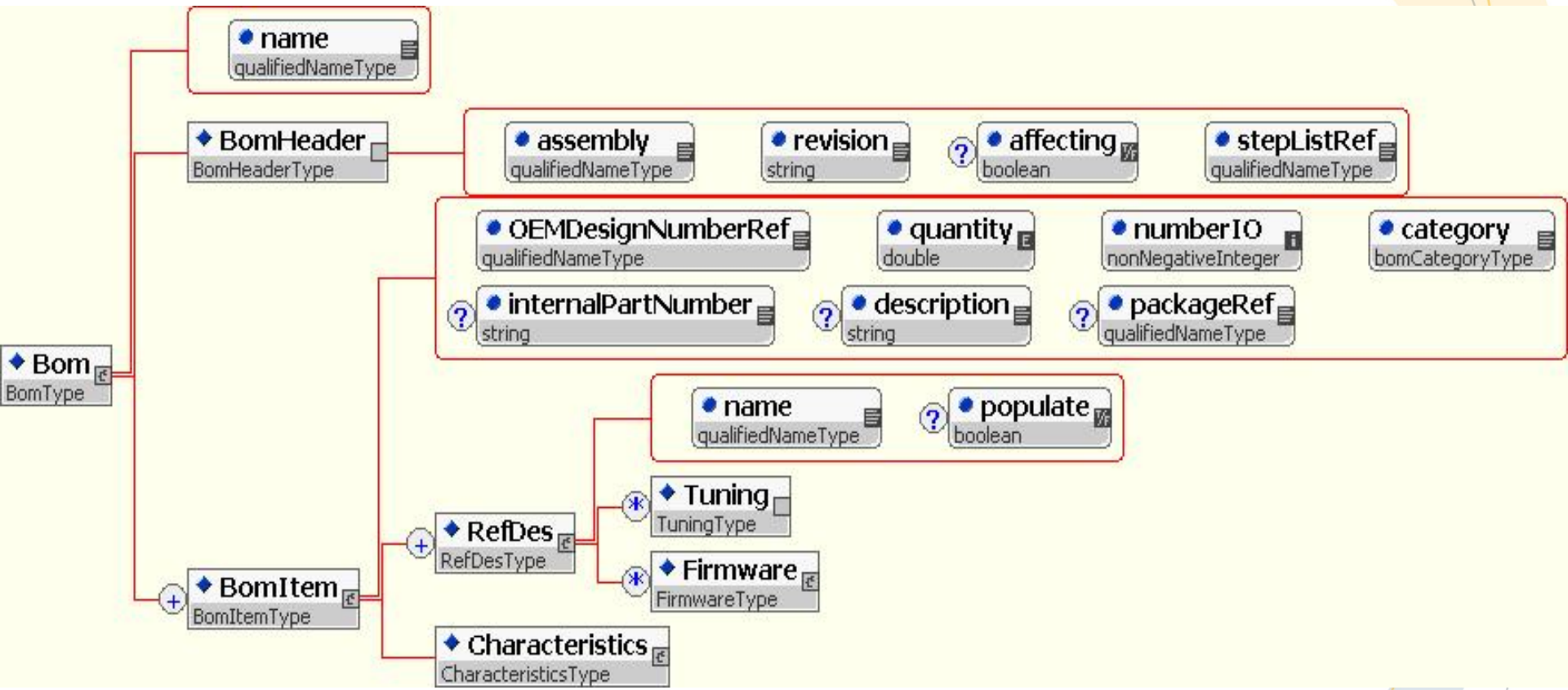

**Indicates file owner as well as Approved Vendors**

# History Record



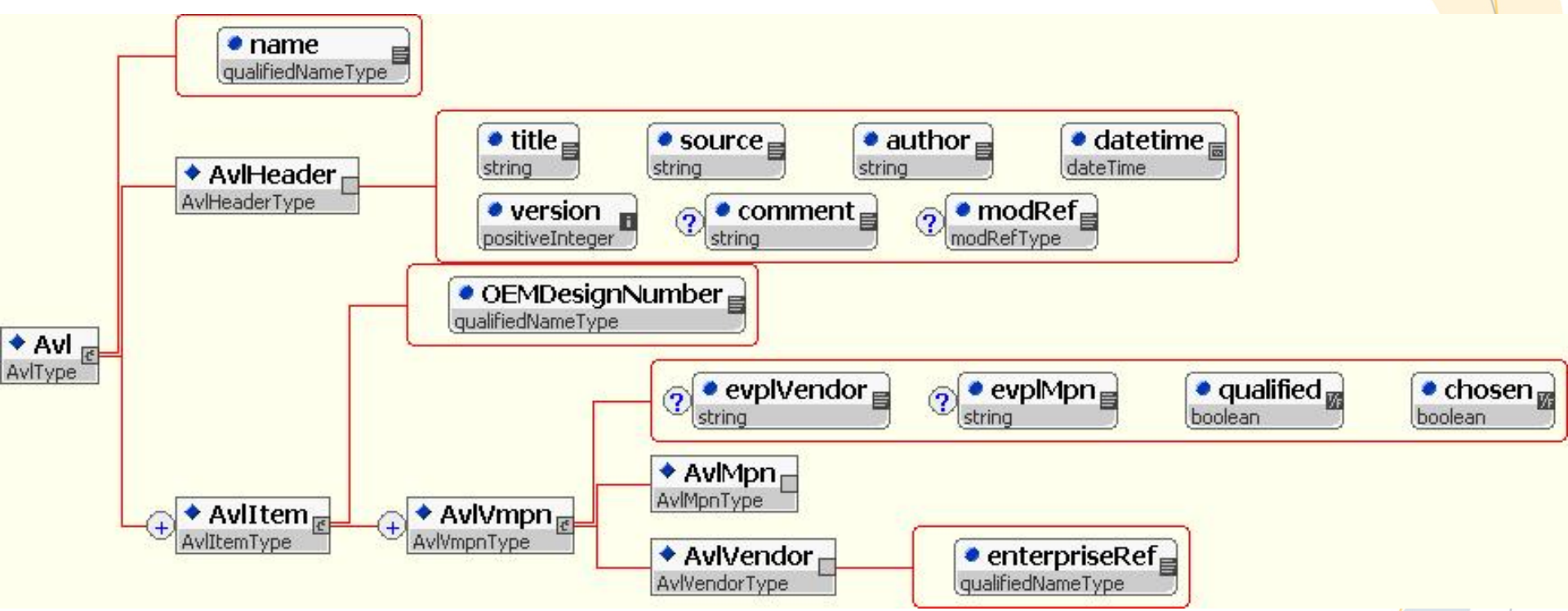

## Configuration Management Section

# Bill of Materials



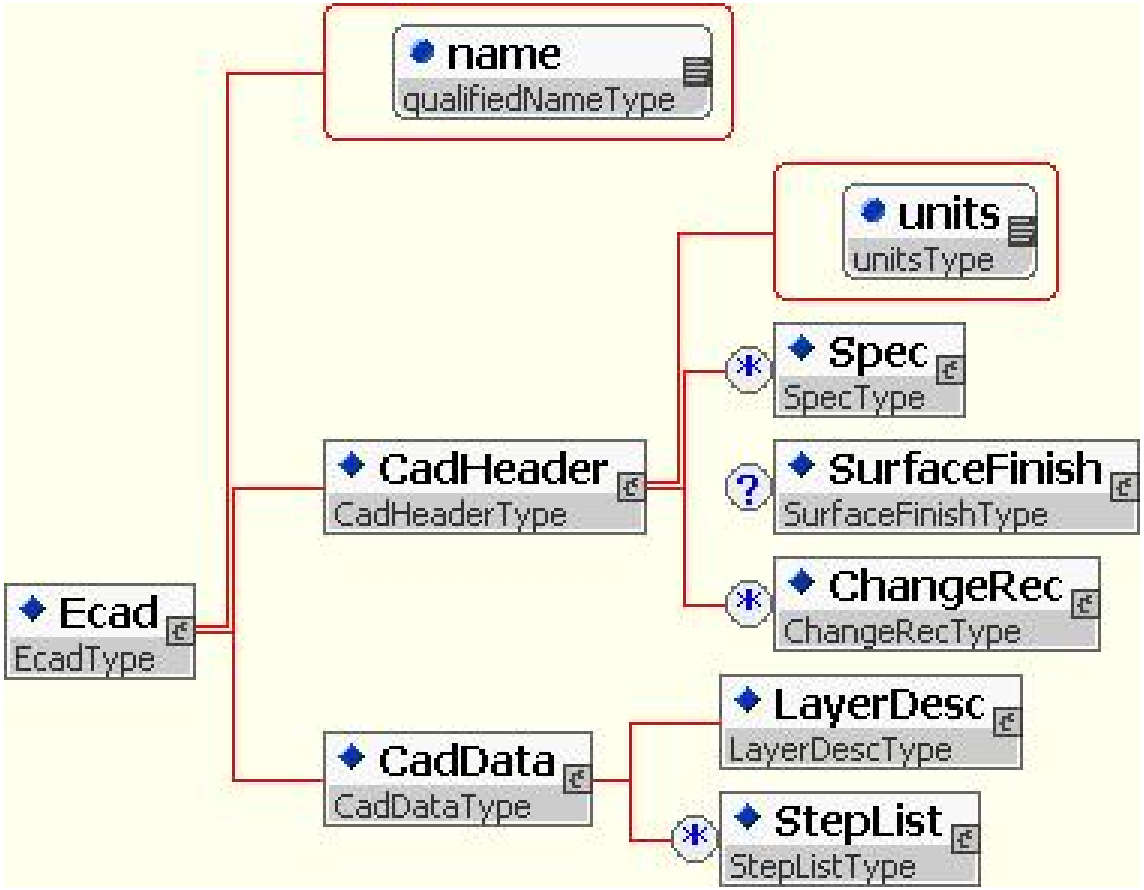

**One to many BOMs including one for Board Material**

# Approved Vendor List

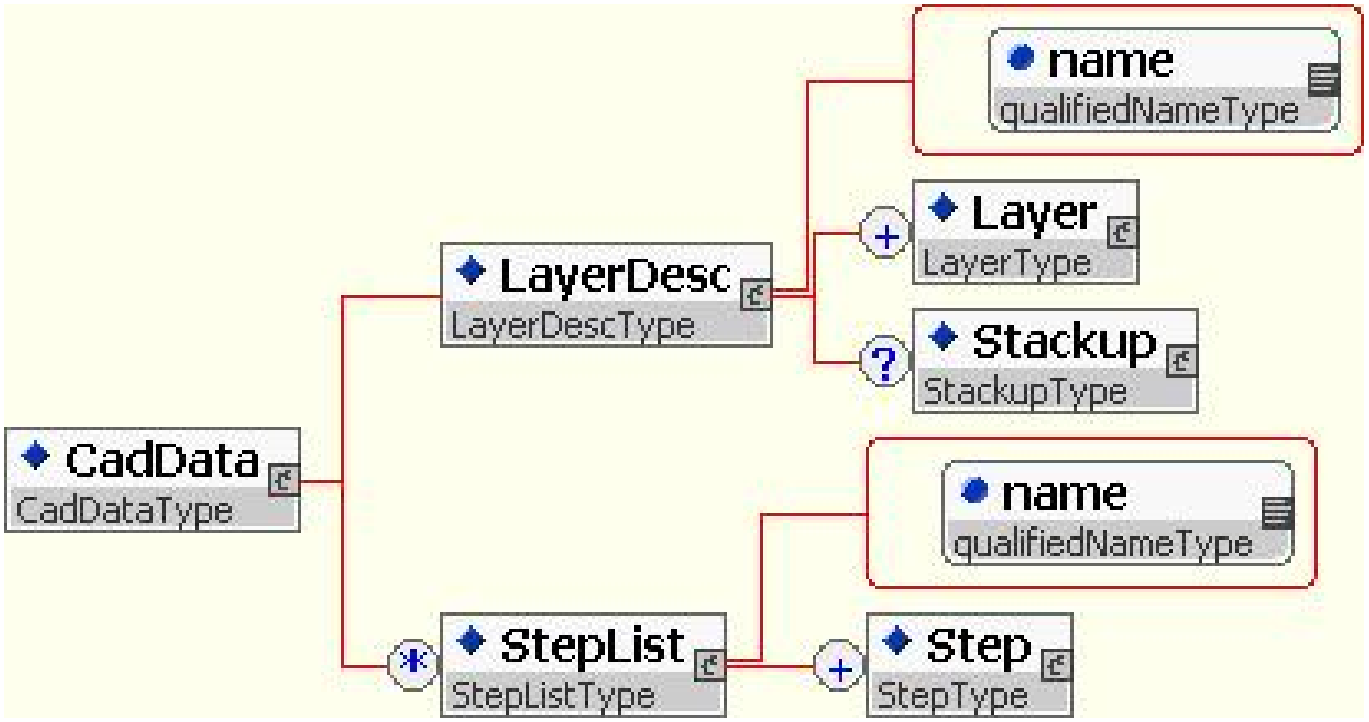



**One master list referenced to BOM items & enterprise**

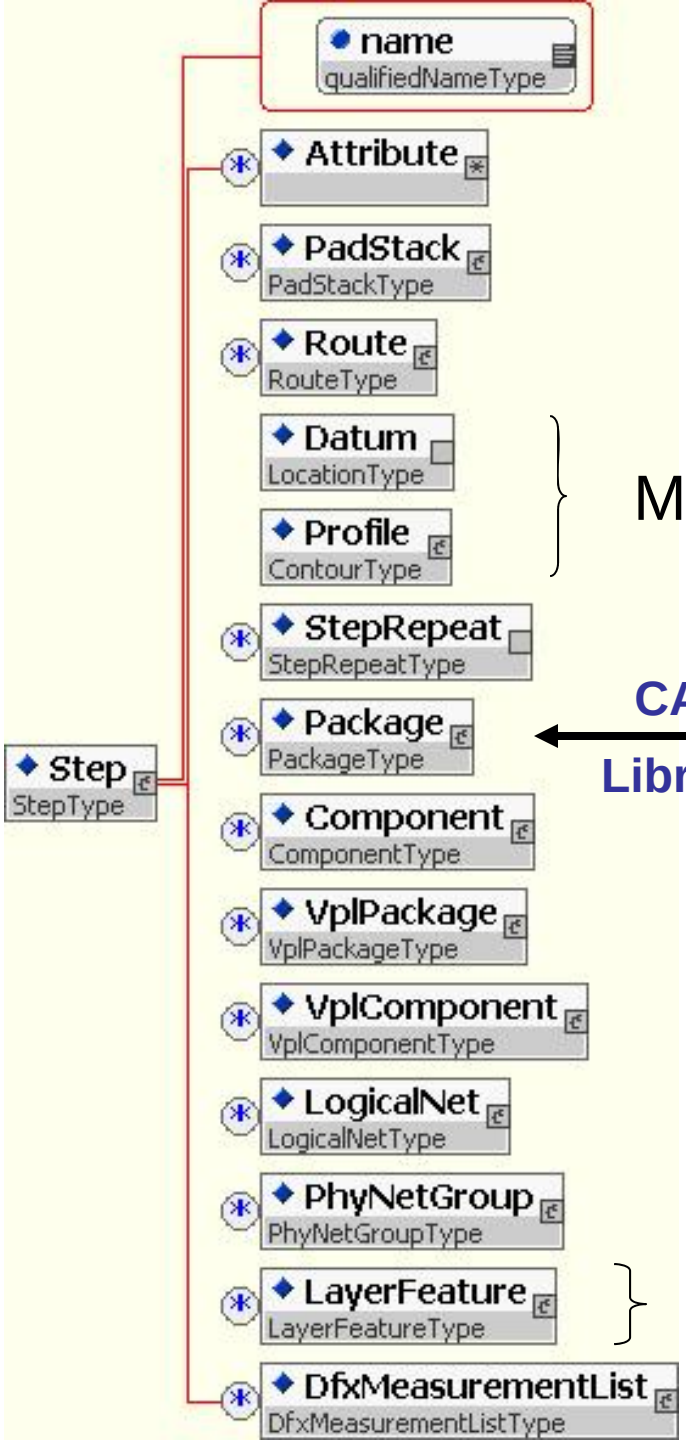
# The Heart and Stamina



# The Information Vessels



# Step Description



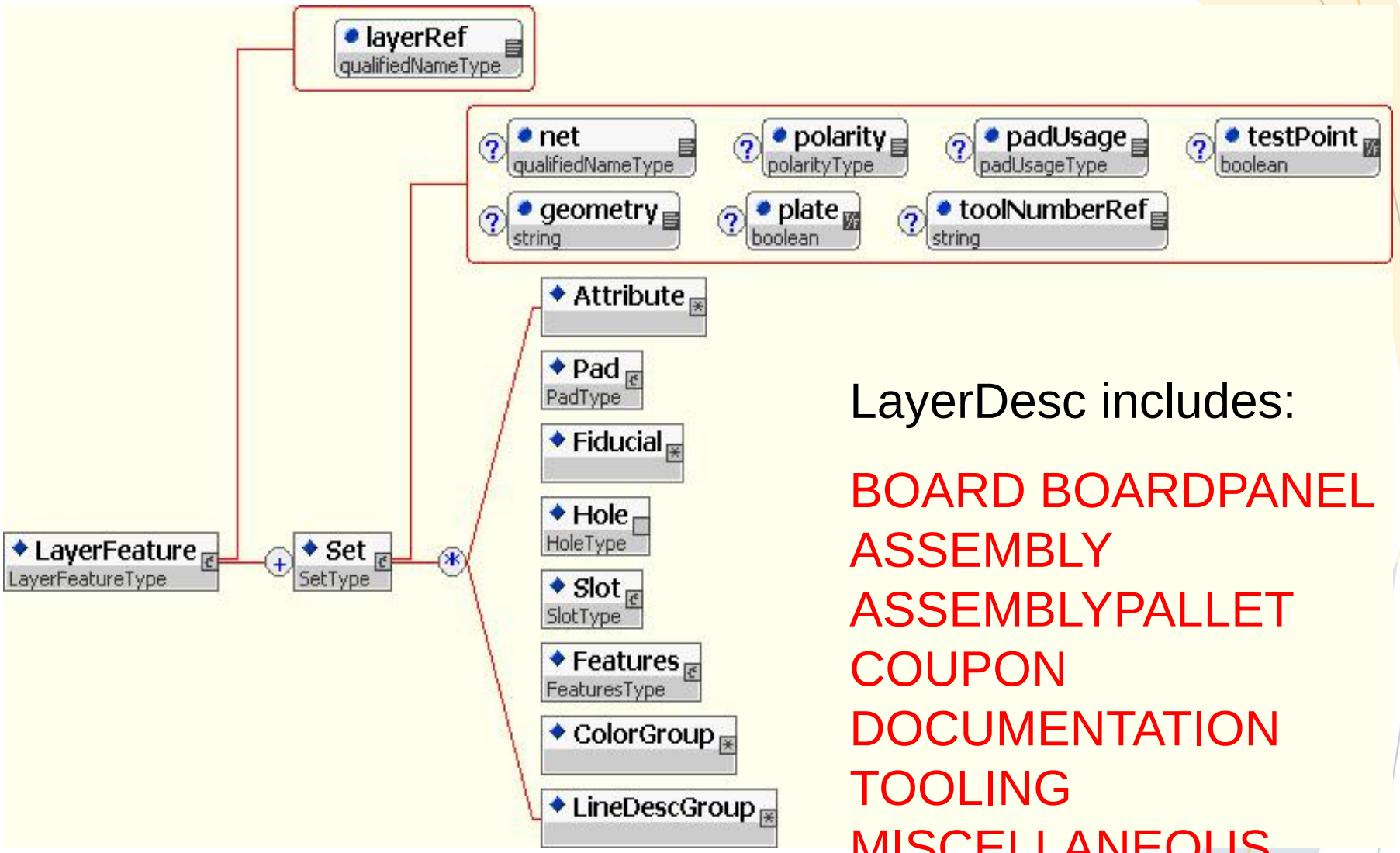

Mandatory Requirements

CAD Library

The step functions define the details of the electronic assembly. This includes the parts, conductors, net list, and DFX analysis.

The individual features

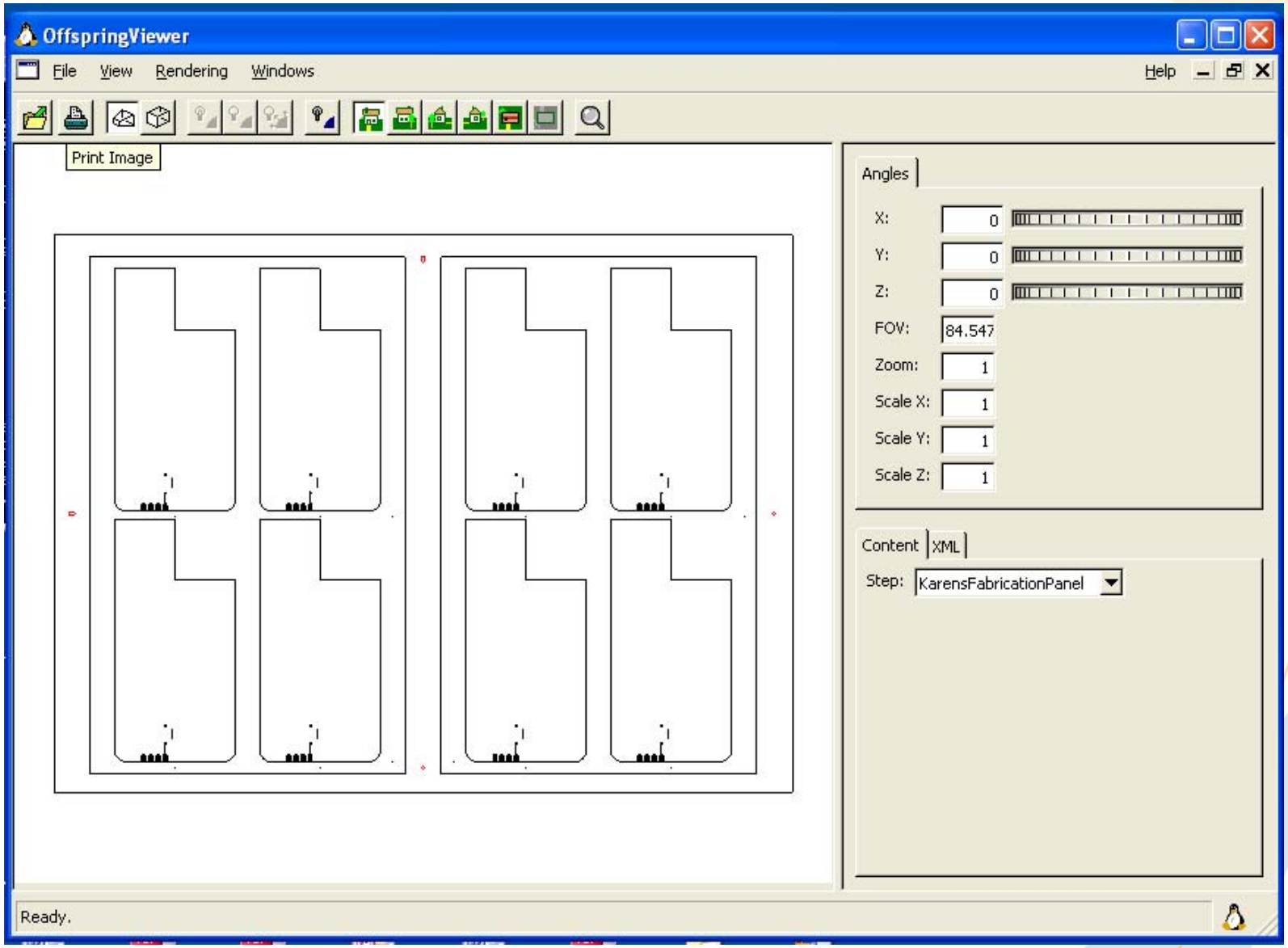
# Detail Descriptions




LayerDesc includes:

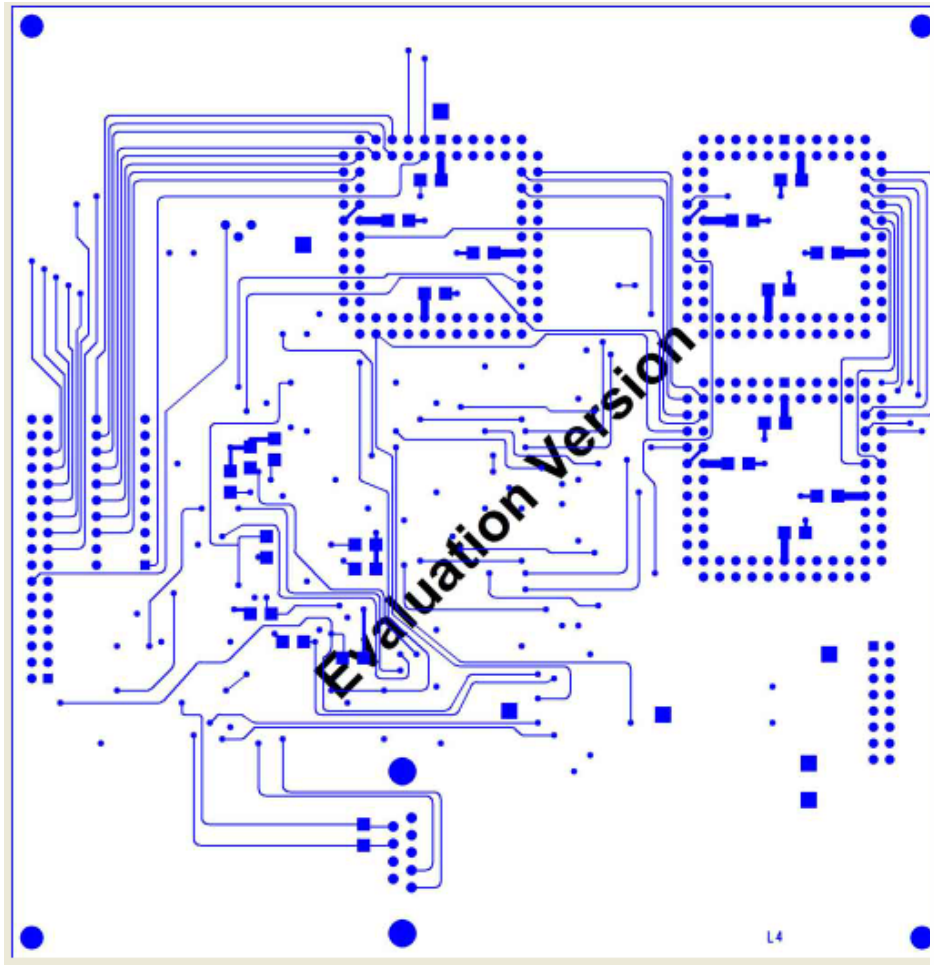
BOARD BOARDPANEL
ASSEMBLY
ASSEMBLYPALLET
COUPON
DOCUMENTATION
TOOLING
MISCELLANEOUS

# NIST Viewer

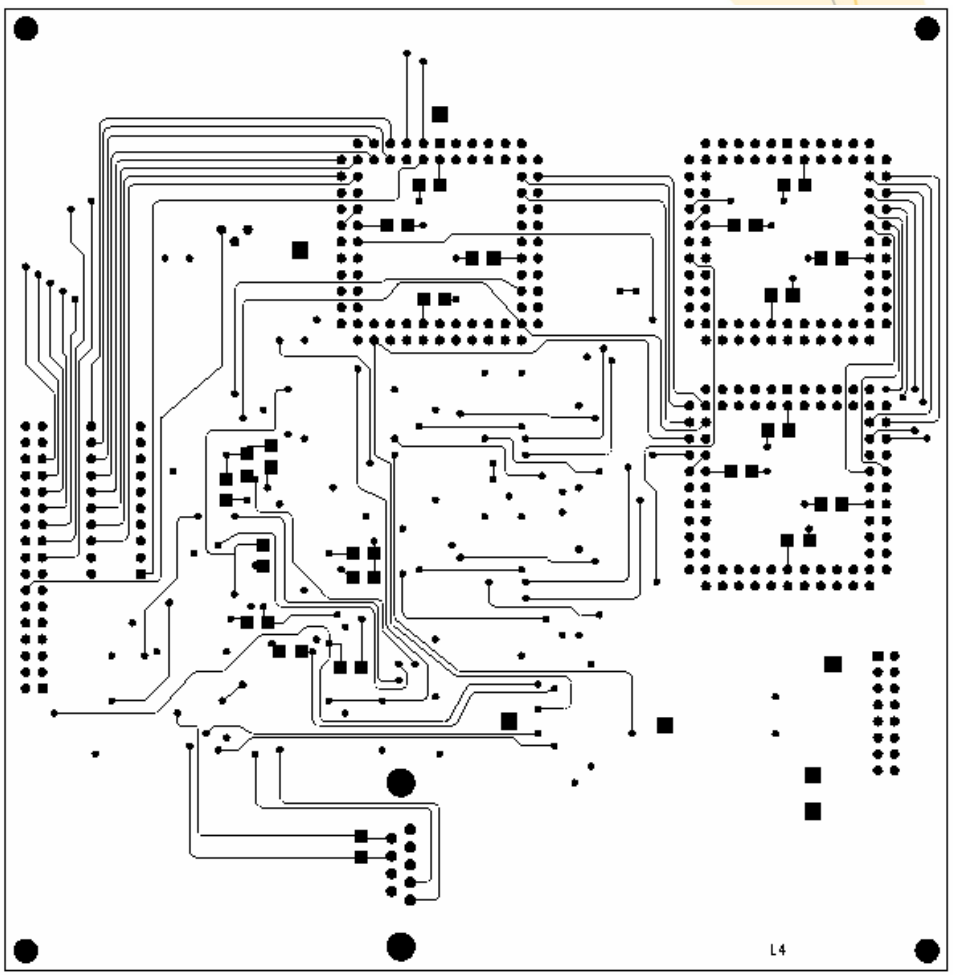

OffspringViewer
File
View
Rendering
Windows
Help
Print Image
Angles
X:
0
Y:
0
Z:
0
FOV:
84.547
Zoom:
1
Scale X:
1
Scale Y:
1
Scale Z:
1
Content
XML
Step:
KarensFabricationPanel
Ready.

# Gerber Conversion Evaluation

Original File




NIST Viewer




Next is conversion of Gerber Macros in “read me” file

# What's Next?

- Standards
  - 2580: Assembly, Testing,  BOM, Design (Archiving)
  - 2610: Assembly, Testing, BOM, Archiving
- Update to NIST Viewer
  - 3D rendering for container clearance evaluation
- Verify fabricator's & assembler's capability to read IPC-2581 data
  - Test various CAD CAM Systems
  - Need Assembler test

# Conclusions

- Many Challenges face the designer
- Mixing and matching Technologies
- Knowing the infrastructure
- Smooth transition prototype to production
- Managing supply chain communication
- Understanding material restrictions
- Created a functional Design
- Providing clear, unambiguous information