IPC-2221, Keeping pace with the times

Gary Ferrari CID+, CII
FTG Circuits
GaryFerrari@firantechnology.com (860) 350-9300
www.firantechnology.com

Surface Finishes

Electroless Nickel/Immersion Gold (ENIG)

Table 4-8 ENIG Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Moderately higher cost to OSP or HASL
Excellent wetability ,with eutectic and Pb-free solder	Multi-step process
Multiple Pb-free reflow cycles	Requires good process control
Ideal contacting surface	Poor process control may lead to Black Pad
Aluminum wire bondable	Not recommended for gold wire bonding
Shelf-Life – capable of J-STD-003 Category 3 durability	Limited re-workability
Improved PTH reliability	Solder mask must be fully cured before ENIG
Nickel barrier reduces copper dissolution during Pb free solder assembly and/or rework.	

Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG)

Table 4-XX ENEPIG Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Moderately higher cost to OSP or HASL
Excellent wetability, with eutectic and lead-free solder	Multi-step process
Multiple lead-free reflow cycles	Requires good process control
Ideal contacting surface	Limited re-workability
Shelf-Life – capable of J-STD-003 Category 3 durability	Solder mask must be fully cured before ENEPIG is plated.
Aluminum and gold wire bondable	Difficult to build thicker gold finishes over palladium
Improved PTH reliability	
No probability of “Black Pad”	
Alleviates copper dissolution from hole walls	

Electroless Nickel/Immersion Gold/Electroless Gold (ENIG/ENAG)

Table 4-XY ENEG Surface Finish Advantages and Limitations

Advantages	Limitations
Uniform coplanar surface	Limited applicability for soldering
Gold wire bondable	Multi-step process
Compression connection surface	More stringent process control of electroless gold required
Improved PTH reliability	Moderately higher cost to OSP or HASL
Shelf-Life – capable of J-STD-003 Category 3 durability	Limited re-workability
No copper sidewalls, No overhang or slivers, pad completely encapsulated	

Immersion Silver

Table 4-9 Immersion Silver Surface Finish Advantages and Limitations

Advantages	Limitations
Uniform coplanar surface	Limited re-workability
Excellent wetability ,with eutectic and lead-free solder	Solder mask \ must be fully cured before Immersion silver
Low loss finish compatible with RF design requirements	Reduced Shelf Life –in environments containing sulfur compounds or chlorides.
	Excessive thickness of IAg combined with lead-free silver bearing solder, has the potential to create an embrittled solder joint.
	No Nickel barrier allows copper dissolution during lead-free solder assembly and/or rework.

Organic Solderability Preservative (OSP)

Table 4-10 OSP Surface Finish Advantages and Limitations

Advantages	Limitations
Uniform coplanar surface	
Some OSPs do not deposit on gold	May require an aggressive flux
Reworkable, aqueous process	Boards with OSP coating requires careful handling
Controllable, automated process	Not easy to inspect or measure
No process thermal shock during application	Exposed copper areas may be vulnerable to corrosion
Preferentially coats copper	Not a suitable contact surface
Consistent compliant pin insertion and rework	Class 3 solder of holes with aspect ratios greater than 10:1 are not achievable.
Least expensive of all final finishes	
	May have limited in-process hold times
	As there is no Nickel barrier, copper dissolution may occur during lead-free solder assembly and/or rework.
	OSPs may be damaged by baking prior to soldering

Additional Finishes

- Surface Finishes not available at printing
  - Immersion Tin
  - Hot Air Solder Leveling (HASL)

Surface Finish Application Guide

Application	Lead-free Hot Air Solder Level	Organic Solderability Protection	Electroless Nickel/ Immersion Gold	Electroless Nickel/ Electroless Palladium/ Immersion Gold	Electroless Nickel/ Immersion Palladium/ Immersion Gold	Electrolytic Nickel/ Electrolytic Palladium/ Electrolytic Gold	Electrolytic Nickel/ Electrolytic Gold	Electroless Nickel/ Immersion Gold/ Electroless Gold	Immersion Tin	Immersion Silver
Reference Paragraph	4.4									
Finish Code	LF-HASL	OSP	ENIG	ENEPIG	ENIPIG	ENEPEG	Ni/Au	ENAG	iSN	iAg
Soldering	◐	◐	●	●	●	●	◐	◐	◐	◐
Gold Embrittlement	●	●	●	●	●	○	○	○	●	●
Switch Contacts	◐	○	●	●	●	●	●		○	◐
Wire Bonding	○	○	●	●	●	●	●	●	○	◐
Press Fit	●	?	●	●	●	●	●		●	◐
Compliant Pin	●	?	●	●	●	●	●		●	◐
Edge Board Connector	◐	○	○	◐	◐	●	●		○	○
Shelf Life (1 year)	◐	○	●	●	●	●	●		○	◐
Oxidation Resistance	●	○	●	●	●	●	●		◐	◐
Solderable After Multiple Reflow Cycles	●	○	●	●	●	●	●		○	●
Coplanarity	○	●	●	●	●	●	●		●	●
Radio Frequency (RF)	◐	◐	◐	◐	◐	◐	◐		◐	●
Special Packaging	●	●	●	●	●	●	●		●	◐

● = Preferred ◐ = Functional ○ = Not Recommended

Surface Finish Codes

Code	Finish	Thickness	Applicable Acceptability Specification	Marking Code[1]
S	Solder Coating over Bare Copper	Coverage & Solderable[2]	J-STD-003 J-STD-006	b0
b1	Lead-Free Solder Coating over Bare Copper	Coverage & Solderable[2]	J-STD-003 J-STD-006	b1
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable[2]	J-STD-003 J-STD-006	b3
X	Either Type S or T	As indicated by code		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	J-STD-003 J-STD-006	b3
G	Gold for edge printed board connectors and areas not to be soldered - minimum	Class 1 and Class 2 0.8 µm [31.5 µin]	None	b4
		Class 3 1.25 µm [49.21 µin]		
GS	Gold Electroplate on areas to be soldered – maximum[3]	0.45 µm [17.72 µin]	None	b4
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) – minimum	0.05 µm [1.97 µin]	None	b4
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3 µm [118 µin]	None	b4

Surface Finish Codes

GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) - minimum	Class 1 and Class 2 0.3 µm [11.8 µin]	None	b4
		Class 3 0.8 µm [31.5 µin]		
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) - minimum	3 µm [118 µin]	None	b4
N	Nickel - Electroplate for edge printed board connectors - minimum	Class 1 2.0 µm [78.7 µin]	None	N/A
		Class 2 and Class 3 2.5 µm [98.4 µin]		
NB	Nickel-Electroplate as a barrier[4] - minimum	1.3 µm [51.2 µin]	None	N/A
OSP	Organic Solderability Preservative	Solderable[7]	None	b6
HT OSP	High Temperature OSP	Solderable[7]	None	b6

Surface Finish Codes

ENIG	Electroless Nickel - minimum	3 µm [118 µin]	IPC-4552	b4
	Immersion Gold - minimum	0.05 µm [1.97 µin][5]		b4
ENEPIG	Electroless Nickel - minimum	3 µm [118 µin]	IPC-4552	b4
	Electroless Palladium - minimum	0.05 µm [2 µin]	ASTM-B-679	N/A
	Immersion Gold – minimum	Coverage and Solderable[7]	None	b4
DIG	Direct Immersion Gold (Solderable Surface)	Solderable[5]	None	b4
IS	Immersion Silver	Solderable[6]	IPC-4553	b2
IT	Immersion Tin	Solderable[7]	IPC-4554	b3
C	Bare Copper	AABUS	AABUS	N/A

Surface Finish Codes – cont'd

Note 1. These marking and labeling codes represent the codes for surface finish categories established in IPC/JEDEC-J-STD-609.

Note 2. Hot Air Leveling (HAL) or Hot Air Solder Leveling (HASL) processes are considered to have a degree of difficulty in their control. This, coupled with pad sizes and geometries placing additional challenges on such processes, places the creation of a practical minimum thickness outside the scope of this specification. See also 4.4.7.

Note 3. Industry investigations have shown that a gold-tin intermetallic phase forms under normal soldering process parameters when the weight percent of gold in the solder joint reaches the 3-4% range. Refer to IPC-J-STD-001 and IPC-HDBK-001 for further information on gold removal to prevent the formation of brittle solder joints resulting from high concentrations of gold dissolving into the solder joint.

Surface Finish Codes

Note 4. Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.
Note 5. See also 4.4.4.1.
Note 6. Surface measurements, when required for immersion silver thickness, require a unique pad size for both thin and/or thick silver deposits. See IPC-4553 for detailed measurement requirements.
Note 7. See 4.4.7.

Assembly Marking

Marking for Lead Free Assemblies

Suggested marking per J-STD-609

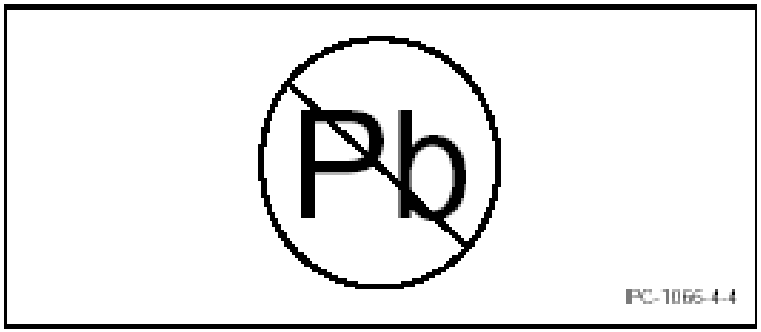


Figure 4-4 Pb-Free Symbol

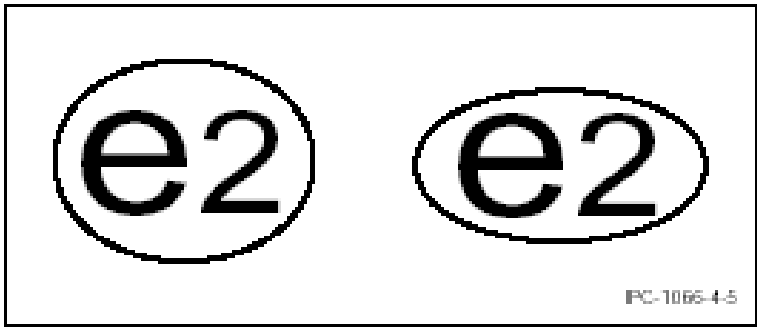


Figure 4-5 Example of Mark Showing Category 2 and Option of Circle or Ellipse

5 LABELING CATEGORIES

5.1 Solder Finish Categories The following categories are meant to describe the Pb-free 2nd level interconnect (see Figure 4-5) terminal finish/material of components and/or the solder paste/solder used in assembly.

e1 – SnAgCu
e2 – Other Sn alloys (ie. SnCu, SnAg, SnAgCuX, etc.) (No Bi or Zn)
e3 – Sn
e4 – Precious metals (ie. Ag, Au, NiPd, NiPdAu, but no Sn)
e5 – SnZn, SnZnX (no Bi)
e6 – Contains Bi
e7 – Low temperature solder (<150°C) containing indium but no bismuth

e8, e9 symbols are unassigned categories at this time.

Testing

Testing

- Assembly testing

  - Boundary Scan (JTAG)
    a) for high density where probe testing is not possible
    b) at a connector – must have compatible components

  - Functional Test
    a) go/No Go
    b) at a connector

  - In Circuit Test (ICT)
    a) bed of nails fixtures
    b) electrical considerations

Testing

- Bare Board Testing – implements IPC-9252A Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

  - resistive continuity (IPC-9252)
    a) measures the resistance of the net: high, good; low, bad
  - resistive isolation (IPC-9252)
    a) Measures resistance between isolated nets: high, good; low, bad
  - indirect isolation & continuity
    a) Measures electrical properties: Capacitance, RF, Impedance, Etc
    b) Insulation resistance & Hi Pot testing

Testing

- Impedance testing
  a) Coupon design

Sample notes:

- XX. Impedance testing (IPC-TM-650, Method 2.5.5.7)
- XX.1 Single ended: (Conductor widths .0059 on Layer X)
- The printed board shall exhibit a characteristic impedance of 52.5 ohms (+/- 15%) as measured using a Time Domain Reflectometer (TDR) which shall be verified by measurement of impedance coupons supplied by the fabricator.
- XX.2 Differential pairs: (Conductor widths .0059 on layer X)
- The printed board shall exhibit a characteristic impedance of 105 ohms (+/- 15%) as measured using a Time Domain Reflectometer (TDR) which shall be verified by measurement of impedance coupons supplied by the fabricator.

Special Materials

Generic Overview of Electronic Component Materials

- Embedded (Buried) Resistors
  - Cost drivers
  - Application drivers
  - Special applications
- Embedded (Buried) Capacitors
  - Distributed capacitance (planar)
- Embedded (Buried) Inductors

Special Requirements

Lead Free References

Added to the following sections:

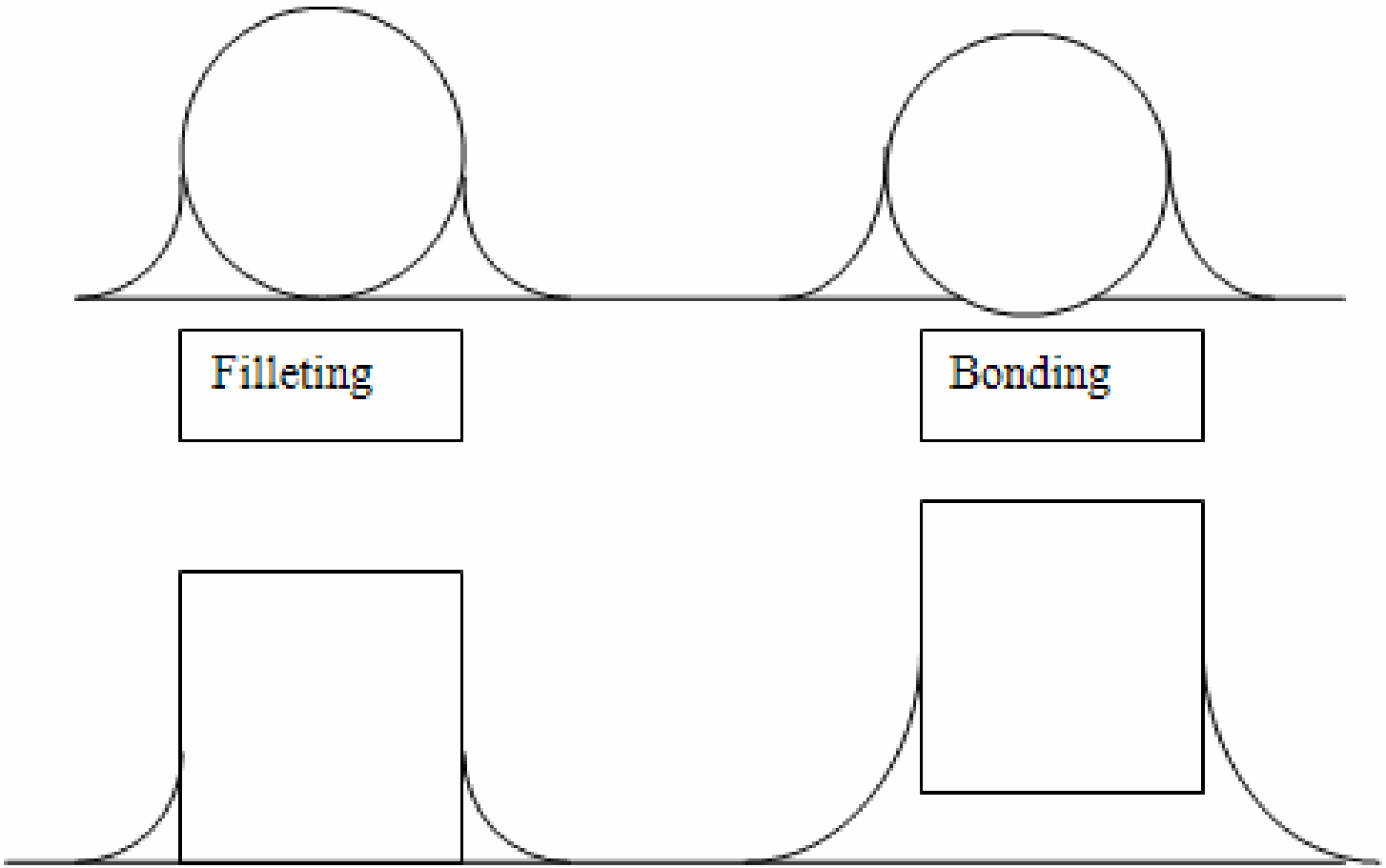
- Materials
- Surface Finishes
- Fabrication
- Components
- Assembly

Tin Whisker Mitigation

- *Conformal coatings*, in particular Type UR, are sometimes used to *help mitigate* tin whiskers as a means of reducing the potential for an electrical short circuit. *However*, when used for this purpose, it is recommended that a second method of tin whisker mitigation be used since *tin whiskers can grow under the coating or may penetrate the coating*, depending on its thickness. See IPC/JEDEC-JP002 for additional information.

Shock and Vibration - Component Bonding

Filleting – after placement of components



Thermal Management – Heat Sinks

Table 7-3 Printed Board Heatsink Assembly Preferences

Method	Major Advantages	Major Disadvantages	Considerations
Rivets	Fastest, no cure cycle or adhesive application	Printed board area and holes needed for rivets	Use standard rivet sizes
Screws	Allows disassembly	Requires washers and nuts, printed board area and holes	Use standard hardware
Film Adhesive	No wasted space, potentially improved heat transfer, higher vibration natural frequency. Increased insulation	Cure time and possible warpage	Low cure temperature will minimize warpage
Liquid Adhesive	No waster space, potentially improved heat transfer, higher vibration natural frequency	Producibility concern as well as cure time and warpage concern	Low cure temperature will minimize warpage

PC Cards (PCMCIA) Technology

- Retiring IPC-2224 Sectional Standard for Design of PWB's for PC Cards

Form Factor Type	Length (+/-0.02)	Width (+/-0.01)	Interconnect Area[1] (+/-0.005)	Substrate Area[1] (+/-0.01)
Type I	85.6 mm	54.0 mm	4.19 mm	4.19 mm
Type II	85.6 mm	54.0 mm	4.19 mm	6.35 max.
Type III	85.6 mm	54.0 mm	4.19 mm	10.0 mm

IPC-2221 to include specific PC Card requirements:

- Smaller features
- Thinner dielectrics
- Reliability issues

PC Cards (PCMCIA) Technology

- Thermal Considerations
  - Maximize planes on every layer
  - Thermal creams of plane rails
  - “Hot” component placement
  - Housing materials
  - Card mounting environment

Conductor Routing

- Internal lands should not be removed to “make enough room” to route a circuit between holes. To help maintain internal minimum spacing, circuit routing should always be performed with all of the lands in place on all layers for each hole. After all circuits have been routed, nonfunctional lands may be removed. (See IPC-2222, section 9.1.4.)

Electricals

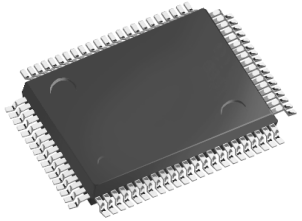
To be Added:

- Applicable reference to IPC-2152 - Standard for Determining Current-Carrying Capacity in Printed Board Design
- Planar Capacitance structures

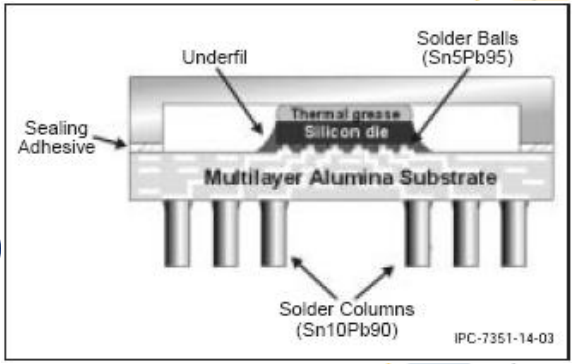
Components

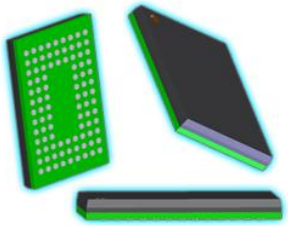
Expanded Component Section

Includes

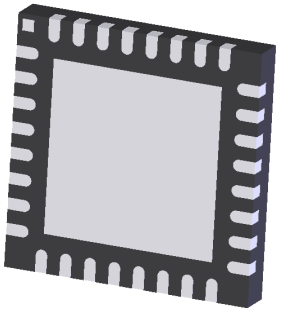


- Component Lead Sockets
- Fine Pitch Devices
  - Thin shrink small outline package (TSSOP)
  - Shrink Quad Flat Package (SQFP)
- Grid Array SMT
  - Ball Grid Array (BGA)
  - Fine Pitch Ball Grid Array (FBGA)
  - Column Grid Array (CGA)
  - Land Grid Array (LGA)

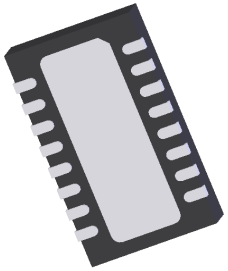


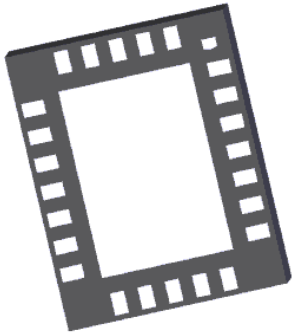


Expanded Component Section



- No Lead Devices
  - Quad Flat No-Lead (QFN)
  - Small Outline No-Lead (SON)
  - Quad Flat No-Lead with Pullback Leads (PQFN)
  - Small Outline No-Lead with Pullback Leads (PSON)



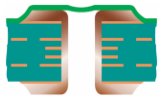
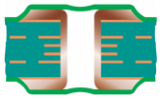
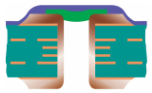
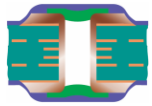
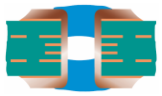
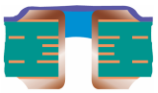


Expanded Component Section

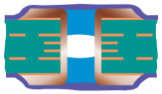
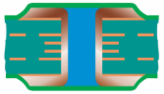
- Compliant Pin Systems
  - Considerations
    a) Standards
       – Insertion and Retention Forces
    b) Qualification as a System
    c) Surface Finishes and Coatings
       – Corrosion compatibility
       – hardness
    d) Environmental

Via Protection

Via Protection - Types

	Description (Type)	Before Final Finish	After Non-Melting Metal Final Finish	Prevent air leakage in ICT (Vacuum Seal)[2]	eeping chemistry or solder from passing through the via	Keeping chemistry or solder from being trapped in the via	Dielectric protection of via land	Fill holes in cores prior to lamination	Improves surface planarity	Prevent migration of solder, adhesives or encapsulants into vias
	Tented-Single-Sided (Ia)	NOT RECOMMENDED[5]								
	Tented –Double-Sided (Ib)	X	X	X	X	X	X			X
	Tented and Covered-Single-Sided (IIa)	NOT RECOMMENDED[5]								
	Tented and Covered-Double-Sided (IIb)	X	X	X	X	X	X			X
	Plugged Single-Sided (IIIa)	NOT RECOMMENDED[5]								
	Plugged Double-Sided (IIIb)	X	X	X	X	X	X		X	X
	Plugged and Covered Single-Sided (IVa)	NOT RECOMMENDED[5]								

Via Protection - Types

	Description (Type)	Before Final Finish	After Non-Melting Metal Final Finish	Prevent air leakage in ICT (Vacuum Seal)[2]	Keeping chemistry or solder from passing through the via	Keeping chemistry or solder from being trapped in the via		Fill holes in cores prior to lamination		Best for thermal conductivity[3]	Prevent migration of solder, adhesives or encapsulants into vias
	Plugged and Covered Double-Sided (IVb)	X	X	X	X	X	X				X
	Filled (fully plugged) (V)	X	X	X	X	X		X	X	X	X
	Filled and Covered (VI)	X	X	X	X	X	X				X
	Filled and Capped (VII)[4]	X	X	X	X	X		X	X	X	X

Derived from Table 5-1 of IPC-4761

1) Descriptions of specific types of via protection are provided in IPC-4761 5.1 through 5.7.

2) Not recommended over melting metals.

3) It is recommended to use a thermally conductive hole filling ink (e.g. silver ink).

4) When specifying Via-in-Pad, it is recommended that Type VII via protection be used.

5) See IPC-4761 3.4 for concerns associated with single sided via protection.

Via Protection

	Tented no fill	Tented and covered	Plugged	Plugged and Covered	Filled	Filled and covered	Filled Capped
Type(b)	I	II	III	IV	V	VI	VII
Minimum Class 1,2	N.A.	N.A.	0.010	0.010	0.010	0.010	0.010
Minimum Class 3	N.A.	N.A.	0.010	0.010	0.013	0.013	0.013
Maximum Class 1 and 2	0.0256	.040	0.050	0.050	0.040*	0.040*	0.040*
Maximum Class 3	0.0256	.0256	0.050	0.050	0.040*	0.040*	0.040*
Maximum Aspect Ratio*** Class 1,2	N.A.	N.A.	N.A.	N.A.	8	8	8
Maximum Aspect Ratio*** – Class 3	N.A.	N.A.	N.A.	N.A.	8	8	8
Minimum Aspect Ratio **Class 1,2	N.A.	N.A.	N.A.	N.A.	3	3	3
Minimum Aspect Ratio** – Class 3	N.A.	N.A.	N.A.	N.A.	3	3	3

Via Protection

Maximum Aspect Ratio*** Class 3	N.A.	N.A.	N.A.	N.A.	8	8	8
Minimum Aspect Ratio **Class 1,2	N.A.	N.A.	N.A.	N.A.	3	3	3
Minimum Aspect Ratio** Class 3	N.A.	N.A.	N.A.	N.A.	3	3	3

* Larger diameter hole fills can be done. Depends on aspect ratios, hole fill material and environment

** Minimum aspect ratio is for thin printed boards/cores below 0.031 inches

***Maximum Aspect Ratio dependent on hole fill material and thickness. This aspect ratio refers to the minimum hole size mentioned in the table. Ie. .010” hole and aspect ratio of 8.