Relationship Between Via Size and Cleanliness

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Abstract
Microvia technology has many advantages: it requires a smaller designed area, which saves the board size and weight, using less space, allowing for a smaller PCB, which can results in lower costs, and the microvia allows for better performance due to a shorter pathway. The practical definition of microvia technology is "high density printed circuit substrates that employ via diameters of under 10 mils [250 microns] in diameter." With all the benefits of the microvia, cleaning issues are often overlooked. Bare board manufacturers have been effective in cleaning the larger vias; however, is the cleaning process as effective on the smaller vias? Failure analysis data suggests that etch residues from the build process are being left in the microvias causing corrosion and electromigration failures. If residues are in vias under components, the risk of contamination related failures increases. Ion chromatography results repeatedly reveal the importance of board and component cleanliness as an indicator of product performance. Manufacturers have historically used a standard rinse process with heated de-ionized water after etch to remove process residues. This process has been effective with traditional larger vias, but may no longer be an effective process with microvia technology. This paper will explore multiple via sizes, different approaches to cleaning, and what data shows may be the most viable option for producing good performing product.

Introduction
Microvia technology provides many advantages linked to its smaller designed area. These advances stem from condensed board size and weight resulting in lower costs and better performance due to a shortened pathway. With such desirable advantages, microvia technologies are being rapidly deployed in increasingly harsh environments and under stringent reliability requirements. The expectation is for these market integrations to be accomplished efficiently, maintaining the cost reductions inherent to the design of this technology. Unfortunately, this goal often neglects the level of quality and reliability considered during processing in favor of prioritizing the manufacturer's bottom line. If efficiency and cost-effectiveness are paramount in design and production, the need for a realistic understanding of what inputs contribute directly to field reliability and to what extent is crucial, especially during the adoption period of an emerging technology such as the microvia. When a microvia lies underneath a component, reliability risks increase even further.

Ionic cleanliness is an established mechanism cited in many of today's field failures. Because of this fact, Foresite has taken the initiative to understand what levels of ionic contamination should be deemed acceptable in relation to the reliability necessitated by differing classes of products and technologies. Historically the acceptance criteria is based on a full bare board extraction that can normalize pockets of contamination such as within the vias over the total surface area. As packaging continues to become denser and more intricate, the potential for trapped ionic residues naturally increases and sensitivity levels require adjusting. The specific issue of via cleanliness in relation to diameter arose from a customer project Foresite encountered involving field returns that targeted a PQFN as the culprit. After mechanically removing the PQFN component in question, the failure analysis team discovered a microvia underneath the part. This discovery became the basis of a paper presented at APEX 2009, *Pockets of Contamination that are Causing Field Failures and How to Avoid Them.* Though this paper discussed helpful findings aimed at mitigating field failures, it also raised the question of just how clean vias are after normal PCB processing, and what should be the acceptable levels of cleanliness for this technology.

Typically, PCB manufacturers have effectively utilized a standard rinse process with heated de-ionized water to remove process residues after etch. This process has proved acceptable for larger diameter vias, but with the introduction of increasingly smaller diameter microvias, it is questionable whether this standard process still cleans PCBs effectively. This study explores the resulting ionic cleanliness levels achieved during normal processing considering a multitude of varying via diameters. We will also examine alternative cleaning protocols and what corresponding cleanliness levels are achieved in an attempt to uncover best practices with regard to PCB fabrication that involves microvia technologies.

Methodology
As an extension of Foresite's 2009 study on pockets of contamination underneath PQFN components that turned out to be driven by an underlying microvia, our team of failure analysts conducted an independent blind study to explore typical levels of via cleanliness after normal PCB processing. The first step in our lab's analysis involved commissioning the production of a group of test boards (figure 1) with 6 each 4/5, 6, 8, 10, and 12 mil vias. For the smallest size via, 4/5 mil we were told that the process was to use a 4 mil bit but the smallest amount of wobble will increase the size to include 5 mil. As we understand

the 4 mil size is uncommon in standard build practice for most electronics at this point. The vendor of the test boards was unaware of the intended use of these boards, and thus our analysis team did not request or receive exact specifications on etchant materials used. This scenario allowed for an unbiased, real-world example of typical boards a manufacturer could expect to receive from a fabricator.

After receipt of the test boards each containing 5 different sizes of microvias, our team began its ionic cleanliness investigation by extracting localized samples from the microvia sites along with a bare board reference site. This was accomplished by utilizing the C3 localized cleanliness tester to effectively penetrate and flush out the vias with a localized burst of deionized steam allowed to soak and draw out ionic contaminants. This localized sample is then aspirated into a testing cell containing a y-electrode that provides an immediate spot-check as to the cleanliness of the sample based on predetermined cleanliness parameters. Though the immediate 'clean' or 'dirty' reading provides a good indicator as to the contamination level of the sites in question, our study aimed to examine the exact types and quantities of residues present with more specificity. Figure 2 shows an example of the flow thru achieved with the localized tester. Actual testing was performed with Kapton® tape covering the bottom side of the open vias to stop the flow of extraction solution and allow for IC testing of solubulized residues. Photo is meant to show evidence of effectiveness of extraction procedure. Data points of bare reference areas as well as tape samples were tested and subtracted from the IC totals.

Now that our team had obtained localized samples of the varying sizes of vias on our test subjects, the extracted samples then underwent ion chromatography analysis under the guidance of IPC-TM-650. Knowing that typical etchant materials include ammonium persulfate, ferric chloride, and sodium persulfate, the main anions of concern for this study were ammonia, sulfate, and chloride.

4/5 Mil

6 Mil

8 Mil

10 Mil

12 Mil

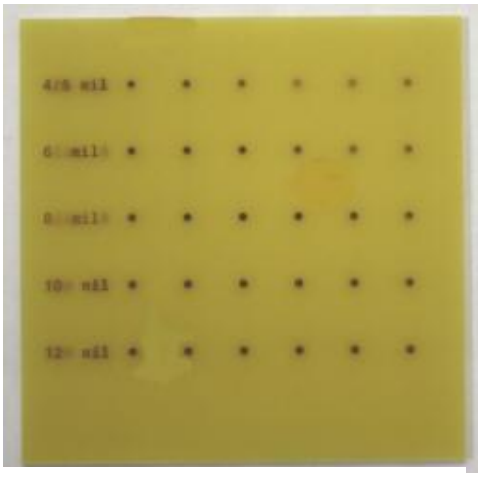


Figure 1-Via Test Board

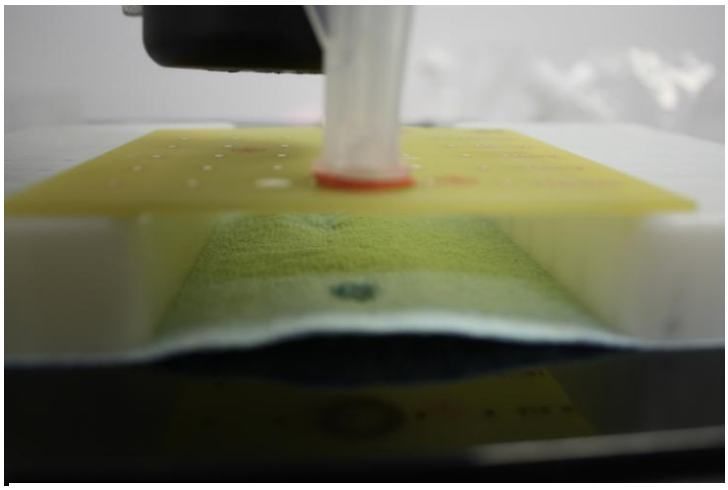


Figure 2- Localized Extraction Example over 4/5 Mil via

When considering via cleanliness, Foresite's hypothesis lies in the thought that the surface tension of heated deionized water does lower the surface tension (figure 3) it is still too high to properly flush out and clean all of the etchant residues in the microvia sites. Lower surface tension makes it a better "wetting agent" to get into pores and fissures rather than bridging them with surface tension. Saponifier and wetting agents further lower the surface tension.

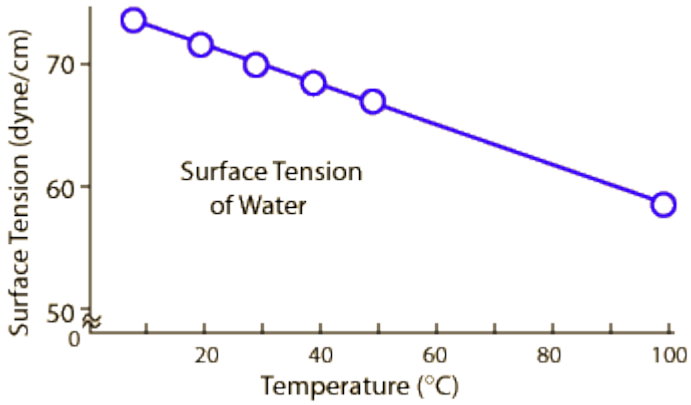


Figure 3-Surface Tension of Heated Rinse Water

Ion Chromatography Methodology

• All testing was performed on a Dionex ICS 3000 ion chromatography system using Chromeleon software

• Controls and blanks were performed on the Dionex ICS 3000 ion chromatography system before the test began. *NOTE: Foresite used NIST-traceable standards for all system calibrations*

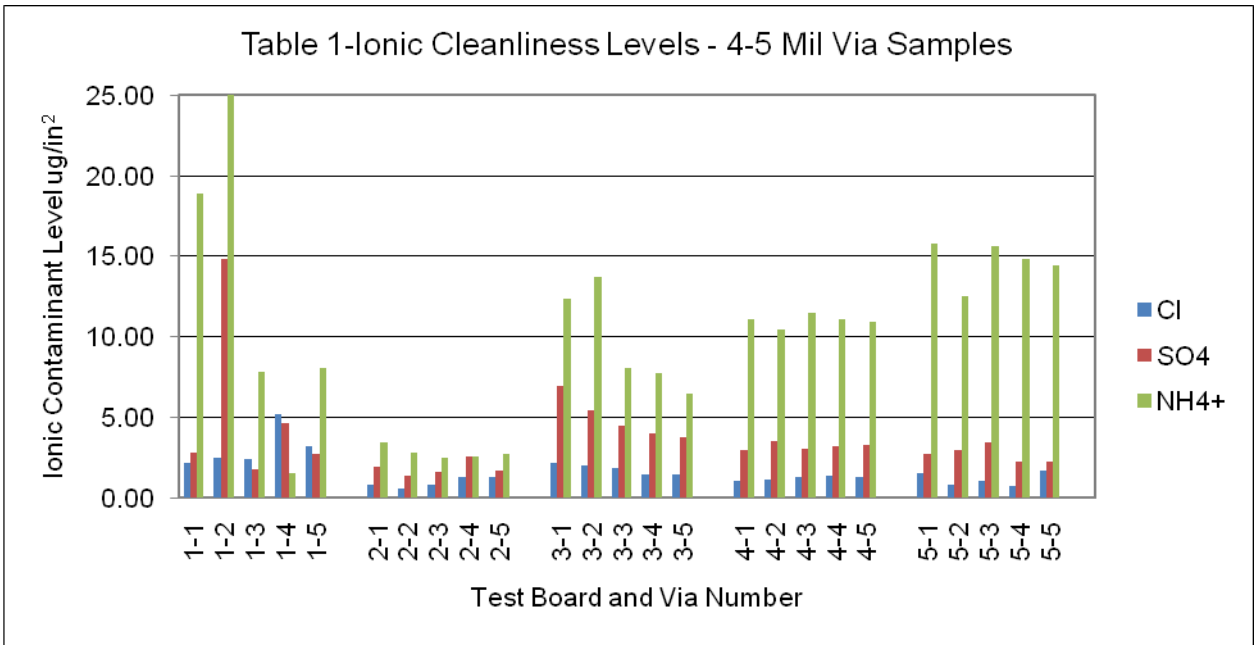
• A 1.5mL sample of each test samples' extracted solution was analyzed using a 1.7mM sodium bicarbonate/1.8mM sodium carbonate eluent.

Test Matrix

Bare Multiple Via Test Board		# of test	Results
Assessment #1	4/5 mil via	25 repetitions	Test Results Table #1
Assessment #2	6 mil via	25 repetitions	Test Results Table #2
Assessment #3	8 mil via	25 repetitions	Test Results Table #3
Assessment #4	10 mil via	25 repetitions	Test Results Table #4
Assessment #5	12 mil via	25 repetitions	Test Results Table #5

Data Results

In the charts below the ion chromatography results have been broken down into each via size and test board number (tables 1-6). A total of 25 extractions for each via size were performed across five test boards, with bare reference areas.



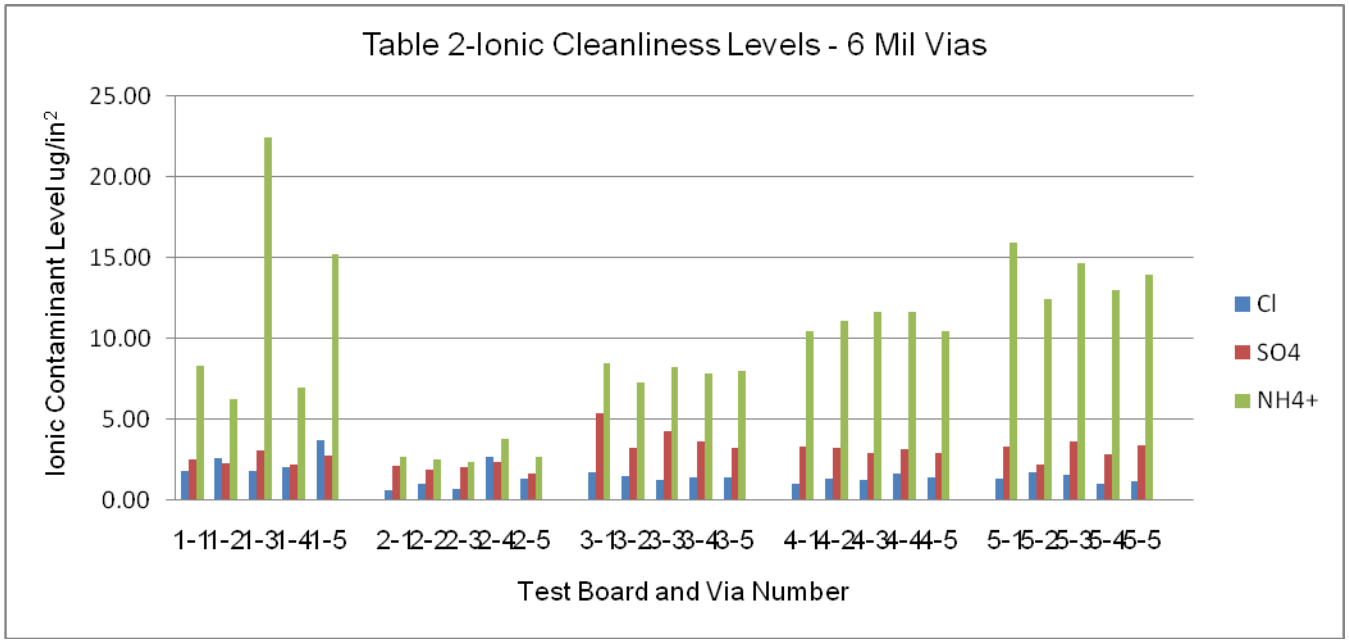


Table 2-Ionic Cleanliness Levels - 6 Mil Vias
Ionic Contaminant Level ug/in2
25.00
20.00
15.00
10.00
5.00
0.00
1-1 1-2 1-3 1-4 1-5 2-1 2-2 2-3 2-4 2-5 3-1 3-2 3-3 3-4 3-5 4-1 4-2 4-3 4-4 4-5 5-1 5-2 5-3 5-4 5-5
Test Board and Via Number
Cl
SO4
NH4+

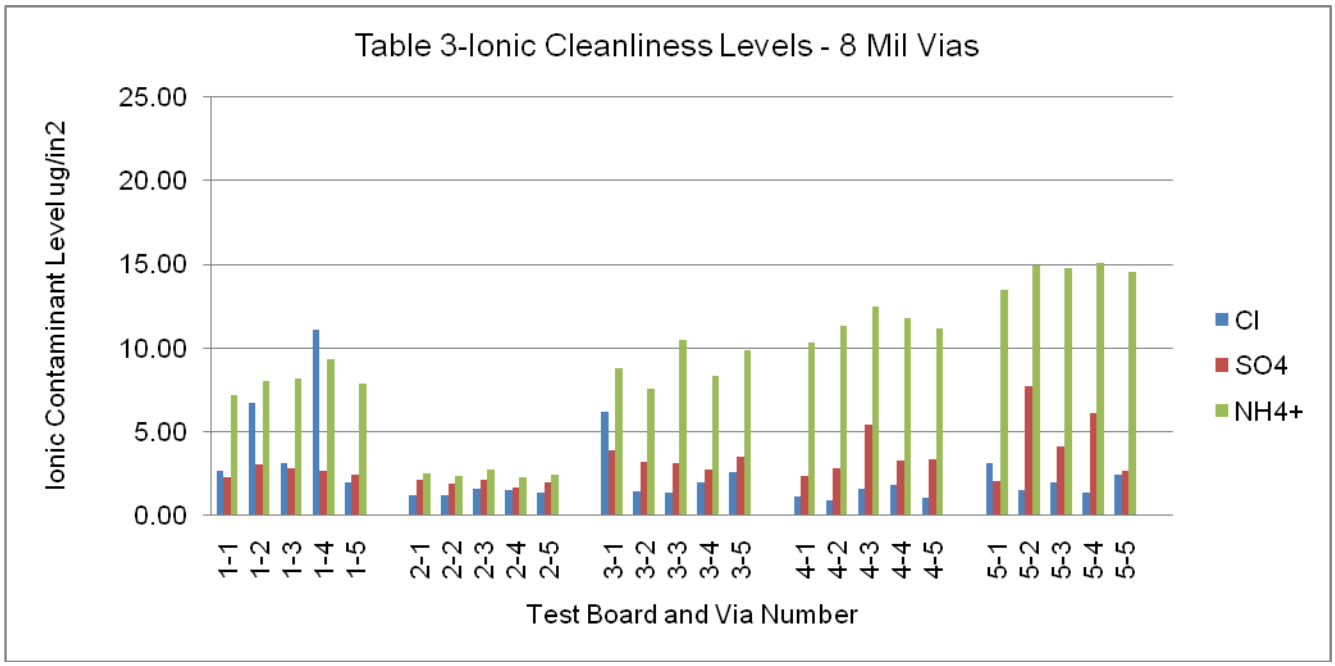


Table 3-Ionic Cleanliness Levels - 8 Mil Vias
Ionic Contaminant Level ug/in2
25.00
20.00
15.00
10.00
5.00
0.00
1-1 1-2 1-3 1-4 1-5 2-1 2-2 2-3 2-4 2-5 3-1 3-2 3-3 3-4 3-5 4-1 4-2 4-3 4-4 4-5 5-1 5-2 5-3 5-4 5-5
Test Board and Via Number
Cl
SO4
NH4+

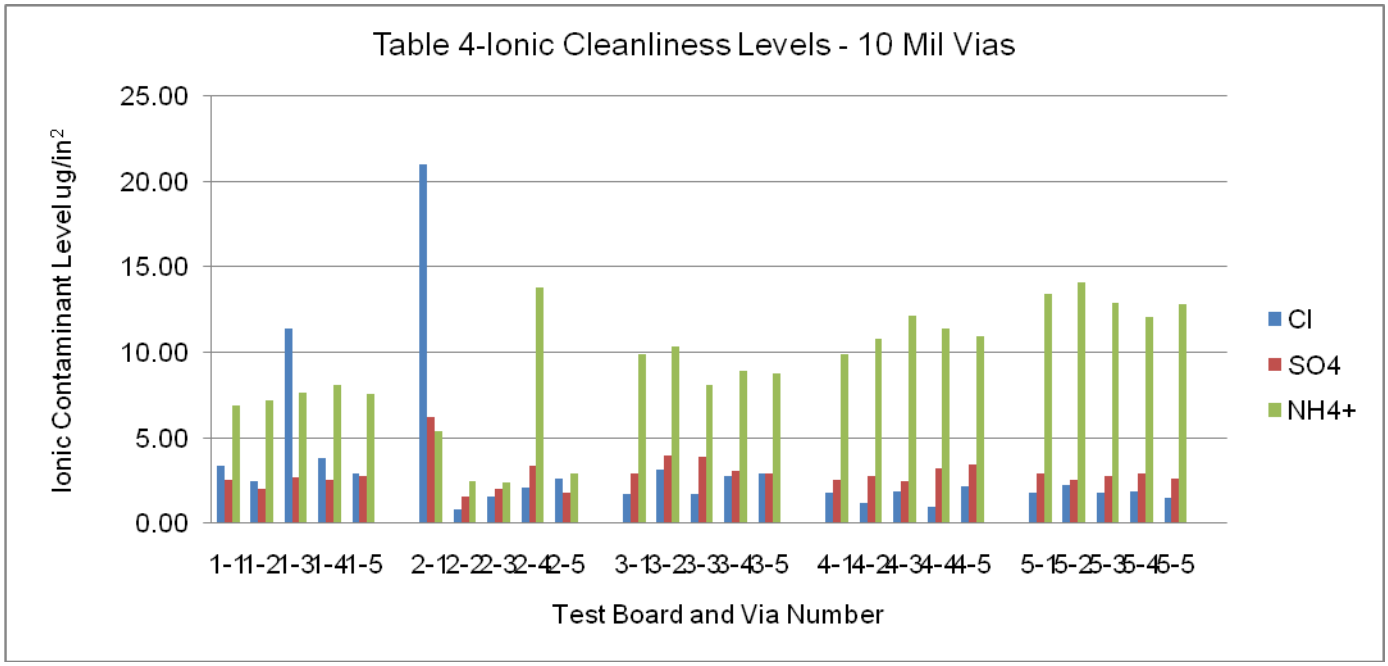


Table 4-Ionic Cleanliness Levels - 10 Mil Vias
Ionic Contaminant Level ug/in2
25.00
20.00
15.00
10.00
5.00
0.00
1-1 1-2 1-3 1-4 1-5
2-1 2-2 2-3 2-4 2-5
3-1 3-2 3-3 3-4 3-5
4-1 4-2 4-3 4-4 4-5
5-1 5-2 5-3 5-4 5-5
Test Board and Via Number
Cl
SO4
NH4+

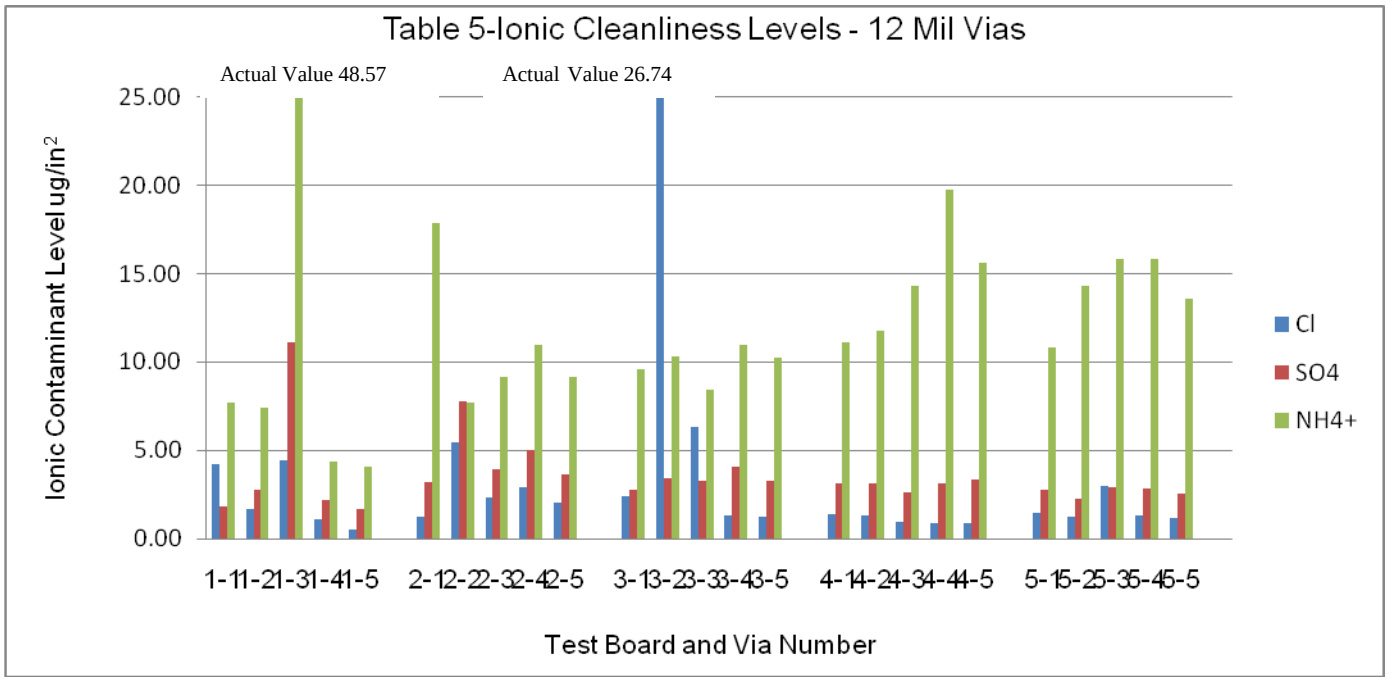
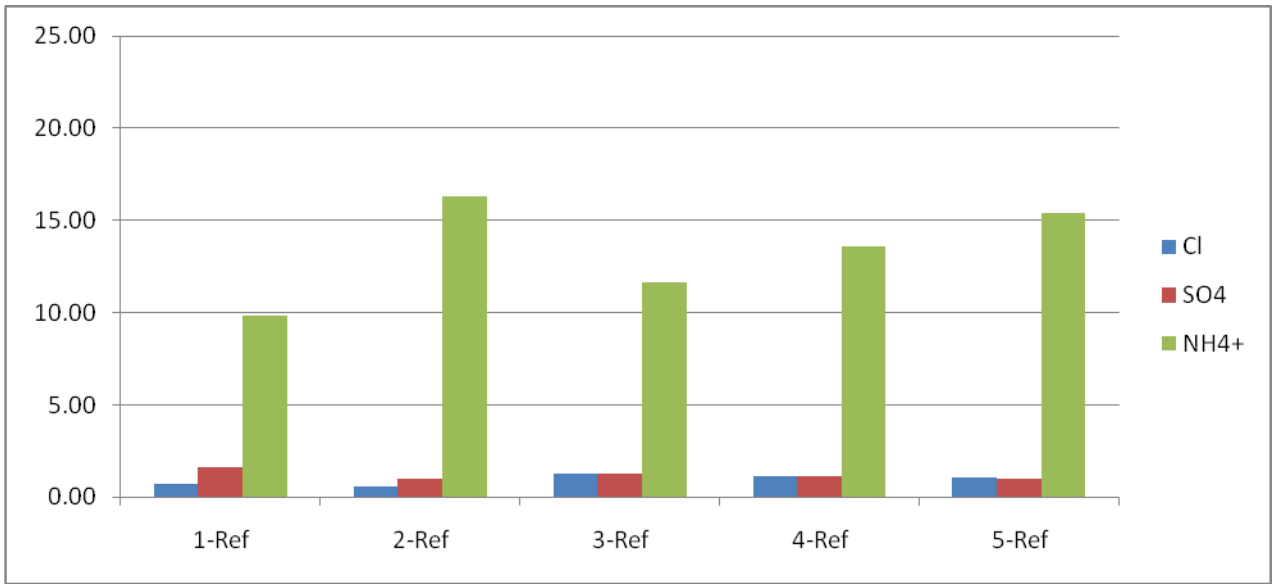


Table 5-Ionic Cleanliness Levels - 12 Mil Vias
Actual Value 48.57
Actual Value 26.74
Ionic Contaminant Level ug/in2
25.00
20.00
15.00
10.00
5.00
0.00
1-1 1-2 1-3 1-4 1-5
2-1 2-2 2-3 2-4 2-5
3-1 3-2 3-3 3-4 3-5
4-1 4-2 4-3 4-4 4-5
5-1 5-2 5-3 5-4 5-5
Test Board and Via Number
Cl
SO4
NH4+

Table 6-Bare Board Reference Areas Away from Vias



Data shows that there is a very wide range of amounts of contaminants in each and every via size tested. The bare reference areas tested show low levels of chloride and sulfate with fairly high levels of ammonium (table 6) so we can say that the residues are confined to the vias themselves and not other outside factors. The levels of contamination from test board to test board are a varying factor that we did not anticipate, as the five test boards selected were chosen as the first five out of a sealed package. Test board number two shows lower levels of all contaminants in vias of all sizes when compared to the other four test boards. This proves the inconsistent nature of rinsing on not only different via sizes but also boards within the same lot. In general the test results show that via sizes of 10 and 12 mils are cleaner than those under 10 mil with a few outliers. We believe that this only furthers the need to better understand levels of cleanliness inside vias of all sizes.

Conclusion

Like every assembly process many cleanliness parameters should be taken into consideration when looking at acceptability criteria for your specific product. There are other unknowns that could also play a significant part in the addition of residues, these include but are not limited to, cleaning parameters at each different board supplier for bath life change out indicators, temperature of rinsing, quality of incoming rinse water, belt speed, impingement angles, pressure of rinse etc. If you plan on using microvias in your design and especially if any of these are to be open and placed under a low stand-off component you need to be very aware of the cleanliness level you are starting with to avoid issues after product is introduced into the field relating to contamination. A localized extraction of various via sizes on your prototype boards and ion chromatography of solution can give you the information you need to determine if your supplier is effectively rinsing off all process residues and lowering the risk of failures. At that point the decision can be made to either rewash the boards with some sort of saponifier and retested to assess via cleanliness. Common sense would tell us that if there are issues with microvia contamination the answer may be to plug them and assume that the residues won't leach/outgas onto the surface of the assembly but at the same time it needs to be noted that if contamination levels, even in plugged vias, are high enough corrosion can still occur within the via.

Follow Up Analysis

More via test boards from other suppliers will be analyzed in the same manner in a round robin type blind study to determine if this issue is widespread across the bare board industry. Step two of this DOE will also include all of the aforementioned unknown parameters to determine if those play an equally large part in microvia contamination. Different finish plating types will also be looked at to include standard and lead-free HASL, imAg, and ENIG.

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Presentation Overview

- Background
- DOE
- Data Findings
- Conclusions
- Recommendations
- Next Steps

Background Overview

- APEX 2009: *Pockets of Contamination that are Causing Field Failures & How to Avoid Them*

- Question: How clean ARE vias after normal processing and how clean SHOULD they be?

Background: Microvias

Per IPC T-50 rev H Terms and Definitions

Microvia (Build-Up Via)

- A blind or subsequently buried hole that is < 0.15 mm [< 0.006 in] in diameter and formed either through laser or mechanical drilling, wet/dry etching, photo imaging, or conductive ink-formation followed by a plating operation.

Background: PTH VIP Definition

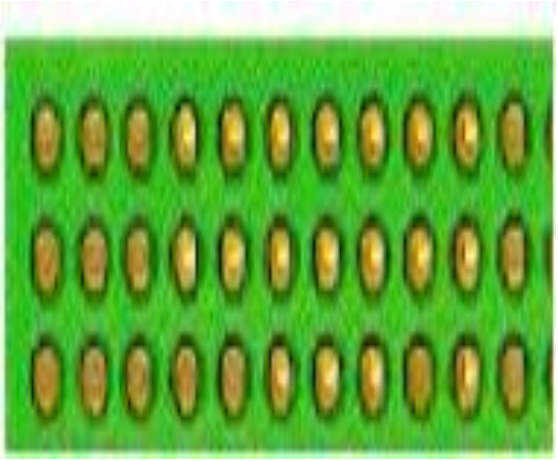
- The structure of a PTH VIP is a copper clad substrate that is drilled and plated with copper from top to bottom of the board. To construct a PTH VIP, a hole is drilled through the pad and then filled with epoxy. Once the epoxy is cured, excess epoxy is removed, and the via is plated with copper on both the top and the bottom. *(Source: Introduction to VIP Board Design – Intel – 2008)*

Background: Via Examples

(Source: Introduction to VIP Board Design – Intel – 2008)

Background: Plated Thru-Hole Via in Pad

- Solder pad is directly over the via



Background: PTH VIP Advantages

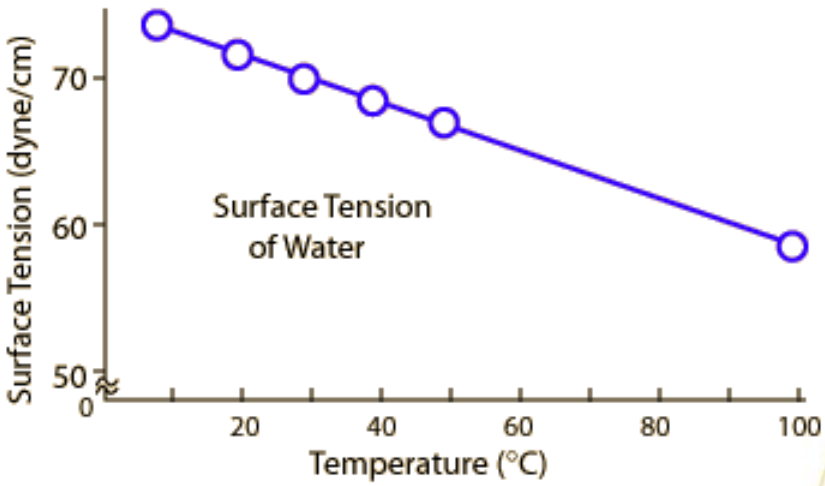
- Smaller pad saves board size and weight
- More chips in less space
- Shorter pathway improves electrical performance
- But…can these advantages be attained without sacrificing quality & reliability?

Background: PCB Manufacturing & Link to PTH VIP

- Heated DI water after etch
- Acceptable for larger vias, but still good enough with shrinking via diameter?
- If not acceptable, what cleanliness levels should be required of PCBs?

Background: Surface Tension of Heated DI H_2O

- Is it too high to flush etchant residues from microvia sites?
- Would saponifier aid this potential problem?



DOE

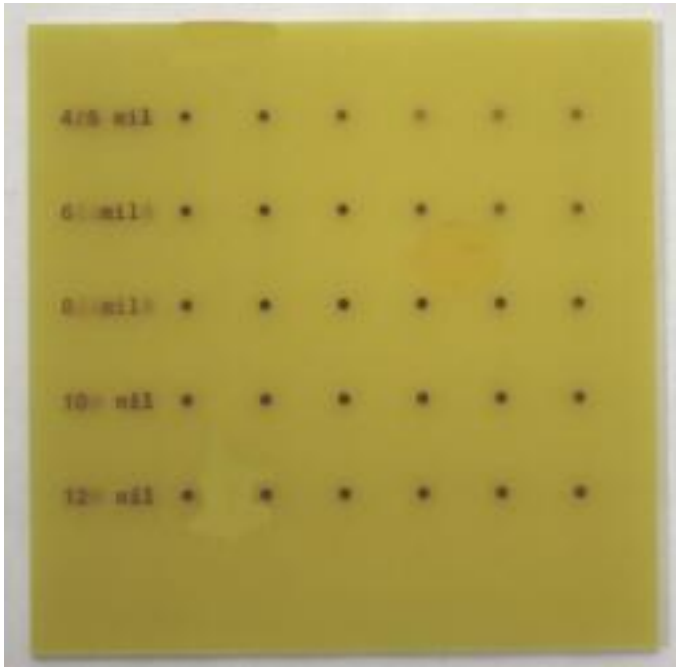
- Blind study to explore typical levels of via cleanliness after PCB processing

- 5 via sizes, 6 of each sized via
  - 4/5
  - 6
  - 8
  - 10
  - 12

DOE: Test Vehicle

The test vehicle used is a simple PCB with 5 different via sizes-6 per row, standard drill process

- 4/5 mil
- 6 mil
- 8 mil
- 10 mil
- 12 mil



DOE: Testing Process

- 25 repetitions of each via size
- Bare board reference area
- Bottom of vias covered with Kapton tape
- Localized extraction of the vias
- Ion chromatography of solution

DOE: Test Matrix

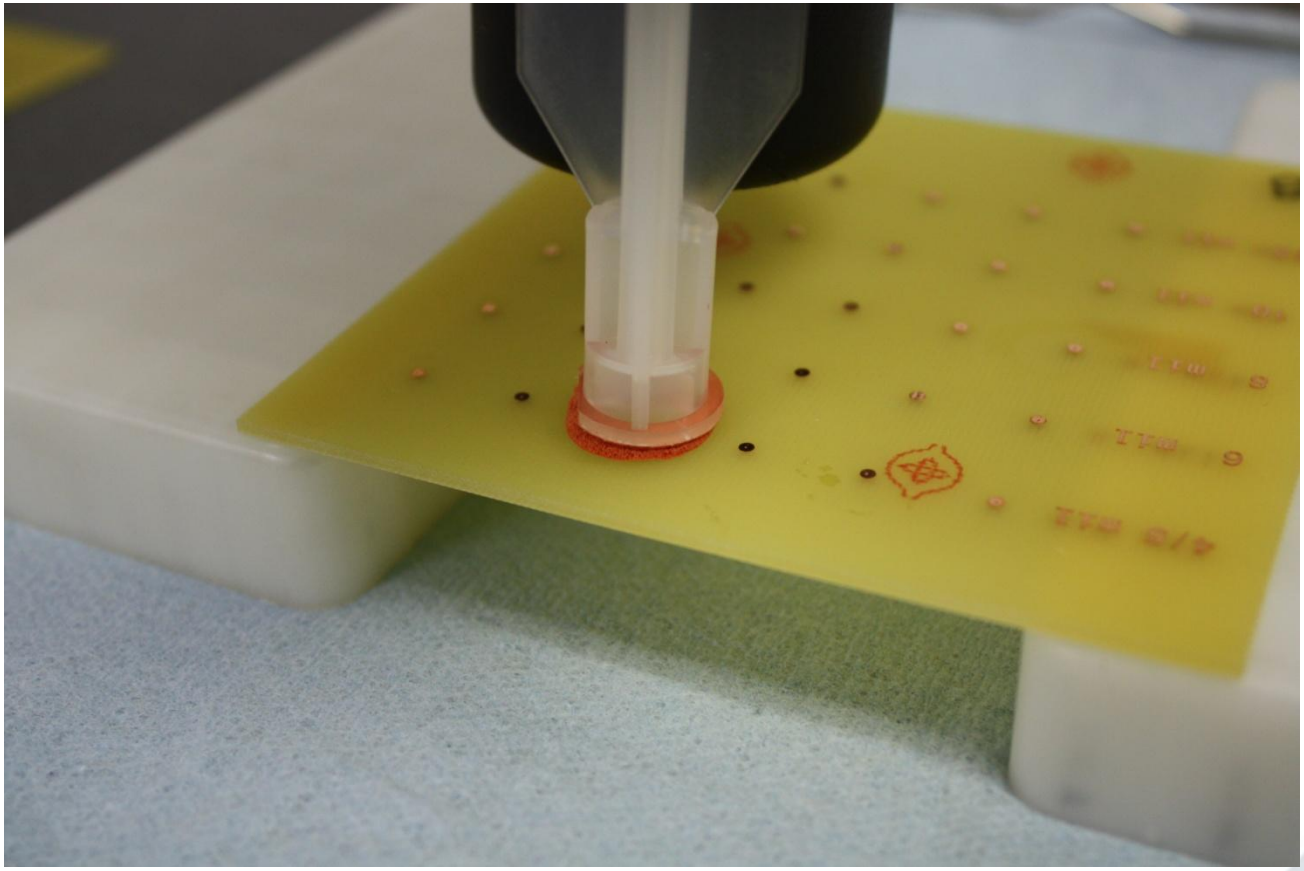
Bare Multiple Via Test Board	Via Size	# Of Test	Results
Assessment #1	4/5 mil via	25 repetitions	Test Results Table #1
Assessment #2	6 mil via	25 repetitions	Test Results Table #2
Assessment #3	8 mil via	25 repetitions	Test Results Table #3
Assessment #4	10 mil via	25 repetitions	Test Results Table #4
Assessment #5	12 mil via	25 repetitions	Test Results Table #5

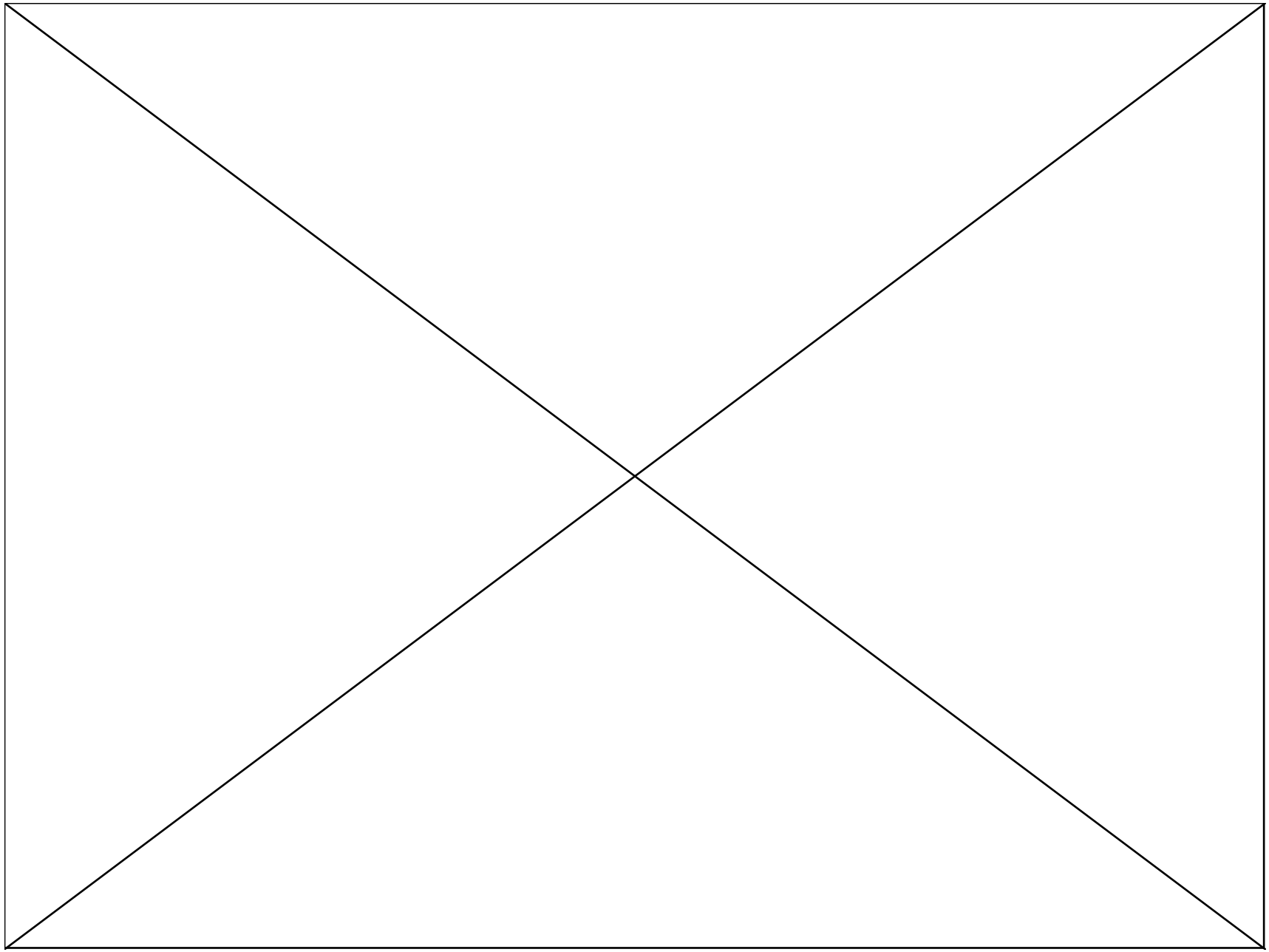
DOE: Test Parameters

- Vias were flushed with approx 2.5 mils of heated 18 megohm DI water over a course of 9 steam cycles with 20 seconds of soak time to solubilize process residues

- DI extraction is brought to 265^{o}F at source and is approximately 180^{o}F at board level

DOE: Localized Sample Extraction





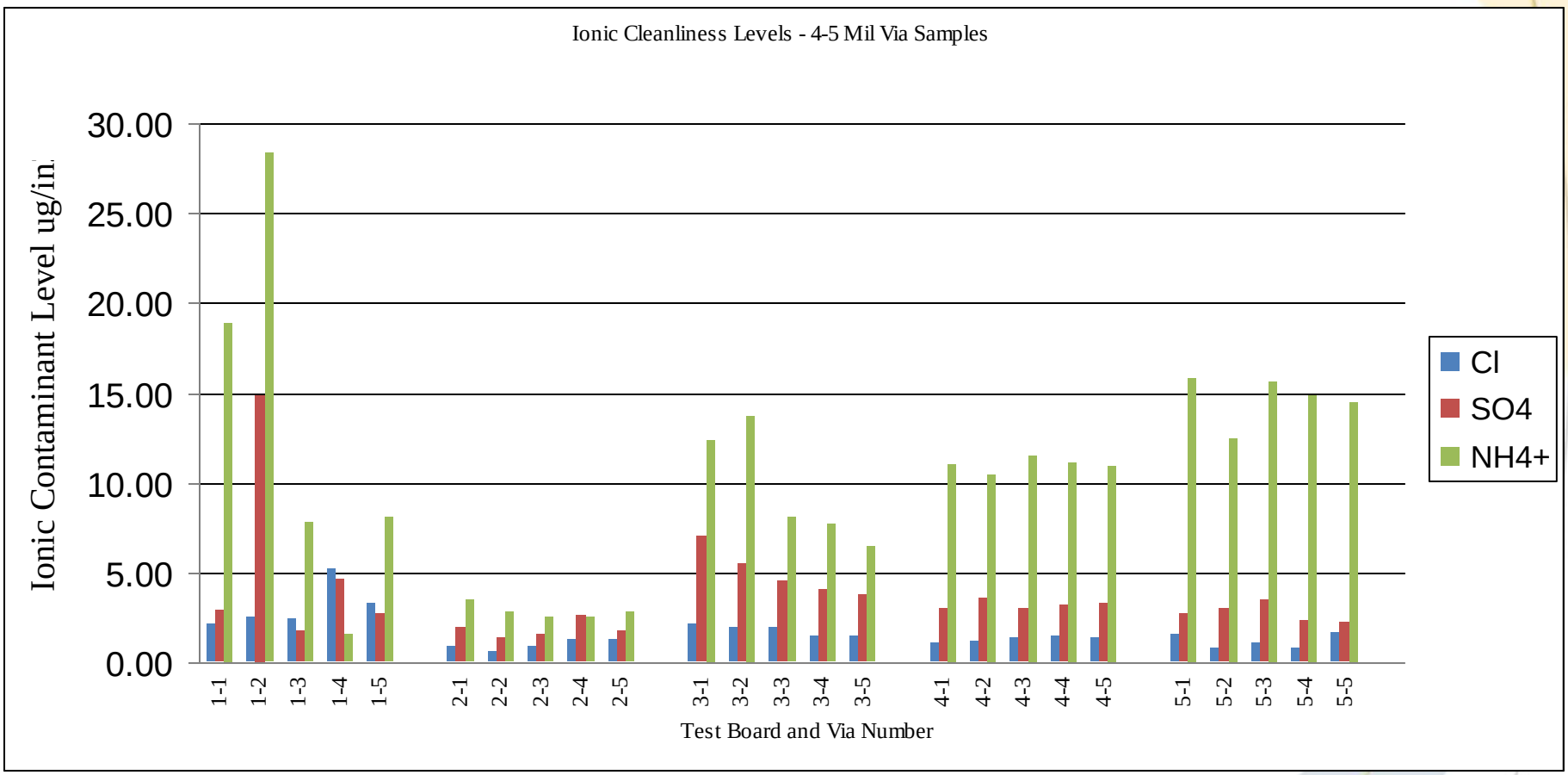
DOE: Ion Chromatography

- IPC-TM-650 2.3.28
- Typical etchant materials include ammonium persulfate, ferric chloride, sodium persulfate
- Hypothesized anions of concern:
  - Ammonia
  - Sulfate
  - Chloride

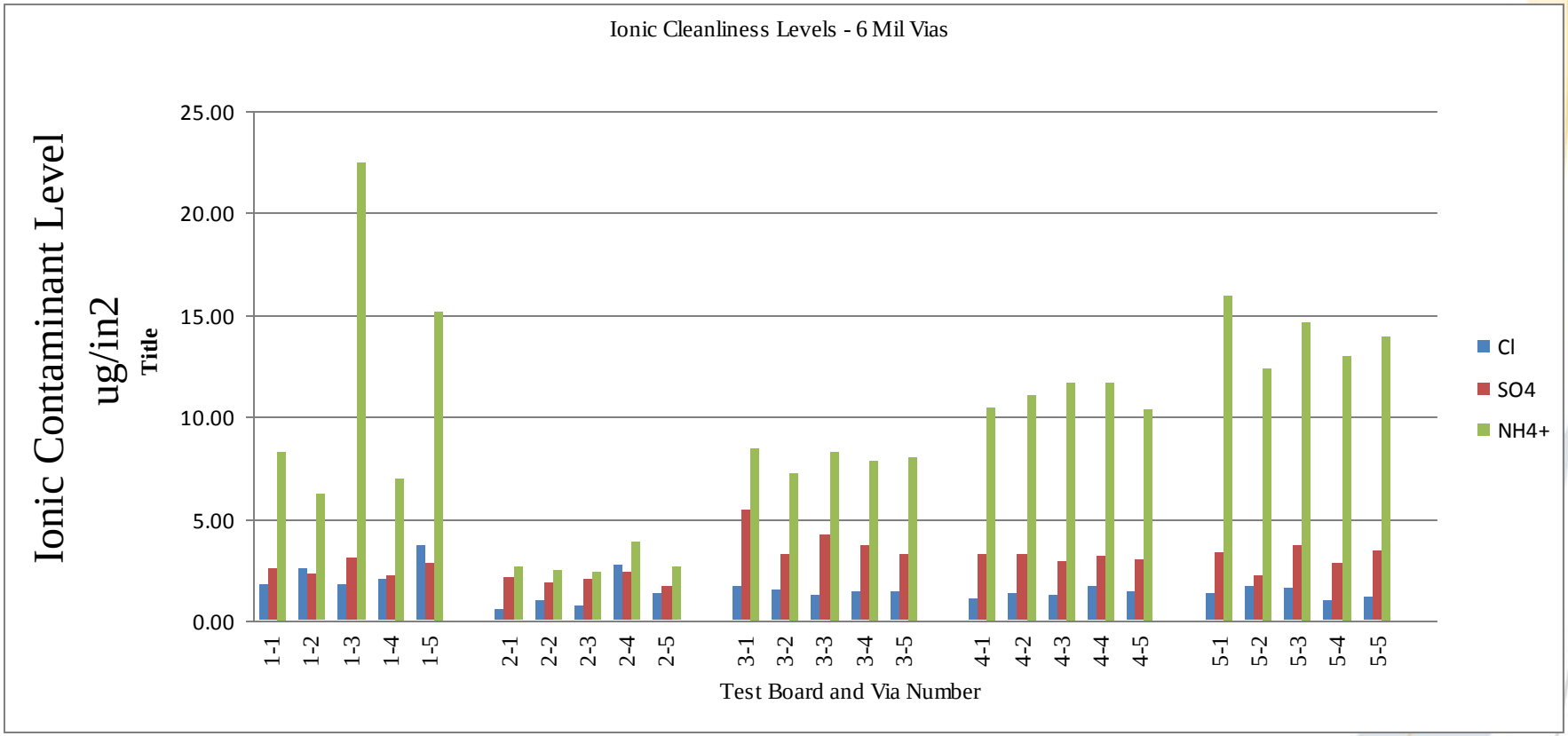
DOE: Ion Chromatography

- Dionex ICS 3000 IC system & Chromeleon software
- Controls & blanks performed before testing using NIST-traceable standards for calibrations
- 1.5mL sample of each test site's extracted solution analyzed using 1.7mM sodium bicarbonate/1.8mM sodium bicarbonate eluent

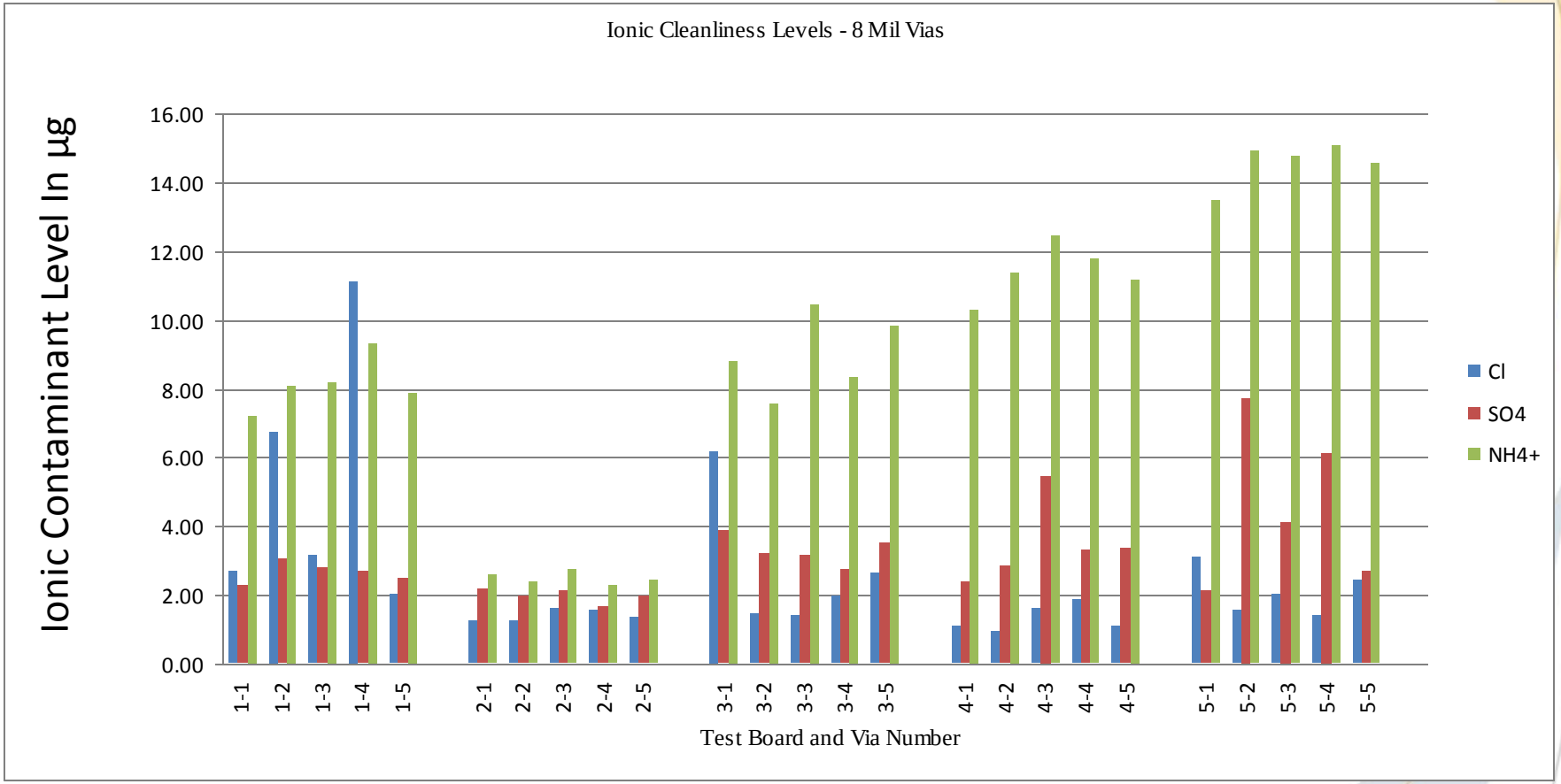
Data Results: 4/5 mil Vias



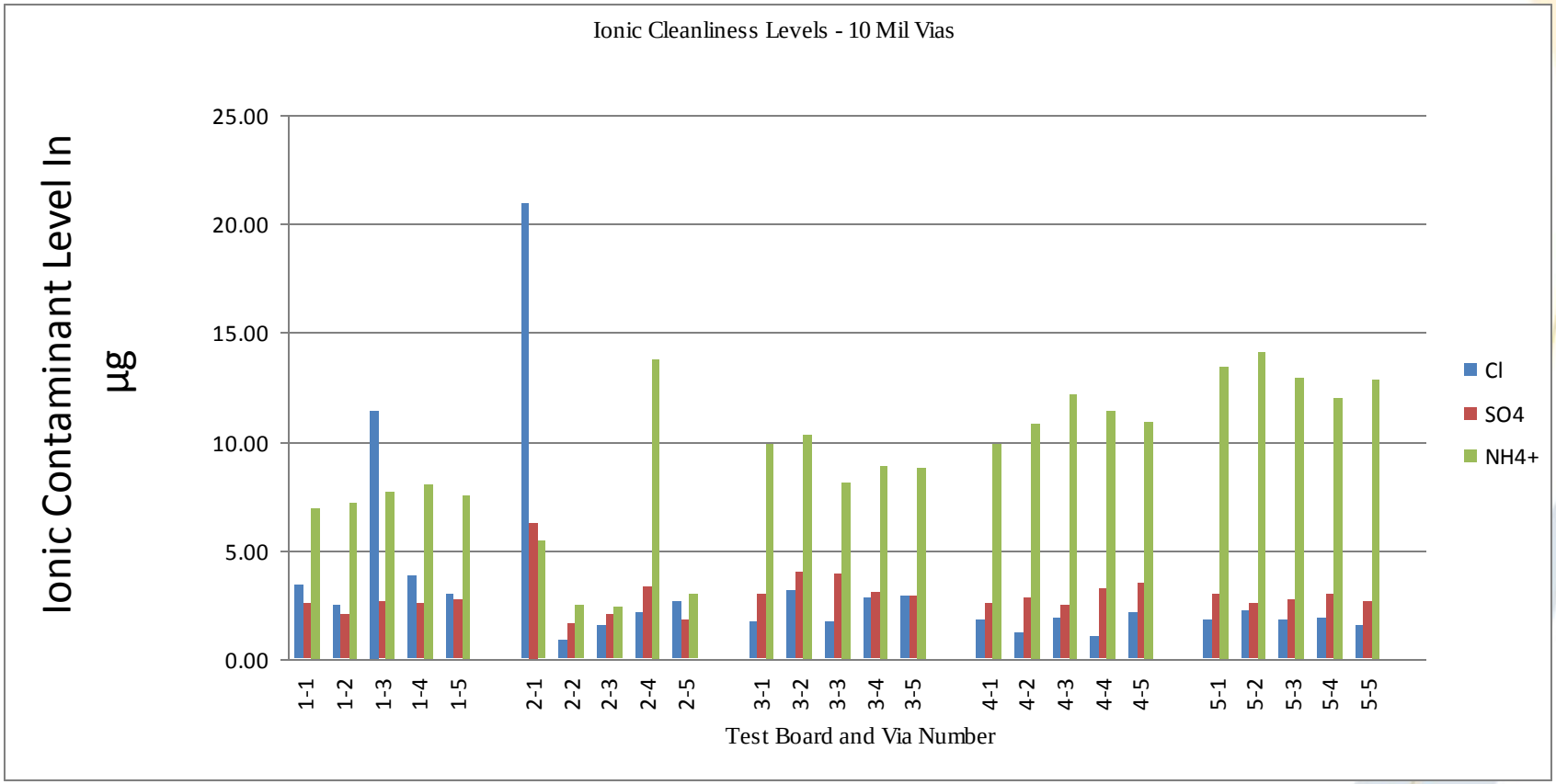
Data Results: 6 mil Vias



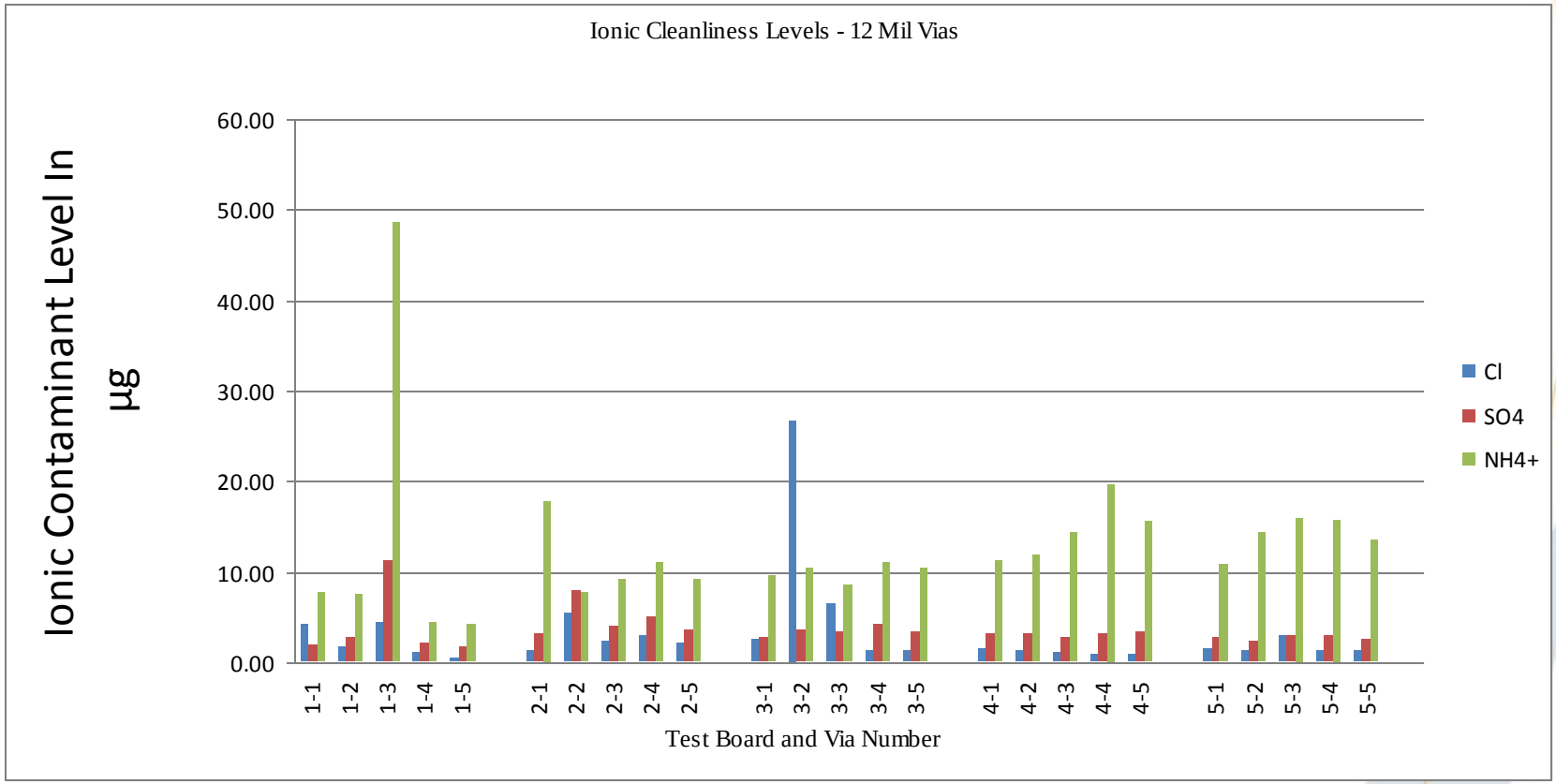
Data Results: 8 mil Vias



Data Results: 10 mil Vias

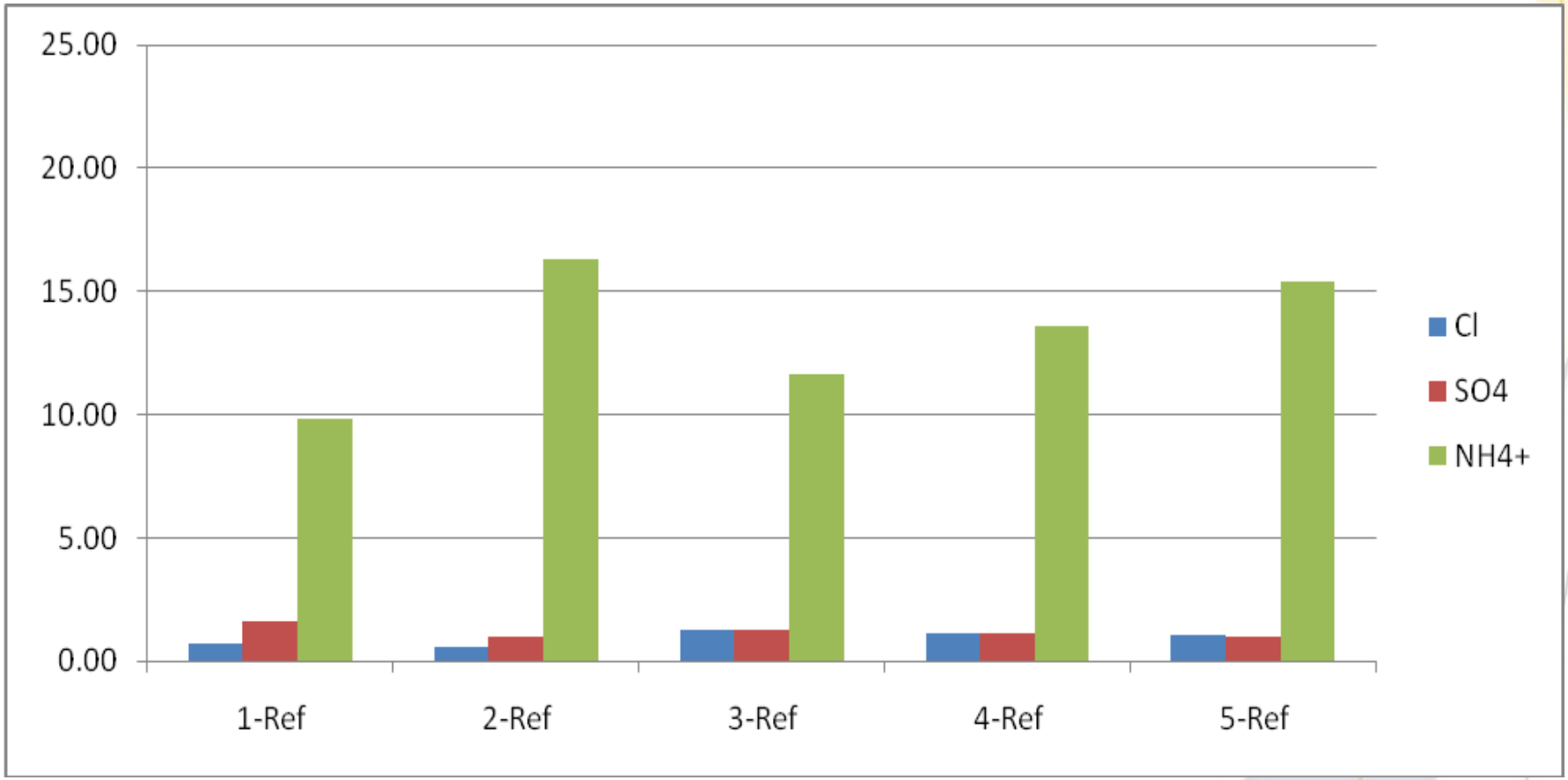


Data Results: 12 mil Vias



Data Results: Bare Board Reference

Table 6-Bare Board Reference Areas Away from Vias



Data Findings Summary

- Bare references show low chloride & sulfate; fairly high ammonium
  - Residues confined to vias & not outside factors
- Contamination levels unexpectedly vary from test board to test board
  - Proves inconsistency of rinse not only on differing via sizes but also boards in same lot
- 10 to 12 mil vias generally cleaner

Conclusions & Recommendations

- Microvia technology requires keen awareness of starting cleanliness levels
  - More critical if open & placed under low stand-off components

Conclusions & Recommendations

- Many cleanliness factors must be considered when examining PCB suppliers including:
  - Bath life change out indicators
  - Rinsing temperature
  - Incoming rinse water quality
  - Belt speed
  - Rinse pressure
  - Ongoing cleanliness monitoring

Conclusions & Recommendations

- Perform localized extraction of various via sizes on prototype boards
- Follow up with ion chromatography to determine if supplier effectively removes process residues
- Remediate negative findings by rewashing with saponifier & retesting
- Don’t assume plugging or tenting vias will solve problems
  - High contaminant levels can still leach/outgas & cause corrosion

Next Steps

- DOE to be expanded on by obtaining test boards from other suppliers
- Analysis will be done in round robin blind study format to determine if these findings are widespread
- Examine additional parameters including finish plating & other unknown parameters
- Come back next year to hear the dramatic conclusion…..

Thank You!

- Questions?