Using DMAIC Methodology for MLP Reflow Process Optimization

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Abstract
The widely publicized and studied implementation of lead free solders has led to increased scrutiny on the solder joint formation for surface mount technology electronic components. During the lead free transition packaging technology for power semiconductor components increasingly embraced molded leaded package (MLP) technology. Due to the application demands of power devices, namely temperature control and reliability, many end users have placed considerable emphasis on process void minimization. Experiments have shown that increasing the quantity of solder paste printed will often minimize process voiding, but incidences of solder balling and beading often increase. Due to their comparative complexity, multi-die MLPs have shown to be more sensitive to solder process design and control. This created the need for a thorough investigation of solder process parameters, and a method to collect and analyze the data from a set of experiments to optimize the process. No previous process found by the experimenters was found to meet the needs of the problem.

Demonstrated in this paper is a six sigma based methodology for developing a rigorous design of experiments for determining the best process for surface mounting a 6x6 DrMOS MLP component. Critical factors will be identified and treated statistically using DMAIC methods.

Introduction
The use of six sigma tools and processes has allowed companies to take many aspects of their businesses to the next level. As a toolset, six sigma methodologies were originally forged in the furnace of manufacturing. This makes the methodologies particularly applicable to surface mount process optimization.

Concurrently, there have been many advances in power semiconductor packaging and applications technology. The insatiable demand for both miniaturization and increased feature sets in consumer electronics has lead to a need for power semiconductor devices to increase power handling and improve power density in designs. With this trend, Intel[2] created specifications for 6x6mm DrMOS products, power semiconductor devices that see the copackaging of a MOSFET gate driver IC, and the high and low side MOSFETs used for synchronous power rectification commonly employed in computing applications. This specification is specific that there are to be three Die Attach Pads (DAPs) and 40 external pins for I/O. Devices based on this specification (though not always complying) often have maximum current ratings in excess of 30 amperes, and switch at frequencies up to and exceeding 1 megahertz. This places a demand on the system for excellent thermal and electrical performance, necessitating high performance execution from circuit to board to reflow process design.

Many engineers and technicians have applied six sigma tools to electronics manufacturing. A search of the literature however did not show many results for applying this methodology to a multi-DAP MLP package which provide their own unique challenges. This paper will demonstrate how to quickly optimize the reflow process for a multi-DAP package, but the methodology will be applicable to any package type.

Power semiconductor suppliers often are requested to support customers at many steps of the design process. As a new design ramps up through qualification builds, the customer may ask the component supplier to help with the optimization of the surface mount process. This can be a very time sensitive request, and is often at a critical juncture in the new product phase for the customer, initial ramp to release. As delays at this point can become widely publicized and commensurately costly, often the customer needs resolution to what can be a difficult problem with interaction effects of both their manufacturing site and the component, very quickly. Correct application of six sigma tools and methodologies can allow for the handling of large designs of experiments and statistical analysis, with production improvements able to follow rapidly. The organization the tools provide to the data allows for faster design of experiment (DOE) turn-around times, and improved customer acceptance of changes to their process.

The Challenge
Every project starts with the formation of a team to solve a specific problem. The problem initiating study here was a 6x6 DrMOS ready to go to market experiencing low, but persistent, levels of solder beading created during reflow as a customer was completing qualification builds for an important new product for their company.

Solder beading, the formation of solder beads not part of the desired solder joint, create a shorting risk and can be a particularly dangerous problem with power electronics. Due to the high level of power, a short can cause catastrophic damage to surrounding components and even the printed circuit board (PCB).

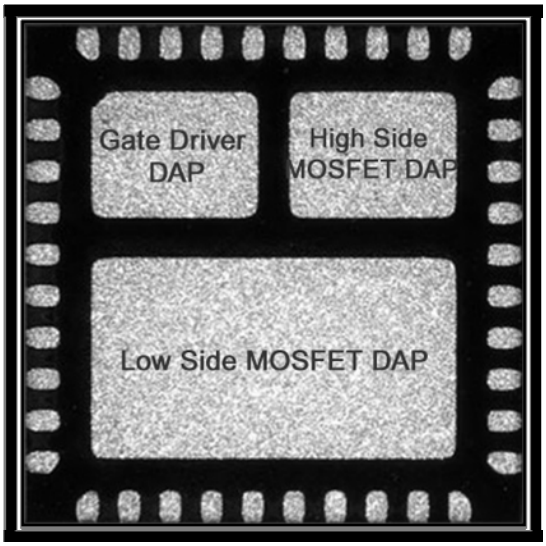


Figure 1: 6x6mm DrMOS

Solder beading is most often attributed to printing excess solder on the PCB. The natural response is to reduce the quantity of paste printed. Reducing the quantity of paste printed can result in an increase in voiding, especially on large solderable areas created for improved thermal performance such as the three seen in the 6x6 DrMOS package design. As previously mentioned, this product may see the repeated application of 30A with switching in the megahertz range creating high heat loads on the solder joints, and temperature cycling of the component.

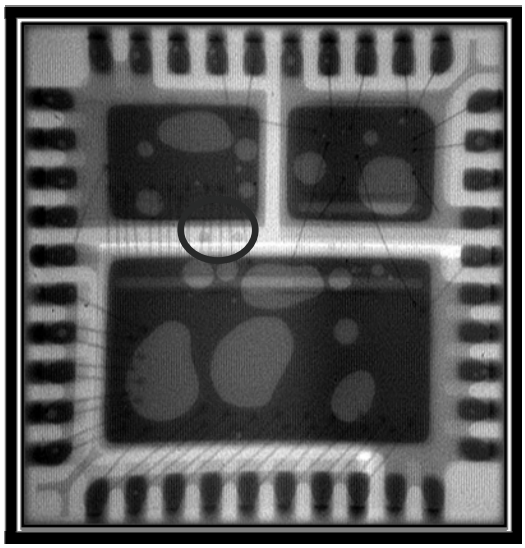


Figure 2: X-Ray Image with Solder Bead

Solder Joint Formation and Strength

For the typical surface mount technology (SMT) component, the solder joint has the duplicitous role of providing the mechanical joint as well as the electrical connection to the system. The mechanical joint also is multi-functional, with the solder joint providing the key heat path out of this type of component, as well as the bond strength to hold the component to the printed circuit board (PCB) through the temperature cycles seen in operation. Compared to small outline (SO) packages, molded leaded packages provide a larger die to footprint ratio, allowing them to have higher current densities. The gull wing leads used in SO package designs create a larger package footprint, but it was not designed in to electronics packaging by providence. The gull wing lead uses a formed geometry that allows for board induced stresses to dissipate before reaching the package. The stress created in these applications is due to the differing coefficient of thermal expansion for all of the materials in the system. The FR-4 PCB, the copper design and thickness on the PCB, the mold compound of the package, the silicon die internal to the package, all expand at different rates with heat.

This creates a stress that bows the board and through thermal cycles due to power and load cycling experienced in the application, fatigue wears out the solder joint to the PCB. The MLP package does away with this gull wing lead in search of higher performance, and higher die to footprint ratios, placing the burden of controlling board stresses on the system designer and SMT process engineer.

Much has been written about the impact of voiding on Ball and Column Grid Array packages, but less on MLPs. While there are conflicting current industry specifications for voiding on BGAs (25 and 30% distributed throughout the joint), there is no attendant specification for MLPs. There is also debate in industry about the effects of voids on solder joints. There are claims that voiding in solder joints actually provides a type of strain relief and stops the propagation of cracks in solder joints. Still others contend the crack will continue on after passing the crack front passes the void location. Stress will concentrate at corners of leads, and an unsoldered lead corner can lead to premature solder joint failure through early crack initiation and propagation. Voiding can lead to a decrease in thermal performance. There are papers suggesting that voiding up to 50% has a limited impact on thermal performance for these types of packages. These discussions are beyond the scope of this paper, but the SMT process engineer should do their due diligence to understand the interplay of these causes and effects.

With so many critical functions impacted by the solder joints it is no wonder SMT engineers are spending more time analyzing and verifying soldering parameters in qualification builds, especially for devices like MLP where process control is critical for avoidance of solder errors due to a lack of ability to visually check solder joints on the internal DAPs.

DMAIC Methodology and SMT

Six sigma for process improvement often uses the Define Measure Analyze Improve Control (DMAIC) acronym. This is an apt description of the methodical process of continuous improvement advocated by practitioners of six sigma in the manufacturing environment. What follows is the description of how it was applied to SMT processing allowing a speedy optimization of a complex reflow process, with focus on balancing the output responses of solder voiding and solder beading.

Define

The first step is to define the problem. In the scenario described for this paper, the problem was solder beading at the three inner die attach pads. The timeframe given to solve the problem, and the customer's corporate design constraints related to PCB design meant that changes to the solder stencil were easily practicable, changes to the oven profile difficult to make as there were larger and smaller components on the board assembly driving the oven profile, and finally, board redesign would have meant a loss of the design win as the delay caused by a PCB redesign could have triggered the designing out of the DrMOS module.

With the problem defined, the experiments could be designed based on the experimenters' knowledge of the system gleaned from voice of the customer interviews and experience in the process. From previous experience it was known that the most likely cause of the solder beading was excess solder. It was also known that reducing the amount of printed solder could cause voiding. It was unknown if the geometry for a given quantity of paste may have an effect, and whether the solder printed on the edge pins could also have an effect on solder beading at the inside DAPs.

The first DOE was a six run experiment including an experimental run mimicking the customer's current process of record, and a fractional factorial experiment designed to quickly get data and report back to the customer whether or not the problem could be replicated, and changing the stencil design could affect the outcome. Using the data from this first experiment which did replicate the problem and showed differing results with changing quantities of paste printing, three subsequent full factorial DOEs, a thirty run and thirty-six run, along with a final twelve run experiment were employed to get fine resolution on a solution. All DOEs were designed using the statistical package and fully randomized.

Measure

The most frequently used systems of solder joint measurement in SMT processing are visual and x-ray. In this experiment the critical output responses for the experiments would be the solder voiding and beading. Because visual examination of the three DAPs, which had the greatest concern in this study, is impossible, x-ray testing was necessary for measurement. Unfortunately the capability of gathering the voiding percentage at the pad/pin interface for each sample was not available. Attempts to estimate voiding percentage with "golden samples" proved unworkable after a basic gauge study of redoing the same samples three times proved unreliable. Therefore solder voiding at each of the three DAPs were rated on a scale of "1" to "3", "3" being the worst, "1" the best. "3" was an unacceptable level of voiding, incomplete wetting of the corners of the DAP, or distributed voiding of over 30%. "2" was an acceptable solder joint with voiding estimated between 15 and 30%. A "1" would have voiding below 15% and was considered ideal. Solder beading was also measured by counting the number of beads created in reflow on the x-ray pictures. Solder voiding and shorting of the edge pins was noted and counted.

Analyze
The analysis of the data is where the emphasis of six sigma statistical methodology allows the experimenter to be more efficient. Used for this specific data was JMP[3], but there are many other statistical packages the experimenter can use. T-testing of the null was used to identify important factors, and the prediction profiler used to predict optimal combinations based on optimizing the output responses. These optimal combinations were then used to identify combinations of factors to try in successive DOEs. Individual factors and interaction effects were examined statistically.

Improve
Using the results of successive DOEs learning were incorporated in the next DOE permitting a more optimized process definition with decreasing levels of granularity as the experiments progressed. The experimenters had frequent contact with the customer communicating results as they became available. Through the successive experiments, it was hoped an improvement in the process would make the process ready for release to manufacturing.

Control
It was beyond the scope of this study to identify control methods for the customer's manufacturing process. However, identified in the experiments was the importance of paste printing quantities and locations. Controls should be enacted to ensure these important parameters have monitoring, and ideally are error proofed to ensure process control. It has been estimated that 60% of all SMT assembly errors are created during solder stencil printing. An optimized process and control system especially true for MLP type packaging where the most effective type of measurement of errors is time intensive and costly high resolution x-ray. Ideally the process could be made so well controlled real time x-ray of every MLP placement would not be necessary in volume production.

DOE #1
In the case studied here, the problem was unacceptable levels of beading at the inner DAPs for a 6x6 DrMOS module at a customer. Because it was late in the product development cycle, the business constraints favored easily changed parameters as the "dials to twist". The fastest and cheapest parameter to change in the process is solder stencil design. Fortunately, solder stencil design can have dramatic effects on surface mount processing.

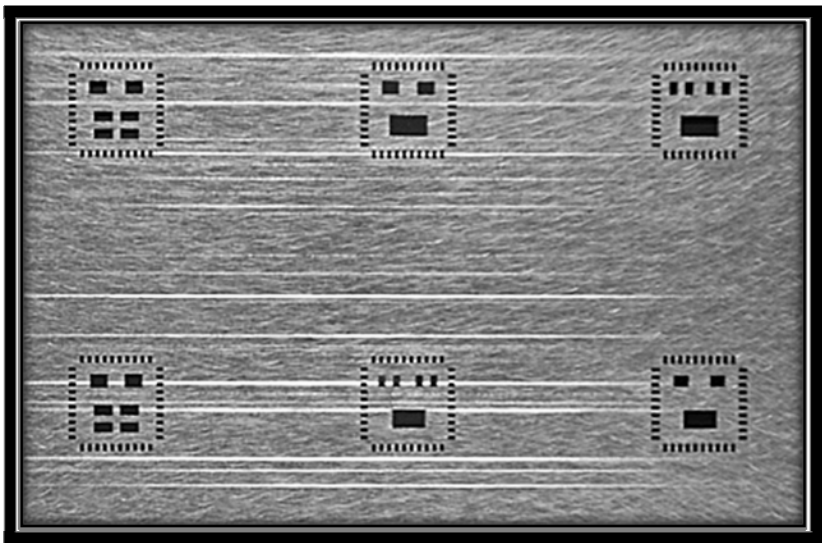


Figure 3: Solder Stencil Apertures

Before the first experiment was designed, there was a meeting of stakeholders between the customer and the supplier team. A set of questions was prepared before this meeting to ensure the team had all inputs needed for clear voice of the customer collection. It was verified the solder paste stencil could be changed within the business timing constraints. The particulars of the customer's PCB design solder paste stencil and solder paste product used in the process were all determined for use in the first experiment which would be conducted at Fairchild[1]'s Surface Mount Technology Applications lab. A six run partial factorial design with the customer's process and five different combinations of solder stencil openings, and one extra run with via in pad, was agreed on to determine if the problem could be replicated to allow the team to work on improving results. For this, and all successive DOEs, a PCB was designed with localized copper trace design, thickness and pad finish to mimic the circuit board used in the customer's application. This first DOE intentionally used coarse changes to investigate whether or not the factors would change the output responses. The solder paste quantity printed on the high side and IC DAPs were reduced by 23 and 40%.

Trials with a reduction in the paste printed on the low side by 30% were tried, along with 1:1 and 70% coverage on the outer forty I/O pins. This experiment would verify if the team was adjusting the right factors and give confidence for communication with the customer for a path to expeditiously resolve this challenge.

Analysis of the x-ray data showed the ability to replicate the customer's problem of solder beading in similar locations with the test coupons, and had also been able to alter the output responses with the experimental runs. The printed paste volume was reduced to the point beading was totally eliminated in some combinations, yet voiding rose to unacceptable levels. Refinement of the process was called for.

DOE #2

With boundaries set for the paste quantities set, this DOE was designed as a full factorial study using five factors, each with two levels. This study would yield thirty-two runs, however the PCB design only had thirty locations. Two combinations were chosen for elimination from the array to allow the use of the PCBs already in stock. The statistical package was used to randomize the experimental locations for DOE's 2, 3 and 4. The factors altered in this DOE were 40% and 23% reduced paste printing on the high side and IC DAPs, and reduced paste printing on the low side by 11 and 30%. The paste was previously printed in one rectangular block, it was decided to study if splitting the paste into multiple blocks for each DAP location, and high and low sides would yield better performance with lower voiding and beading. Trials were made with and without split solder paste. Finally it was decided to study if reduced printing of paste on the outer I/O pins would lead to lower beading. Being a full factorial study, interaction effects could also be studied. Interaction effects are when two factors separately may not have an effect, but together may. Nine panels were built yielding nine data points for each combination.

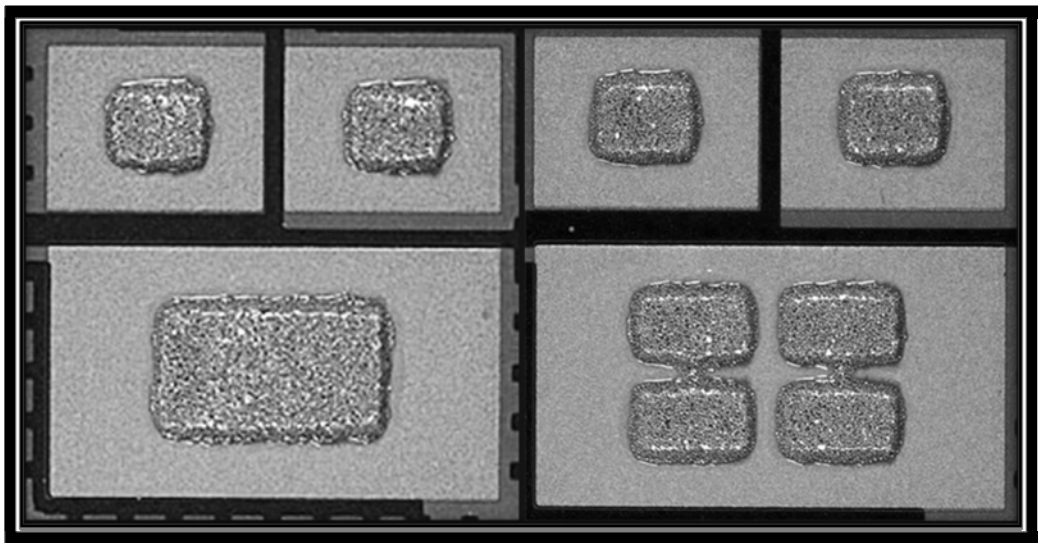


Figure 4: Printed solder paste, same area coverage solid blocks and split blocks.

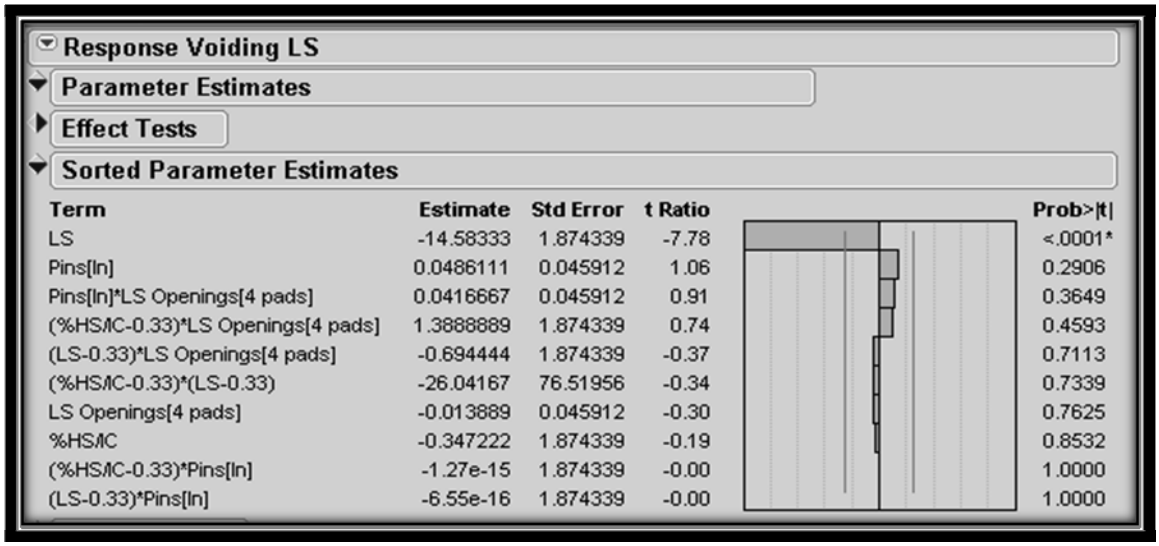
Statistical analysis of DOE #2 was completed by entering the x-ray results into the statistical package. The data was sorted by board location and panel number for all DOEs. This allowed the analyst to determine if there were any maverick panels which could skew the data. The data was modeled and t-tests were used to look for the statistically significant factor for each location on the PCB. There were no interaction effects, simplifying the optimization of the process for the future. It was found printing 1:1 pad size to solder aperture size yielded shorting, for all future experiments the I/O pins would have reduced prints of approximately 70% coverage. An example of the statistical analysis applied is shown below, testing against the null for factors related to voiding at the low side location. In a pattern that would repeat itself, DOE#2 resulted in the learnings that high side and driver integrated circuit (HS/IC) coverage was a statistically significant factor in both HS/IC voiding and solder beading. Low side (LS) solder coverage was statistically significant for LS voiding, and it was found splitting the solder paste print on the low side improved voiding performance.

DOE#3

The data from DOE #2 showed promising direction with the split solder printing, but did not find a combination deemed optimal by the team. A meeting with the customer and related stakeholders allowed for communication of the data from DOE#2. The customer found the statistical data particularly compelling, and expressed a preference for the solid block high side solder print, eliminating this factor from further study. DOE#3 would attempt to further fine tune the process using a new PCB design allowing thirty six locations. The factors studied in this full factorial DOE were a two level study of the split low side DAP solder print design, into four and six squares. Two three level factors were specified for DOE#3. For the

low side DAP 30, 19 and 11% less solder volume than originally printed was used. For the high side and IC DAPs, 30, 23 and 16% less paste than the customer's process of record was printed. A proprietary geometry was tried on the IO pins, with two levels used in this DOE, with the geometry rotating 180 degrees. This yielded thirty six combinations; eight panels with a trial for each combination, were built.

A similar data analysis to DOE#2 was used. Again no interaction effects were identified. It was learned that printing four or six squares of solder paste on the low side did not make a statistically significant difference on voiding performance. Because having only four holes in the stencil would allow for a more durable stencil in production, this was chosen as the optimized recommendation. It was found that rotating the solder paste geometry on the outer I/O pins had no statistically meaningful differences, so the original, non-rotated orientation was chosen. It was noted that the bottom end of the solder paste volume did not seem to be defined. It was decided to do one more DOE to study this further.



Term	Estimate	Std Error	t Ratio	Prob>|t|
LS	-14.58333	1.874339	-7.78	<.0001*
Pins[In]	0.0486111	0.045912	1.06	0.2906
Pins[In]*LS Openings[4 pads]	0.0416667	0.045912	0.91	0.3649
(%HS/C-0.33)*LS Openings[4 pads]	1.3888889	1.874339	0.74	0.4593
(LS-0.33)*LS Openings[4 pads]	-0.694444	1.874339	-0.37	0.7113
(%HS/C-0.33)*(LS-0.33)	-26.04167	76.51956	-0.34	0.7339
LS Openings[4 pads]	-0.013889	0.045912	-0.30	0.7625
%HS/C	-0.347222	1.874339	-0.19	0.8532
(%HS/C-0.33)*Pins[In]	-1.27e-15	1.874339	-0.00	1.0000
(LS-0.33)*Pins[In]	-6.55e-16	1.874339	-0.00	1.0000

Figure 5: Statistical chart showing T-testing the results of DOE#3 for Low Side DAP voiding, including interaction effects.

DOE#4

After presenting the data from DOE#3 to the stakeholders, it was decided one more DOE was warranted. This DOE would reduce paste until voiding was too high. The customer again expressed a preference for not splitting the solder paste print on the low side DAP, so this factor was added to the study. It was decided to define three levels of solder coverage combinations. Two of the paste combinations yielded equal area coverage ratio on the high side, IC and low side DAPs. A third paste combination was tried with very low solder coverage as suggested by a customer experiment. A two level factor split or no split low side solder print, and finally a two level factor for reflow profiles, "hot", at the high end of the recommended process window, and "cold", at the low end of the process window. Because the reflow profile cannot be changed across panels, this factor was not included on the same panel it had to be done across panels.

Analysis showed that splitting the solder paste on the low side was again preferred. Additionally, it was learned that the system was tolerant of swings in the reflow profile within the recommended range of the solder paste with no statistically meaningful difference found between the "hot" and "cold" profiles. Two of the solder paste combinations were tried to see if printing a similar volume in relation to pad area would improve performance by equalizing the thickness of the solder between the three DAPs. The third combination was an attempt to print so little paste voiding was unacceptably high.

Conclusions

Six sigma methods and tools allowed the teams to quickly resolve a complicated problem with eighty four discrete combinations of surface mount process factors. Splitting solder paste prints, varying areas, varying outside pin coverage, and changing the reflow profile were all tried and the effects analyzed. The differences studied were sometimes subtle, which without proper experimental methodology would have been difficult to distinguish as meaningful improvements. The tools gave team members a superior way to set up and organize DOEs, with clear DOE set ups easily communicated between engineers and technicians. At the customer site, the statistical evidence was powerful data to persuade both the customer team members, and their management to make changes. These efforts were not in vain. This product now ships in very high volume across multiple manufacturing sites with no reported failures attributed to the surface mount process.

Endnotes

[1] Fairchild and Fairchild Semiconductor are trademarks of Fairchild Semiconductor Corporation
[2] Intel is a trademark of Intel Corporation
[3] JMP is a trademark of SAS Institute Inc

Works Cited

[1] Amkor, "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages", September, 2002
[2] W. Engelmaier, "Voids in solder joints- reliability", Global SMT & Packaging, January, 2006
[3] IPC, IPC-A-610D, "Acceptability of Electronic Assemblies", February, 2005
[4] R. Perry, D. Bacon, *Commercializing Great Products with Design for Six Sigma*, Prentice Hall PTR, 2006
[5] S. Shina, *Six Sigma for Electronics Design and Manufacturing,* McGraw Hill, 2002

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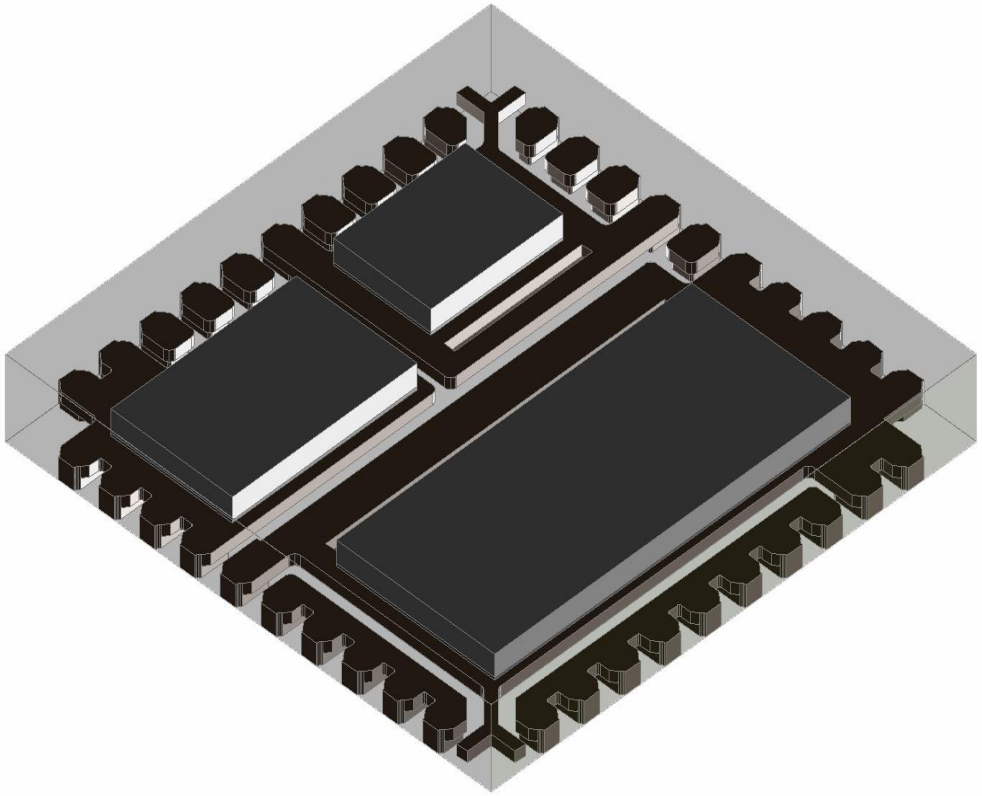
Engineering Manager

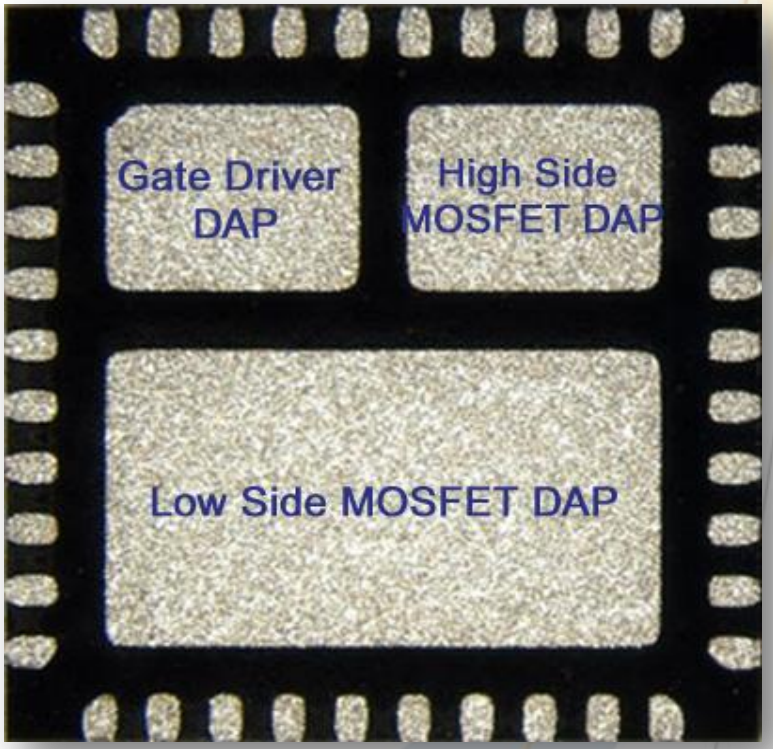
Ever had that call…

Bringing Order to Chaos

- Talk marketing and sales back from the edge
- Turn to your engineer's toolbox
  - DMAIC
  - *Rigorous application of these tools led to a succession of experiments with 84 discrete combinations of factors, within the course of ~2 weeks and successful resolution of the problem.*

Multi-DAP DrMOS MLP





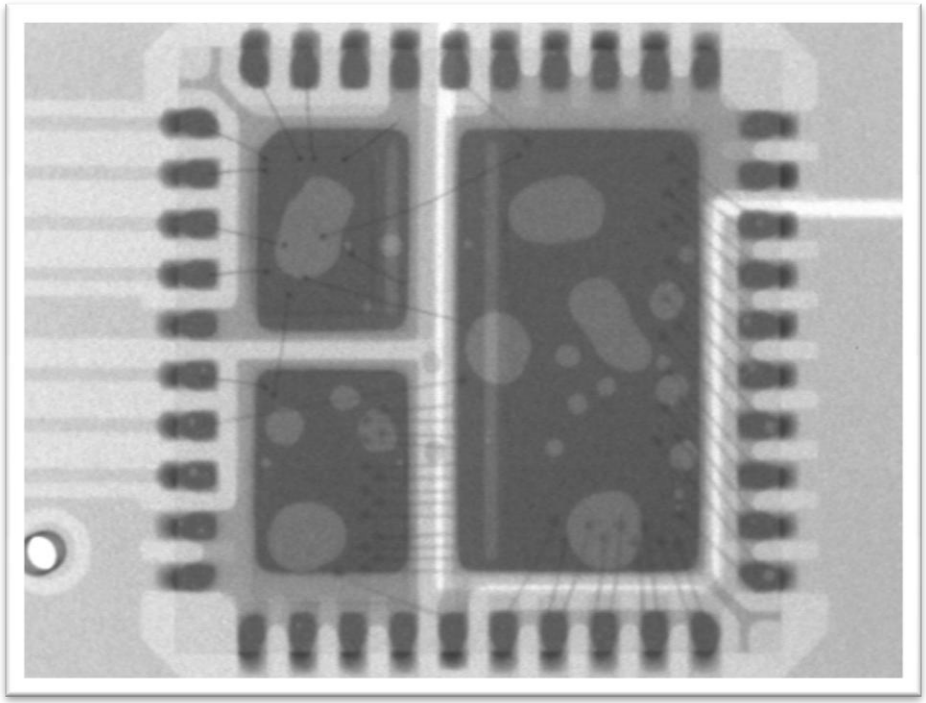
Defining the Problem

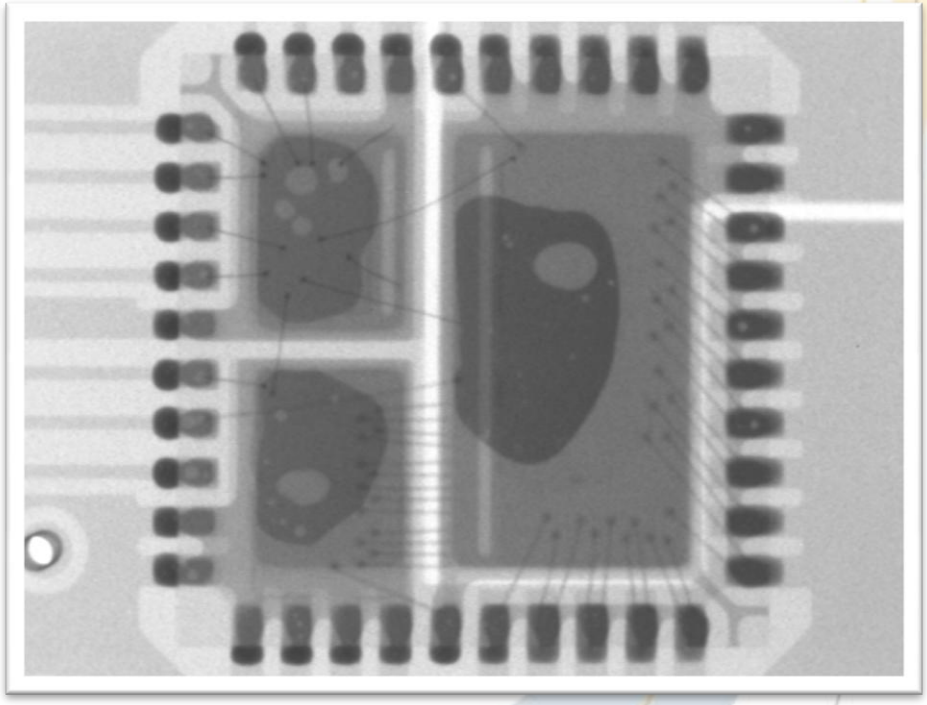
- Initial problem was solder beading/balling during prototype builds at customer site
- JMP used to construct a series of DOEs

Measure

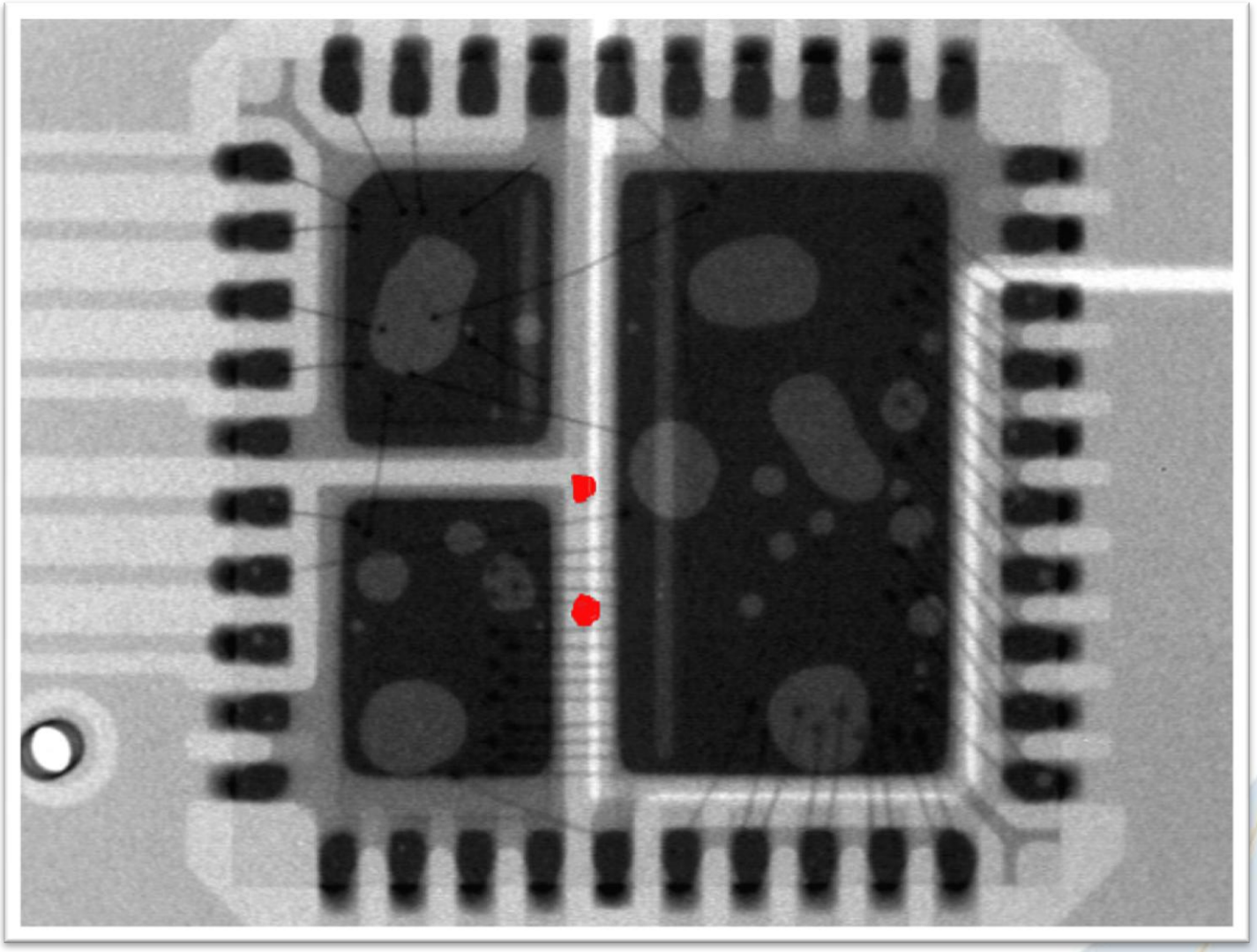
- X-ray inspection used to measure responses during all DOE
  - X-ray equipment/software that could measure voiding as a percentage not available
- Rudimentary gauge R&R performed to assess efficacy of void estimation
  - Not reliable
  - Rating system of 1-3 devised

X-Ray Images of Defects

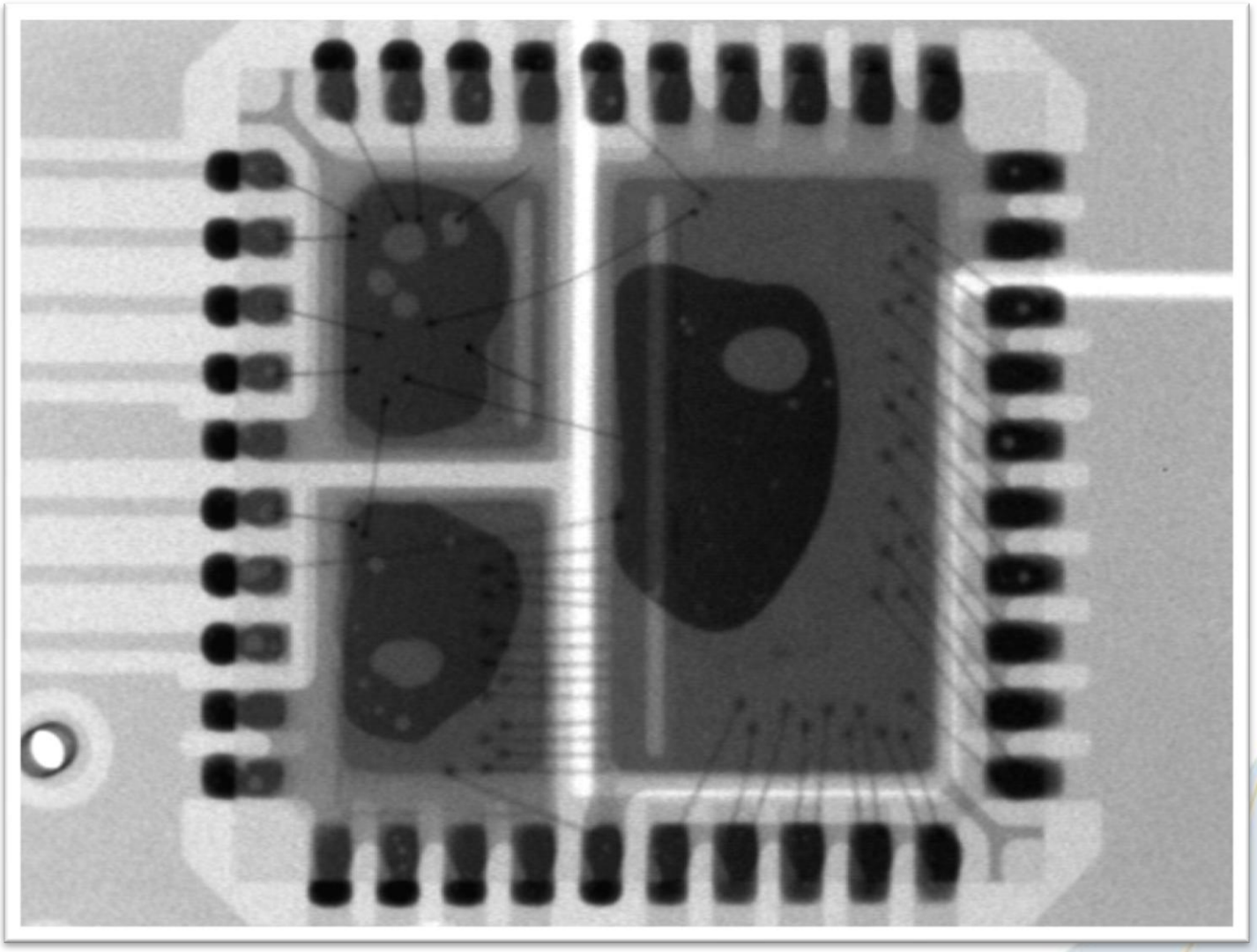




Beads



Non-Wetting



Analyze

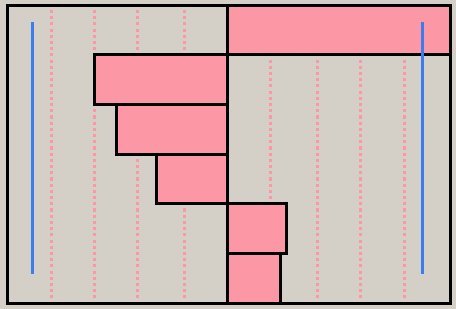
- Statistical modeling utilizing a software package allowed for quick analysis times
  - T-testing of the model allowed the experimenters to determine the important factors for the beading/voiding responses
  - Prediction profiler used to define factor parameters for successive DOEs

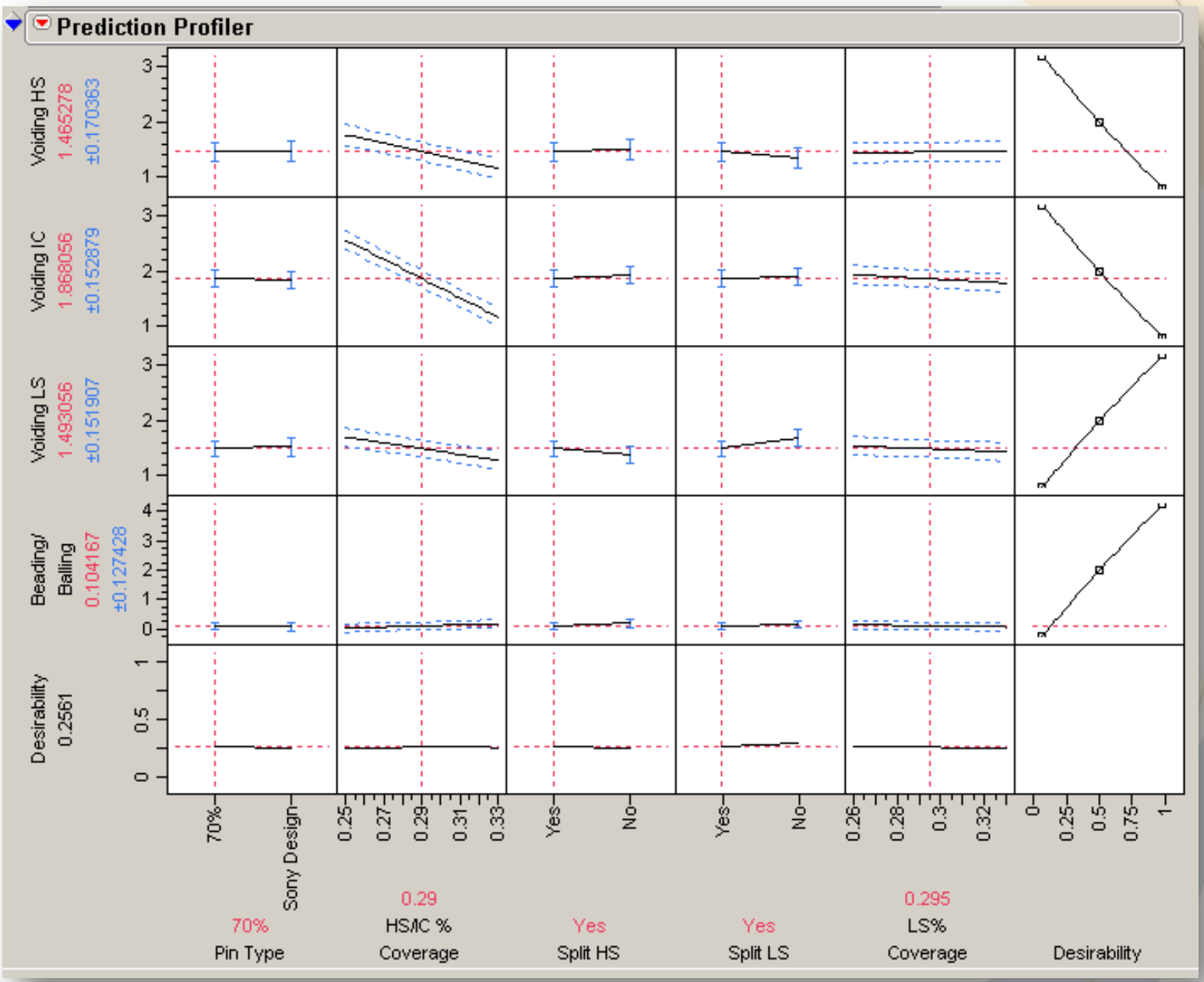
T-test with Interaction Effects

Response Beading/Balling

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
HS/C % Coverage(0.25,0.33)	0.0753968	0.033536	2.25	0.0254*
Split HS[Yes]	-0.045455	0.033839	-1.34	0.1803
LS% Coverage(0.26,0.33)	-0.03851	0.033839	-1.14	0.2561
Split LS[Yes]	-0.024621	0.033839	-0.73	0.4675
Pin Type[70%]*HS/C % Coverage	0.0198413	0.033536	0.59	0.5546
Pin Type[70%]	0.0176768	0.033839	0.52	0.6018




Prediction Profiler
Voiding HS
1.465278
±0.170363
Voiding IC
1.868056
±0.152879
Voiding LS
1.493056
±0.151907
Beading/ Balling
0.104167
±0.127428
Desirability
0.2561
70%
Sony Design
0.25
0.27
0.29
0.31
0.33
Yes
No
Yes
No
0.26
0.28
0.3
0.32
0
0.25
0.5
0.75
1
70%
Pin Type
0.29
HS/C %
Coverage
Yes
Split HS
Yes
Split LS
0.295
LS%
Coverage
Desirability

Improve

- Improvements came from consecutive DOEs permitting finer and finer resolution on an optimized process

Control

- Estimated that 60% of all SMT assembly errors created at stencil printing
  - Important to optimize this process for best yields!
  - For best results, an integrated focus on manufacturability should start with the circuit and PCB designers
- Pokie Yokie

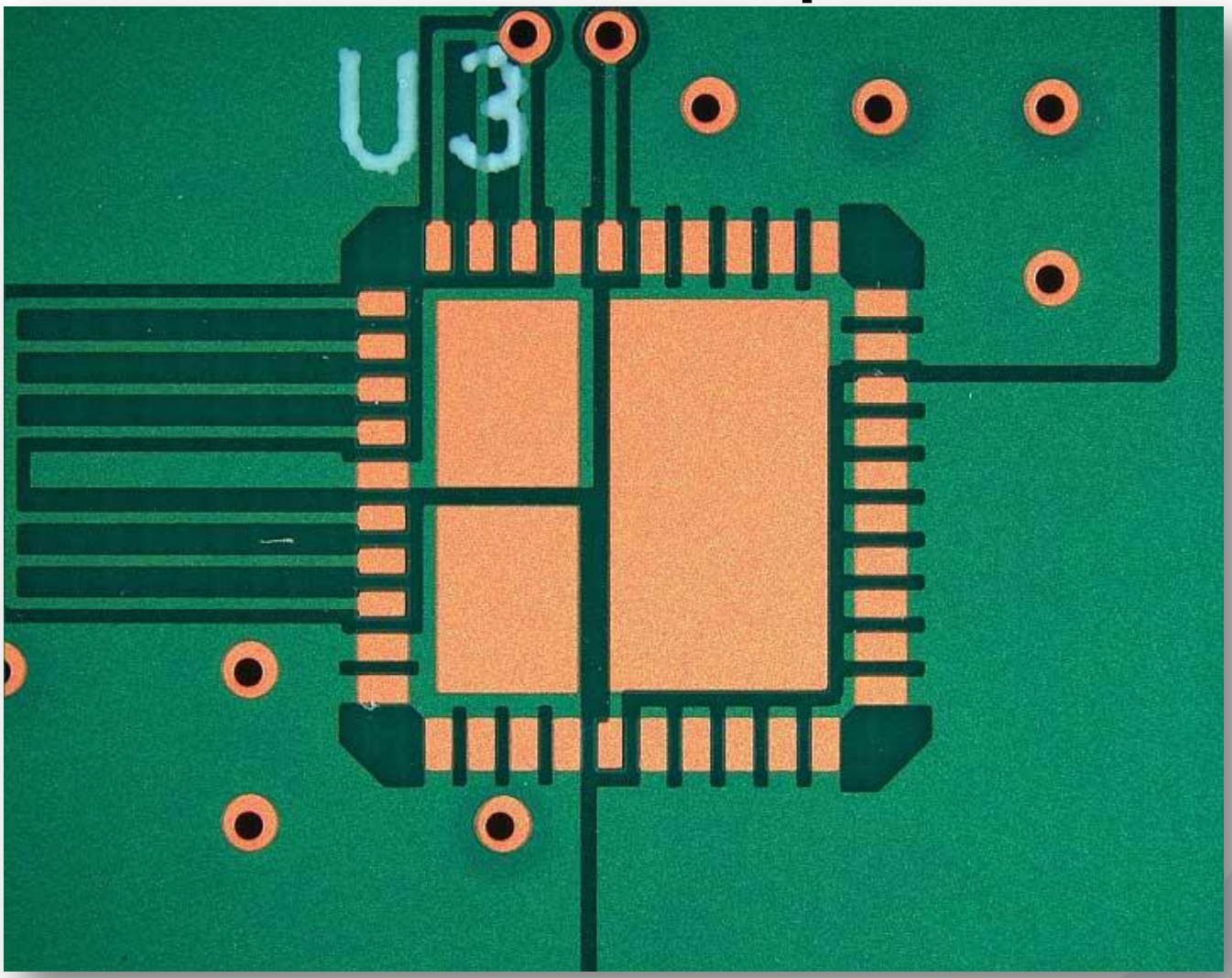
Which Part of the SMT Process Will Be Studied

- Problem occurred as customer was ramping new consumer electronics product
  - Very time sensitive problem, with top level management applying commensurate pressure on the team
  - Within the customer's manufacturing specification, changing the solder stencil was cheapest, and easiest solution
- The team believed the problem could be solved through stencil optimization

DOE#1

- Partial factorial DOE to determine if problem could be replicated at the Fairchild SMT Apps Lab, and confirm response could be altered with paste print combinations
- PCB matching local board design in customer's application designed
  - Finish, copper weight and geometry, pad finish, etc etc
  - 1 row on panel designed with via in pad
- Stencil designed with 5 combinations of solder coverage

Board Footprint



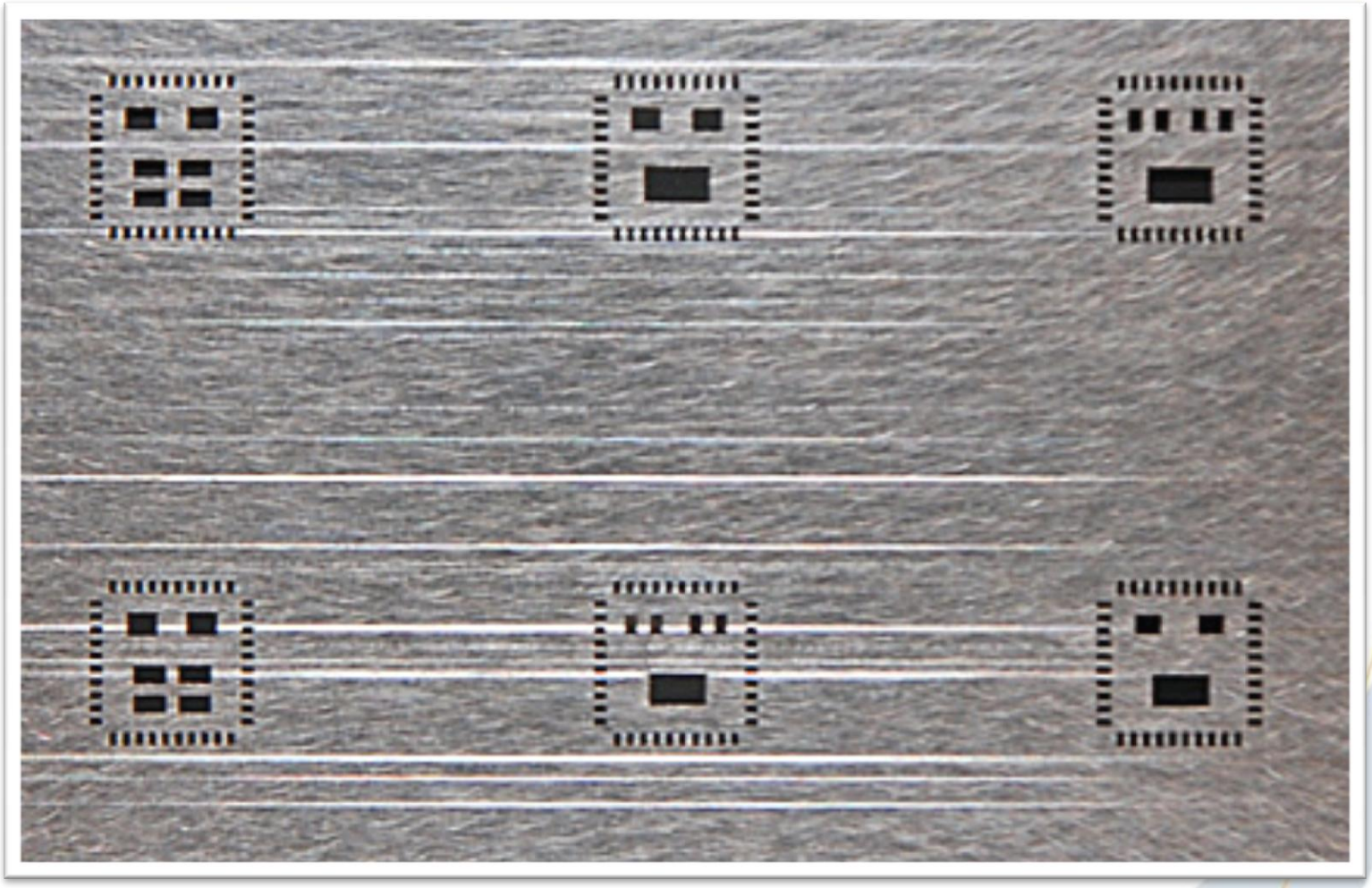
Results DOE#1

- With customer's process mimicked, solder anomaly was replicated
- Printing more or less paste did vary the response
- Via in pad did not improve the performance
  - Would not be studied further

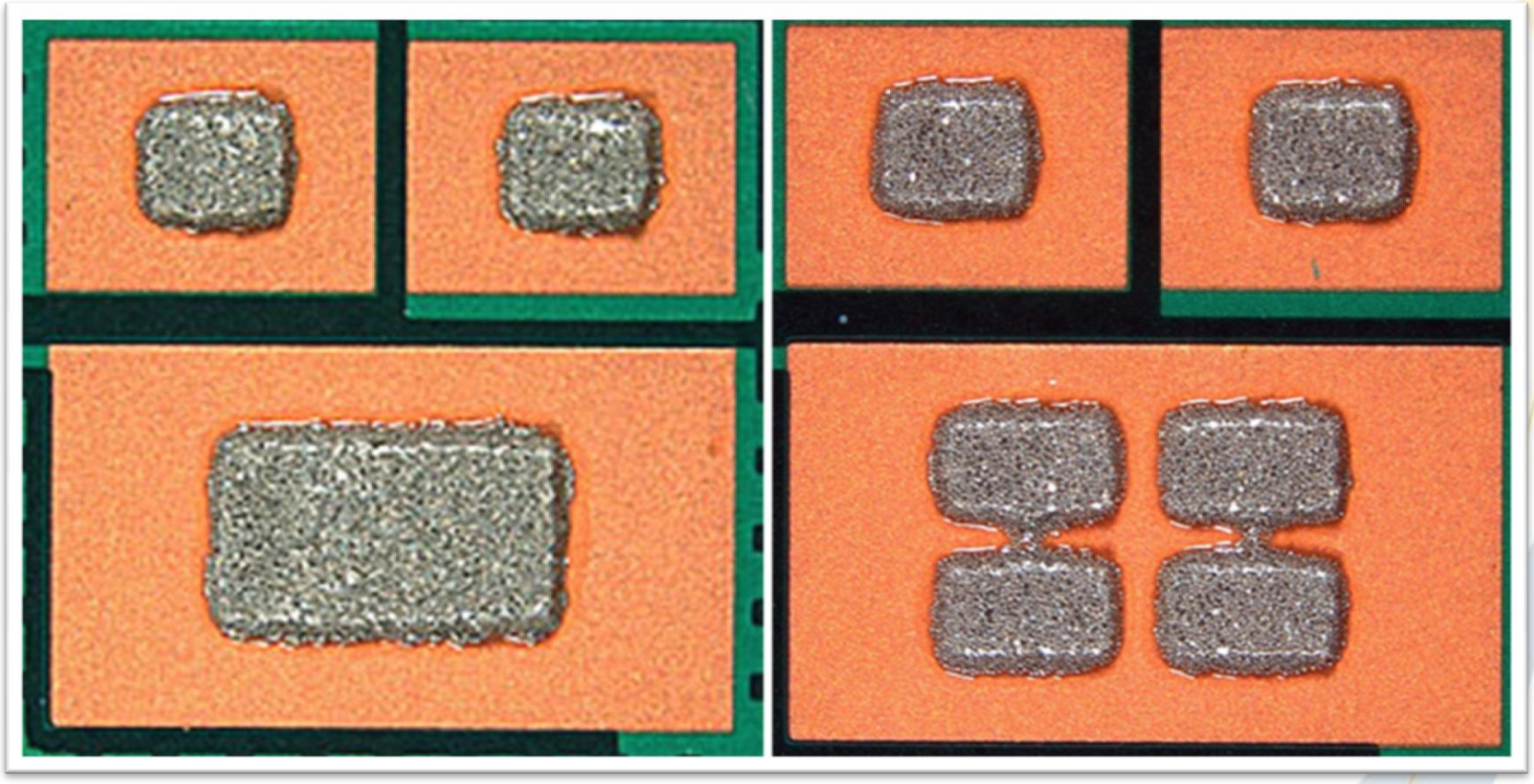
DOE#2

- 30 run DOE
  - Solder Coverage HS/IC - 2 level
  - Solder Coverage LS- 2 level
  - Split LS- Yes or No
  - Split HS- Yes or No
  - Outside Pin Coverage- 70% and 100%
- Full factorial study
  - Board had 30 locations, 2 combinations eliminated
  - Randomized runs across PCB panel
- 9 panels built, 270 devices mounted and x-rayed

Solder Stencil



Printed Paste

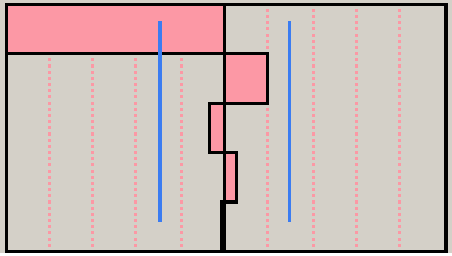


DOE#2 T-Test Voiding HS/IC

Response Voiding HS

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
HS/IC % Coverage(0.25,0.33)	-0.303704	0.04468	-6.80	<.0001*
Split LS[Yes]	0.0599747	0.045185	1.33	0.1856
Split HS[Yes]	-0.023359	0.045185	-0.52	0.6056
LS% Coverage(0.26,0.33)	0.0183081	0.045185	0.41	0.6857
Pin Type[70%]	-0.004419	0.045185	-0.10	0.9222

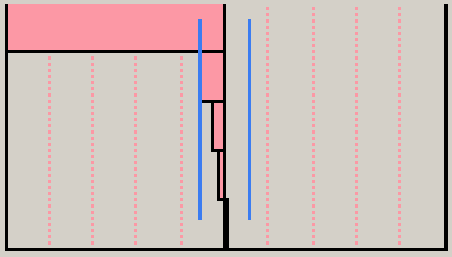


Least Squares Fit

Response Voiding IC

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
HS/IC % Coverage(0.25,0.33)	-0.7	0.040095	-17.46	<.0001*
LS% Coverage(0.26,0.33)	-0.076389	0.040548	-1.88	0.0607
Split HS[Yes]	-0.034722	0.040548	-0.86	0.3926
Split LS[Yes]	-0.020833	0.040548	-0.51	0.6078
Pin Type[70%]	0.0069444	0.040548	0.17	0.8641



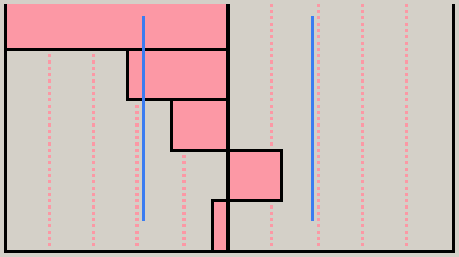
DOE#2 T-Test Voiding LS

Least Squares Fit

Response Voiding LS

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t
HS/C % Coverage(0.25,0.33)	-0.207407	0.03984	-5.21	<.0001*
Split LS[Yes]	-0.095328	0.04029	-2.37	0.0187*
LS% Coverage(0.26,0.33)	-0.053662	0.04029	-1.33	0.1840
Split HS[Yes]	0.0505051	0.04029	1.25	0.2111
Pin Type[70%]	-0.015783	0.04029	-0.39	0.6956

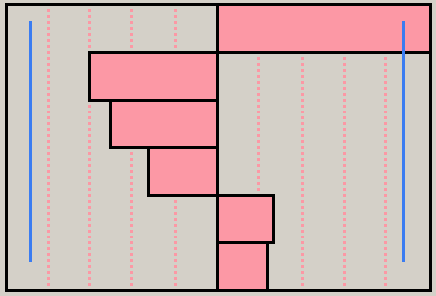


DOE#2 T-Test Beading/Balling

Response Beading/Balling

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
HSMC % Coverage(0.25,0.33)	0.0753968	0.033536	2.25	0.0254*
Split HS[Yes]	-0.045455	0.033839	-1.34	0.1803
LS% Coverage(0.26,0.33)	-0.03851	0.033839	-1.14	0.2561
Split LS[Yes]	-0.024621	0.033839	-0.73	0.4675
Pin Type[70%]*HSMC % Coverage	0.0198413	0.033536	0.59	0.5546
Pin Type[70%]	0.0176768	0.033839	0.52	0.6018



DOE#2 Results/Conclusions

- Voiding directly related to paste printed
  - More paste yielded less voiding response
  - More paste yielded more beading response
- Splitting the low side solder paste print had a statistically meaningful impact on LS voiding response
- Splitting the high side solder print did not meaningfully change voiding response (null hypothesis confirmed)
- Beading and balling response most strongly related to HS/IC print

DOE#3

- 36 Run DOE
  - Split LS- 2 level
    - 4 squares or 6 squares
  - Solid HS
    - Based on DOE#2 result and customer preference
  - Solder coverage HS/IC- 3 level
  - Solder coverage LS- 3 level
  - Asymmetric pad design- 2 level
    - 0º rotation, 180º rotation
- New PCB with 36 locations
- 8 panels, 288 devices mounted/x-rayed

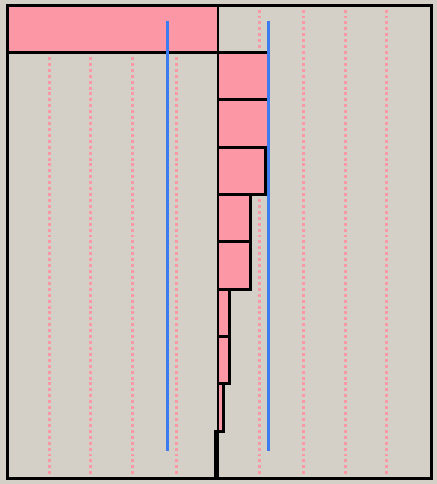
DOE#3 T-Test for HS Voiding

Response Voiding HS

Effect Tests

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
%HS/C	-16.49306	2.009351	-8.21	<.0001*
Pins[In]*LS Openings[4 pads]	0.0972222	0.049219	1.98	0.0492*
Pins[In]	0.0972222	0.049219	1.98	0.0492*
(%HS/C-0.33)*LS Openings[4 pads]	3.6458333	2.009351	1.81	0.0707
(LS-0.33)*LS Openings[4 pads]	2.6041667	2.009351	1.30	0.1960
(%HS/C-0.33)*Pins[In]	2.6041667	2.009351	1.30	0.1960
(LS-0.33)*Pins[In]	0.8680556	2.009351	0.43	0.6661
LS	0.8680556	2.009351	0.43	0.6661
(%HS/C-0.33)*(LS-0.33)	17.361111	82.03141	0.21	0.8325
LS Openings[4 pads]	-0.006944	0.049219	-0.14	0.8879



DOE#3 T-Test for Voiding IC

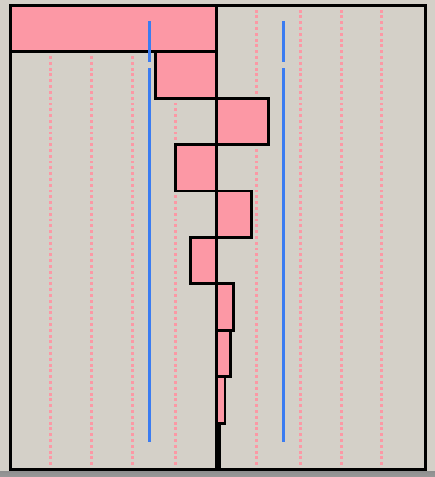
Response Voiding IC

Parameter Estimates

Effect Tests

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
%HSMC	-12.15278	2.018235	-6.02	<.0001*
LS Openings[4 pads]	-0.086806	0.049436	-1.76	0.0802
Pins[In]*LS Openings[4 pads]	0.0729167	0.049436	1.47	0.1414
(%HSMC-0.33)*(LS-0.33)	-95.48611	82.3941	-1.16	0.2475
(%HSMC-0.33)*LS Openings[4 pads]	2.0833333	2.018235	1.03	0.3029
(LS-0.33)*Pins[In]	-1.5625	2.018235	-0.77	0.4395
(%HSMC-0.33)*Pins[In]	1.0416667	2.018235	0.52	0.6062
(LS-0.33)*LS Openings[4 pads]	0.8680556	2.018235	0.43	0.6675
Pins[In]	0.0104167	0.049436	0.21	0.8333
LS	0.1736111	2.018235	0.09	0.9315



DOE#3 T-Test Voiding LS

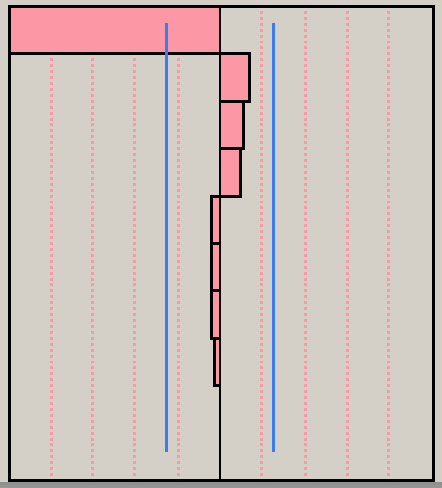
Response Voiding LS

Parameter Estimates

Effect Tests

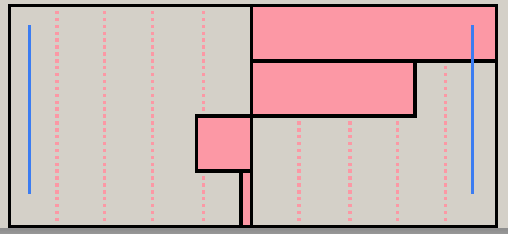
Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
LS	-14.58333	1.874339	-7.78	<.0001*
Pins[In]	0.0486111	0.045912	1.06	0.2906
Pins[In]*LS Openings[4 pads]	0.0416667	0.045912	0.91	0.3649
(%HSMC-0.33)*LS Openings[4 pads]	1.3888889	1.874339	0.74	0.4593
(LS-0.33)*LS Openings[4 pads]	-0.694444	1.874339	-0.37	0.7113
(%HSMC-0.33)*(LS-0.33)	-26.04167	76.51956	-0.34	0.7339
LS Openings[4 pads]	-0.013889	0.045912	-0.30	0.7625
%HSMC	-0.347222	1.874339	-0.19	0.8532
(%HSMC-0.33)*Pins[In]	-1.27e-15	1.874339	-0.00	1.0000
(LS-0.33)*Pins[In]	-6.55e-16	1.874339	-0.00	1.0000



DOE#3 T-Test Beading/Balling

Term	Estimate	Std Error	t Ratio	Prob>|t|
LS	3.125	1.440262	2.17	0.0309*
%HSMC	2.0833333	1.440262	1.45	0.1491
LS Openings[4 pads]	-0.017361	0.035279	-0.49	0.6230
Pins[In]	-0.003472	0.035279	-0.10	0.9217



DOE#3 Results/Conclusions

- Splitting the low side solder paste print into 4 or 6 rectangles had no meaningful impact on voiding response
  - Choose 4 rectangle layout, more robust solder screen
- Beading and balling response most strongly related to LS print within this range
- Rotating asymmetrical pins did not change results

Observation

- On second check, the profiler showed the PWI with the new board had increased from 50% to 84%
  - Seemed to show some degradation in performance

DOE#4

- Minimum combination for HS/IC print, 2 additional legs equal coverage HS/IC/LS
- Split LS- Yes/No
- Pin Coverage kept same
- Two reflow profiles

Reflow Profile- “Cold”/Previous

General | Description | Optimization

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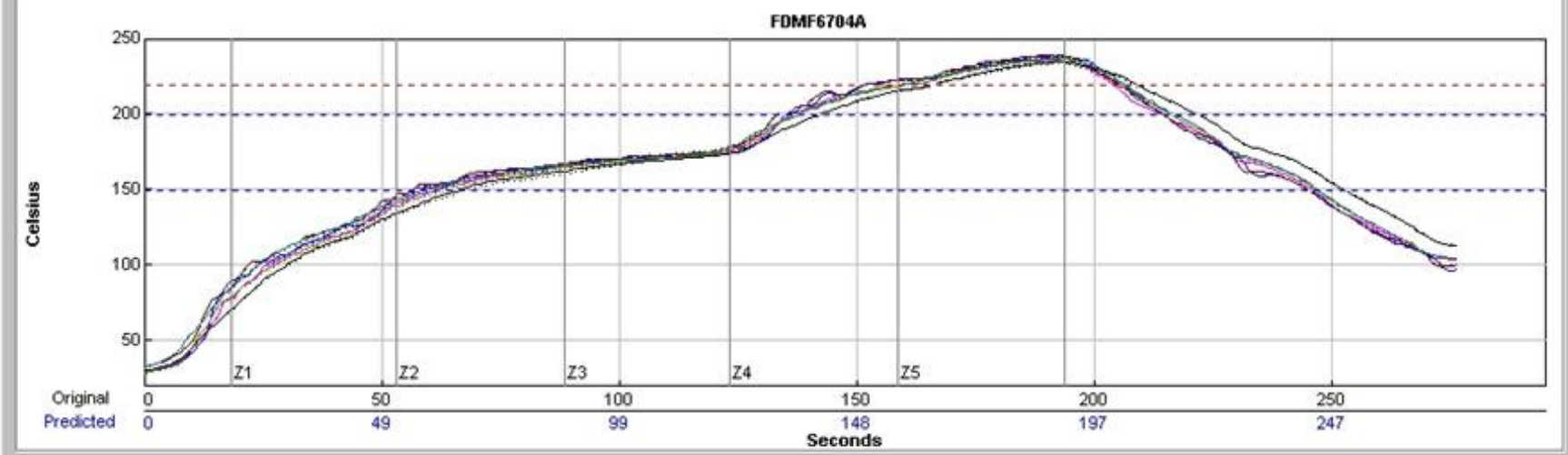

TCs	Max Rising Slope		Soak Time 150-200C		Reflow Time /220C		Peak Temp	
Front	3.3	35%	75.9	-47%	44.1	-6%	236.2	-38%
Middle	3.5	53%	77.2	-43%	53.0	53%	239.4	-6%
Rear	3.2	21%	75.7	-48%	44.7	-2%	236.3	-37%
Front 2	2.9	-3%	76.1	-46%	42.4	-18%	235.3	-47%
Rear 2	3.4	38%	77.3	-42%	53.6	57%	239.6	-4%
Middle 2	3.3	26%	78.3	-39%	47.5	17%	237.5	-25%
Delta	0.61		2.59		11.26		4.35	
P.Front	3.4	36%	72.8	-57%	41.1	-26%	235.1	-49%

	P.W.I.	inch/min	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5
Original Top	57%	20.4	182.0	182.0	180.0	251.0	258.0
Original Bottom			182.0	182.0	177.0	244.0	258.0

Reflow Profile- “Hot”

General | Description | Optimization

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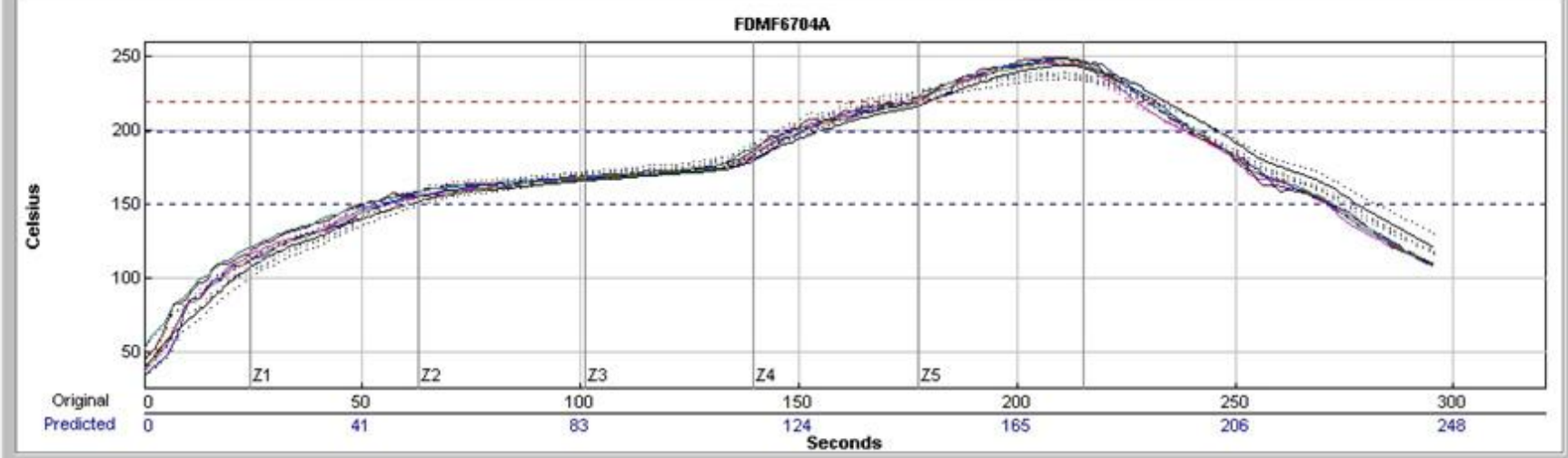


TCs	Max Rising Slope		Soak Time 150-200C		Reflow Time /220C		Peak Temp	
Front	3.5	50%	95.3	18%	49.5	30%	245.9	59%
Middle	3.7	70%	96.4	21%	52.5	50%	249.1	91%
Rear	3.4	37%	94.7	16%	52.5	50%	246.3	63%
Front 2	2.9	-3%	94.6	15%	53.6	57%	244.4	44%
Rear 2	3.3	27%	96.5	22%	54.7	65%	249.8	98%
Middle 2	3.1	6%	97.3	24%	55.4	70%	248.7	87%
Delta	0.79		2.71		5.94		5.40	
P.Front	3.4	45%	73.3	-56%	45.5	3%	237.1	-29%

	P.W.I.	inch/min	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5
Original Top	98%	17.6	190.0	177.0	176.0	240.0	275.0
Original Bottom			190.0	177.0	176.0	240.0	275.0

T-Testing Reflow Profile

Response Voiding HS

Whole Model

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Profile[Cold]	0.0091298	0.050421	0.18	0.8564

Response Voiding IC

Whole Model

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Profile[Cold]	-0.017735	0.051759	-0.34	0.7321

Response Voiding LS

Whole Model

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Profile[Cold]	-0.062626	0.044219	-1.42	0.1577

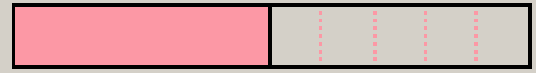
Parameter Estimates Beading/Balling

Response Beading

Whole Model

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Profile[Cold]	-0.031682	0.051973	-0.61	0.5426



DOE#4 Conclusions

- Reflow Profile within paste guidelines is not a statistically significant factor in voiding or beading
- Equal solder paste printing not necessarily best

Conclusions

- Six sigma tools allow for
  - Quick DOE creation
  - Powerful data analysis
  - Keep the experimenters on point
  - Can yield interactive factors
- SOLVE PROBLEMS!

Thank You!