FLAT-WRAP™

A Novel Approach to Copper Wrap Plate

Rajwant Sidhu, Ph.D.; DDI, Corp.

Abstract:

Copper Wrap Plate as specified in IPC 6012B table 3-2, is a requirement developed to enhance reliability for PCB's designed with via structures that require planarization and surface capping. PCB's built without wrap plating are more prone to failures associated with separation between the interconnection of the barrel copper to the surface copper. The improvement in reliability is a function of the copper wrap thickness, which supports the difference in IPC requirements for Class II and Class III programs. The general rule is "the thicker the wrap plating the better the reliability." The increase in copper thickness, associated with wrap plating, however competes with the ability for PCB fabricators to manufacture products with high density and fine features. The general rule for manufacturing fine features is "the thinner the copper the better the manufacturability."

The **technology** developed by **DDI Corp**. called **FLAT-WRAP™** offers a copper wrap solution that does not require build-up of copper on the external surface of a filled plated hole. This allows the improvement in reliability without sacrificing the ability to manufacture designs with high density and/or fine features. This technology also facilitates, in process non-destructive copper thickness measurements and ensures consistency of copper wrap thickness across the entire board surface. In this technology, the external surface copper thickness of filled plated holes will control the copper wrap thickness. In Printed Circuit Board designs requiring multiple copper wraps, the benefits of this technology are even more evident.

This article examines the current process problems with copper wrap plate and discusses the benefits provided by the **new technology** with respect to manufacturing and reliability.

Introduction:

Multilayer PCB production is a constantly evolving, increasingly complex interplay of, processing techniques, customer demands, design rules, and product specifications. Many times new processes will be added to meet certain demands, but are not easily and fully integrated into the existing process web. There is always a search for better ways to improve and simplify manufacturing processes. IPC added Copper Wrap Plate requirement to IPC 6012B specification, requiring copper plating from the filled plated hole to continue around the knee of the hole and onto the surface. This requirement was introduced to improve reliability for failures due to separation between surface features/caps and the plated hole-wall. The increased surface copper thickness due to copper wrap plate posed additional challenges for manufacturers to manufacture and designers to design the PCB's. This article highlights the current issues for dealing with the copper wrap requirements specified in IPC 6012B and the benefits of the new technology called **FLAT-WRAP™**.

IPC 6012 Wrap Plating Specification:

IPC-6012B specifies that Copper Wrap Plating shall be continuous from the filled plated hole onto the external surface of the plated structure and extend by a minimum of 25 microns (984 micro-inches) where an annular ring is required. Figure 1 shows this requirement.

Figure 2, shows that any reduction of wrap plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed. IPC-6012B Table 3-2 gives the requirements for copper wrap thickness. The continuous minimum wrap requirement for class 2 designs is 0.000197" and for class 3 designs is 0.000472".

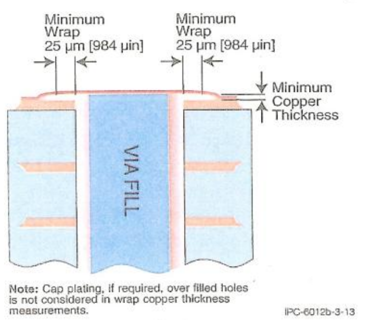


Figure 1

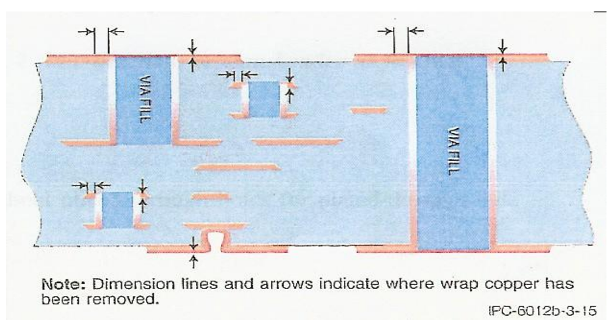


Figure 2

Figure 3 shows a sketch of a PCB design with three different sets of blind vias sharing a common layer and having terminations on different layers built with conventional copper wrap process. Three sequential copper wrap plates are required for this type of design.

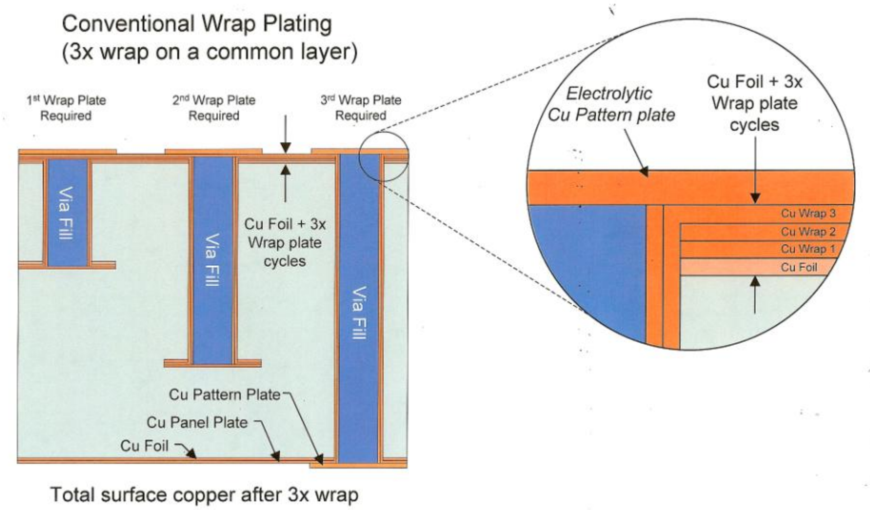
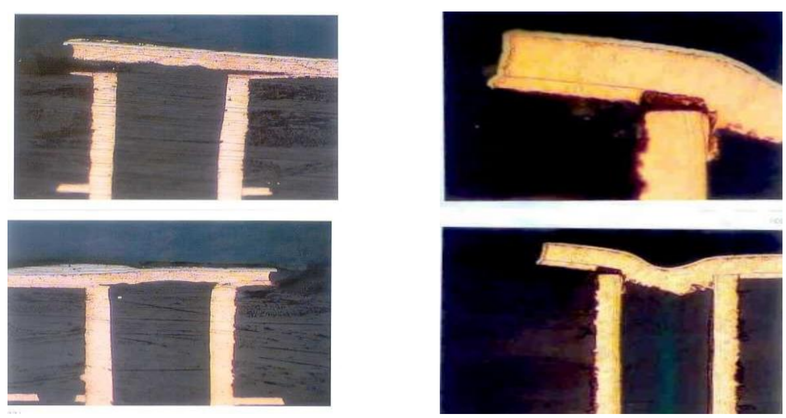


Figure 3 Conventional Copper Wrap Plate

Reliability vs. Copper Wrap Plate:

Figures 4 and 5 are cross-sectional views of filled plated holes showing varying degrees of separation between the copper barrel and their corresponding surface copper caps.

The thermally induced separations are the result of **insufficient or no** copper wrap plating.



Figures 6 and 7 are cross sectional views of filled plated holes with sufficient Copper Wrap Plate. The holes in figures 6 and 7 were thermally stressed similar to the failed holes shown in Figure 4 and 5. These holes show no sign of separation between the copper barrel and their corresponding surface copper caps validating that copper wrap plate improves reliability.

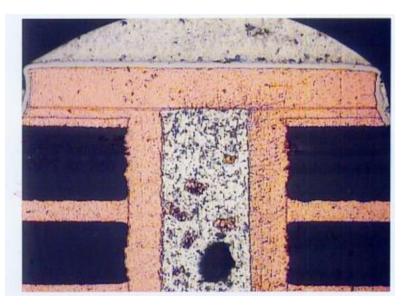


Figure 6

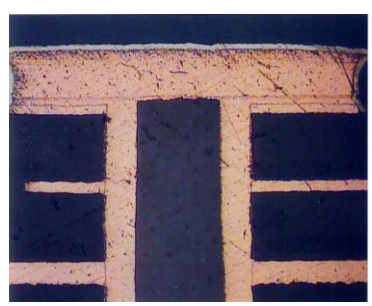


Figure 7

Figures 8 and 9 are cross sectional views of filled plated holes with visible copper wrap plate but exhibiting separation between hole wall and the plated copper caps over the filled plated holes. The holes in figures 8 and 9 were thermally stressed similar to the failed vias shown in Figure 4 and 5. In these examples, copper wrap is evident; however the thickness is not sufficient to prevent separation. The hole size, type of fill material and board material, construction & thickness are functions of how much copper wrap plate may be sufficient to insure reliability.

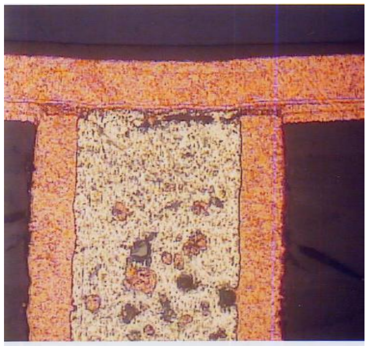


Figure 8


Figure 9

<u>PCB Industry Issues</u>

PCB's requiring filled plated holes, with copper wrap plate are less prone to thermally induced separations between surface features and the plated hole-wall. However, conventional wrap plating increases surface copper thickness due to copper wrap build up over surface copper.

This increased thickness makes it difficult for fabricators to produce PCBs with higher density and fine lines. IPC specification for Class 2 requires a minimum of .0002" continuous copper wrap from hole-wall onto the external surface of a plated structure and IPC Class 3 requires a minimum of .0005" continuous copper wrap. **The problem here is, how to build high reliability PCB's without compromising the design rules that are required to fabricate HDI designs.**

Table 1 illustrates the effect of copper wrap on fabrication design rules for line width and space. For example, starting with 3/8 oz copper foil, this particular fabricator shows a space requirement of 0.0035" to produce 0.003" features for designs that **do not** require wrap plating. In the same example, if two copper wraps are needed the space requirement increases from 0.0035" to 0.007" for Class 2 and from 0.0035" to 0.0085" for Class 3 (standard builds).

Table 1

Space Requirements for PCB's requiring Copper Wrap Plate (Conventional Process)								
Design Rule (3/8 Oz Cu)	**IPC 6012B Class 2**				**IPC 6012B Class 3**			
	No Wrap	**1X Wrap**	**2X Wrap**	**3X Wrap**	**No Wrap**	**1X Wrap**	**2X Wrap**	**3X Wrap**
Space req.	**0.0035"**	0.005"	**0.007"**	0.009"	**0.0035"**	0.00575"	**0.0085"**	0.0115"

Fabrication processes such as lamination; plating and planarization have an affect on the consistency of copper wrap plating thickness across a PCB panel. Variation from these processes force fabricators to plate more copper on external surface of filled plated holes than required by IPC specification 6012B. This is done to insure minimum copper wrap is maintained across the entire panel which further reduces the capability to produce fine lines and spaces. Figures 10 shows copper wrap plating for a filled plated hole with **three Class 2 wraps**. The total surface copper thickness of three copper wrap plates and initial copper foil is 0.0014". This copper thickness is etched to create the surface copper features. Figure 11 shows the top of the BGA pad features illustrated by the cross-section view in figure 10. Starting with an imaged pad size of 0.022", the resulting finished diameter of the pad is 0.0176" as measured from the top. Likewise, figure 12 shows copper wrap plating for a filled plated hole with **three Class 3 wraps**. The total surface copper thickness of three copper wrap plates and initial copper foil is 0.0029". This copper thickness is etched to create the surface copper features. Figure 13 shows the top of the BGA pad features illustrated by the cross-section view in Figure 12. Starting with an imaged pad size of 0.022", the resulting finished diameter of the pad is 0.0137" as measured from the top.

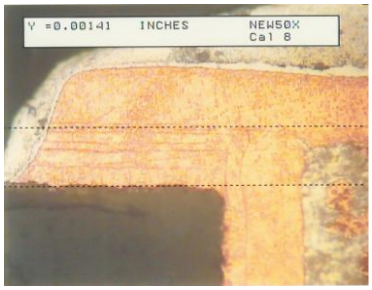


Figure 10
Surface Copper Class 2 Design (3X Wrap)

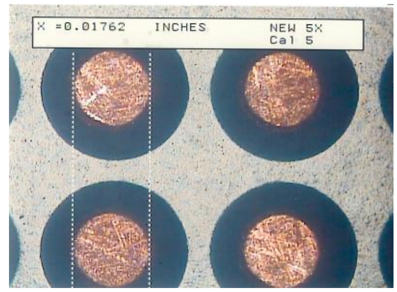


Figure 11
Pad Size Class 3 Design (3X Copper Wrap)

Side view of pad in Figure 11

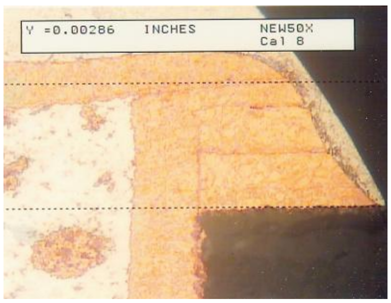


Figure 12
Surface Copper Class 3 Design (3X Wrap)

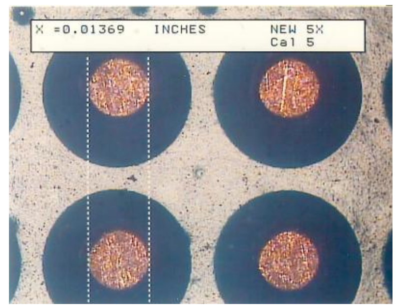


Figure 13
Pad Size Class 3 Design (3X Copper Wrap)

Side view of pad in Figure 13

Conventional Process:
There are two commonly used conventional processes for processing PCB's with copper wrap requirements.

The less common technique is to image and plate a dot image around via fill holes and the barrel at the same time. After via fill, the bumps are partially sanded in order to leave an annular ring of copper wrap plate on the surface. The only way to measure the amount of Copper Wrap Plate is with destructive cross-sectioning technique. The complete lot is generally accepted or rejected based on one or two correlations between test coupons and the board area. Since each panel is planarized individually, cross sections from one panel may not represent the copper wrap plate thickness on other panels within the lot. With this technique, if the through-holes with wrap requirements are in a tight BGA area, it becomes very difficult for the photo resist to conform around pads/bumps for subsequent processing. This could ultimately cause shorts between BGA pads.

The most common Copper Wrap Plate process is to panel plate the hole-wall and the surface simultaneously. Plating on the surface must exceed the minimum required thickness of copper wrap plate to facilitate the planarization process. A selective barrel plate process is used to further plate the hole-wall to the customer specification. The holes after selective barrel plate are via filled and planarized to remove the excess via fill material and plated bumps around the filled holes to obtain a flat copper surface. This is done with care to leave sufficient copper wrap plate thickness on the panel surface in order to meet the minimum specified wrap thickness in IPC 6012B, table 3.2. Destructive cross sections are required to verify wrap thickness. Using this wrap process, additional wrap plating cycles will add additional thickness to the surface copper. Table 2 shows the variation of one Class 2 copper wrap with 3/8 oz foil. The table illustrates the variation across one panel and from panel-to-panel within a 5-panel lot.

Table 2

COPPER WRAP AND TOTAL SURFACE COPPER THICKNESS VARIATION (CONVENTIONAL-class 2)					
PRODUCTION LOT #1		**SIDE - 1**		**SIDE - 2**	
Panel #	**X-sec. #**	**COPPER WRAP**	**SURFACE COPPER**	**COPPER WRAP**	**SURFACE COPPER**
1	5	0.00033”	0.00079”	0.00031”	0.00076”
1	4	0.00039”	0.00088”	0.00048”	0.00089”
1	3	0.00043”	0.00091”	0.00048”	0.00084”
1	2	0.00034”	0.00087”	0.00048”	0.00081”
1	1	0.00021”	0.00075”	0.00030”	0.00082”
2	1	0.00051”	0.00094”	0.00045”	0.00092”
3	1	0.00027”	0.00074”	0.00027”	0.00079”
4	1	0.00037”	0.00090”	0.00046”	0.00094”
5	1	0.00040”	0.00094”	0.00054”	0.00107”
Statistical Analysis					
Max		0.000510”	0.000940”	0.000540”	0.001070”
Min		0.000210”	0.000740”	0.000270”	0.000760”
Range		0.000300”	0.000200”	0.000270”	0.000310”
Average		0.000361”	0.000858”	0.000419”	0.000871”
Std Dev		0.000088”	0.000078”	0.000098”	0.000096”
Std Dev (Panel)		0.000083”	0.000096”	0.000096”	0.000047”
Std Dev (Lot)		0.000117”	0.000115”	0.000115”	0.000111”

A Novel Solution to the Wrap Plate issues

The new technology offers a novel solution to the design and manufacturing issues related to copper wrap requirements. **This technology offers reliability without limiting fabrication capability**. The new technology also offers the benefit of verifying the wrap thickness without coupon correlation and destructive cross-sectioning analysis. With this technology, one can control the copper wrap thickness by changing the starting surface copper thickness. Figure 14 shows a sketch of a similar PCB design as shown in Figure 3 with three different sets of blind vias sharing a common layer and having terminations on different layers built with **new copper wrap process**. This design also requires three sequential wrap plate cycles.

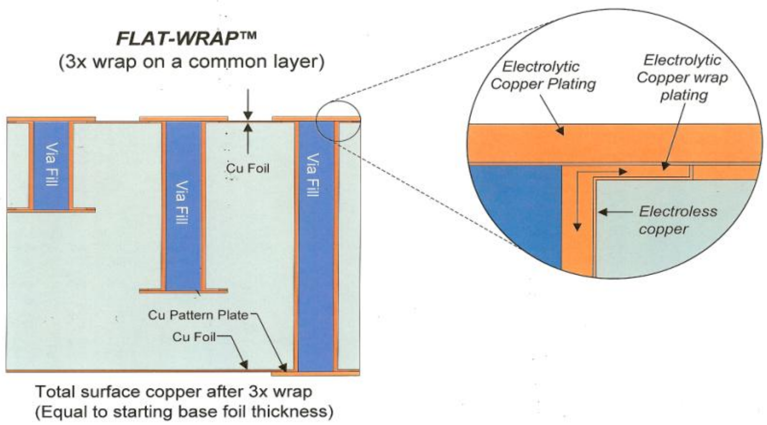


Figure 14

Table 3 shows theoretical surface copper buildup for multiple wraps, comparing conventional Class 2, Class 3 and Class 3 with **the new technology.** With conventional wrap process, the surface copper thickness increases with every wrap plate cycle. With the **new technology**, the surface copper thickness remains the same regardless of the number of wrap plate cycles.

Table 3

SURFACE COPPER THICKNESS (INCLUDING FOIL (H oz.)) FOR COPPER WRAP PLATE								
CLASS 2 (Conventional)			CLASS 3 (Conventional)			CLASS 3 (New Process)		
1X	2X	3X	1X	2X	3X	1X	2X	3X
0.0009”-0.0012”	0.0011”-0.0017”	0.0013”-0.0022”	0.0012”-0.0015”	0.0017”-0.0023”	0.0022”-0.0031”	0.0006”-0.0009”	0.0006”-0.0009”	0.0006”-0.0009”

Table 4 shows a comparison of surface copper thickness and finished pad size starting with half-ounce foil and an imaged pad size of 0.022” for Conventional Class 2 & Class 3 and **Class 3** with the **new technology.** The surface copper thickness is critical as this thickness of copper is etched to create copper surface features.

Table 4

PAD SIZE COMPARISON (STARTING PAD SIZE 0.022”)					
Conventional Process CLASS 2 (3X WRAP)		Conventional Process CLASS 3 (3X WRAP)		New Technology CLASS 3 (3X WRAP)	
Surface Copper	Finished Pad Size	Surface Copper	Finished Pad Size	Surface Copper	Finished Pad Size
0.0141”	0.01762”	0.00286”	0.01369”	0.00074”	0.01901”

Table 5 illustrates the benefit of the **new technology** on fabrication design rules with copper wrap requirements. Starting with 3/8 oz copper foil, this particular fabricator shows a space requirement of 0.0035” to produce 0.003” features for designs that **do not** require wrap plating. Starting with the same surface copper thickness, the space requirement remains the same with the **new technology** regardless of the number of wrap plate cycles.

Table 5

Space Requirements for PCB’s requiring Copper Wrap Plate (New Technology)								
Design Rules (3/8 Oz Cu)	IPC 6012B Class 2				IPC 6012B Class 3			
	No Wrap	1X Wrap	2X Wrap	3X Wrap	No Wrap	1X Wrap	2X Wrap	3X Wrap
Etch comp	0.0005"	0.0005"	0.0005"	0.0005"	0.0005"	0.0005"	0.0005"	0.0005"
Space req.	0.0035"	0.0035"	0.0035"	0.0035"	0.0035"	0.0035"	0.0035"	0.0035"

Figures 15-17 show the advantage of controlled feature size produced by using the **new technology**. Figure 15 shows the image photo-tool with a pad size (0.022”) used to produce the pads shown in Figures 16 and 17 and previous Figures 10,11,12, and 13. Figure 16 shows copper wrap plating with the **new technology** for a filled plated hole with three Class 3 wraps. The total surface copper thickness of three copper wrap plates and initial surface copper is 0.0007”. This copper thickness is etched to create the surface copper features. Figure 17 shows the top of the BGA pad features illustrated by the cross-section view in figure 16. Starting with an imaged pad size of 0.022”, the resulting finished pad diameter is 0.0190” as measured from the top.

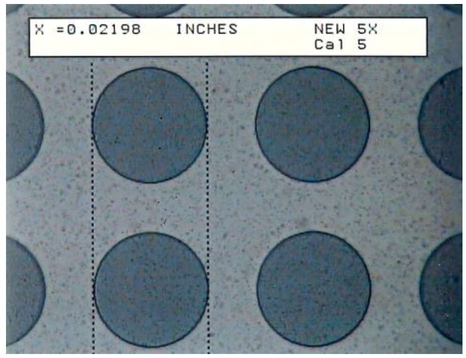
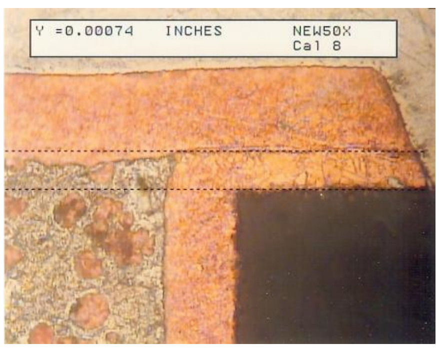


Figure 15 A/W Pad Size



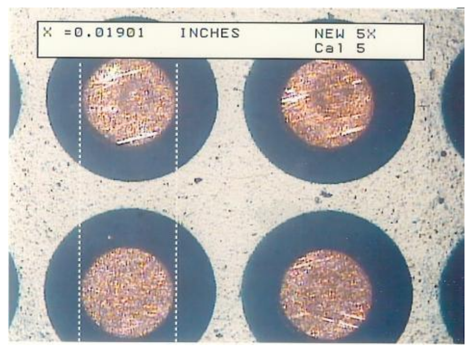


Figure 16
Wrap Thickness, Class 3 Design (3X Wrap)

Figure 17
Pad Size Class 3 Design (3X Copper Wrap)

(New Technology)

<u>Description of the New Process</u>

In **the new** process, the copper wrap plate is created by selectively recessing or removing the surface copper around the filled plated holes.

The plating from the hole-wall continuously wraps onto the surface of the substrate to substantially the same thickness height of the surface copper. This feature of this process allows verification of the wrap plate thickness without destructive cross sectioning. The wrap thickness can be measured by using a surface copper probe. This process also enables fabricators to verify wrap thickness across the entire panel and for each panel within a lot. Figure 18 shows that the wrap plate thickness is essentially the same as the initial starting thickness of the surface copper. Figure 19 shows a cross section of the entire filled plated hole shown in Figure 18.

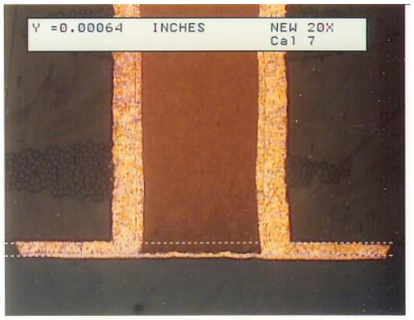


Figure 18

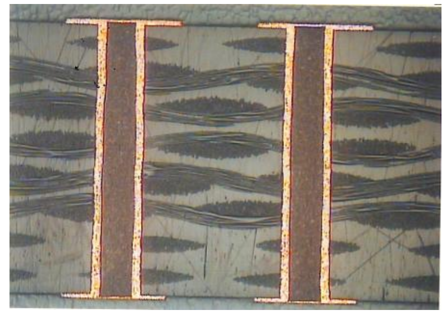


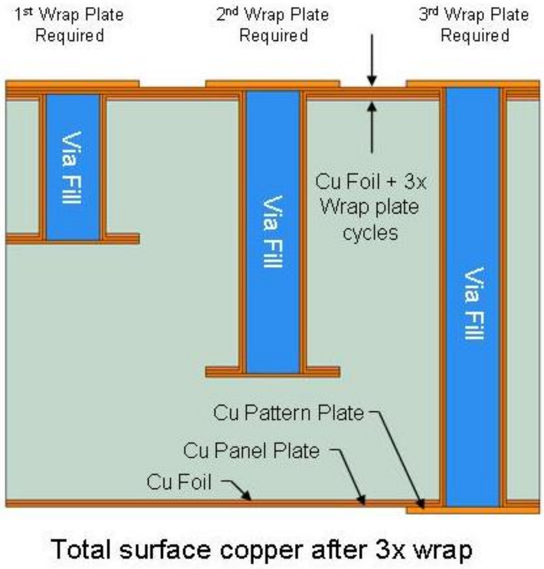
Figure 19

Table 6 shows the variation of one Class 2 copper wrap starting with 3/8 oz foil. The table illustrates the variation across one panel and from panel-to-panel within a 5-panel lot.

Table 6

COPPER WRAP AND TOTAL SURFACE COPPER THICNESS VARIATION (NEW TECHNOLOGY-Class 2)					
PRODUCTION LOT #2		**SIDE - 1**		**SIDE - 2**	
Panel #	**X-sec. #**	**COPPER WRAP**	**SURFACE COPPER**	**COPPER WRAP**	**SURFACE COPPER**
1	5	0.00053”	0.00053”	0.00050”	0.00050”
1	4	0.00054”	0.00054”	0.00054”	0.00054”
1	3	0.00056”	0.00056”	0.00053”	0.00053”
1	2	0.00052”	0.00052”	0.00053”	0.00053”
1	1	0.00050”	0.00050”	0.00046”	0.00046”
2	1	0.00053”	0.00053”	0.00051”	0.00051”
3	1	0.00055”	0.00055”	0.00051”	0.00051”
4	1	0.00051”	0.00051”	0.00054”	0.00054”
5	1	0.00054”	0.00054”	0.00049”	0.00049”
Statistical Analysis					
Max		0.000560”	0.000560”	0.000540”	0.000540”
Min		0.000500”	0.000500”	0.000460”	0.000460”
Range		0.000060”	0.000060”	0.000080”	0.000080”
Average		0.000531”	0.000531”	0.000512”	0.000512”
Std Dev		0.000019”	0.000019”	0.000026”	0.000026”
Std Dev (Panel)		0.000022”	0.000022”	0.000033”	0.000033”
Std Dev (Lot)		0.000021”	0.000021”	0.000029”	0.000029”

Figure 20 and 21 shows a schematic sketch comparison of a PCB design with three different sets of blind holes sharing a common layer that terminate on different layers. For this type of design, three copper wraps are required on the common layer. Figure 20 represents the design built with conventional copper wrap plate. Figure 21 shows the same design built with **the new** technology. Figure 21 compared to Figure 20, illustrates the benefit of creating multiple copper wrap plates without adding additional copper to the surface copper thickness.



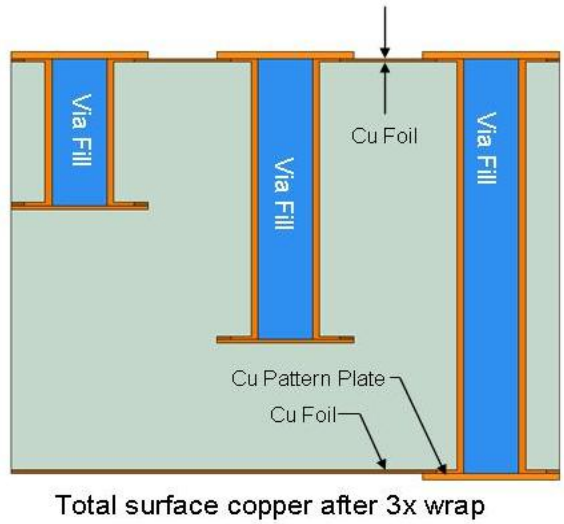


Figure 20
Conventional Copper Wrap Plate

Figure 21
FLAT-WRAP™ Technology

Reliability Test Results of New Technology

The reliability of **this technology** was demonstrated through a series of vigorous thermal testing methods including lead free assembly simulation. Sample coupons were tested using PCB industry recognized test techniques as follows:

1. Solder Float test (3X & 6X) at 500°F and 550°F
2. Lead free reflow assembly simulation
3. Interconnect Stress Test (IST)
4. Highly Accelerated Thermal Shock (HATS)
5. Materials tested: High Tg - FR-4 and Polyimide

The Test matrix and test results are listed in Table 5,6,7,8 and 9.

TABLE 5

Description of Tests for 8 layer PCB with 3 X Wrap on layer 1					Remarks	Test Status	Test Results
Production Tests	As received - Microsection PTH Quality	Plated Barrel Copper Thickness	Record Avg Plating Thickness		Microsection analysis performed by DDi	Completed	Passed
Pb-Free Assy Process Compatibility	Solder Float Test - Microsection PTH Quality	Temperature Deg C (Deg F)	260 (500)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
			288 (550)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
	Pb Free Reflow Assembly Simulation	Temperature Deg C (Deg F)	260 (500)	4X	Microtek Labs to process BGA coupons through Pb Free profile through IR Reflow oven and DDi to do microsection analysis	Completed	Passed
				6X			Passed
Reliability Tests	IST - Interconnect Stress Test	IST Pre-conditioning cycles at 260 C	4X		3 coupons / preconditioning (Total of 18 coupons). Dual sense test performed by DDi VA. Two different test conditions with Non-Cond & Cond via fill materials	Completed & Reported by Avg Cycles	Blind Vias No Failure & Thru Vias Pass 864 @ 6X & 1176 @ 4X
			6X				
	HATS - Highly Accelerated Thermal Shock	Pb Free Assembly Profile Pre-conditioning, peak temp 260°C	0		A total of 36 coupons were tested with 3 pre-conditions, 6 As Is, 15 @ 4X and 15 @ 6X	Coupons tested by Microtek Labs to 500 cycles	Passed
			4X				
			6X				

Table 6

Summary of HATS testing for High Tg FR4 laminate and prepreg Testing done by MICROTEK Laboratories							
Coupon #	Description	Coupon	Reflow pre-condition @ 260°C	HATS test to 500 cycles			
				Net 1 - Through Vias L1-L8	Net 2 - Through Vias L1-L8	Net 3 - Blind Vias L1-L6	Net 4 - Blind Vias L1-L7
1	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	3
2	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	Pass
3	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	Pass
4	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	Pass
5	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
6	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
7	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
8	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
9	New Approach	HATS_0722	6x	Pass	Pass	Pass	Pass
10	New Approach	HATS_0722	6x	Pass	Pass	Pass	Pass
11	New Approach	HATS_0722	6x	Pass	Pass	Pass	Pass
12	New Approach	HATS_0722	6x	Pass	Pass	Pass	Pass
13	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	123
14	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	Pass
15	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	Pass
16	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	Pass
17	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	Pass
18	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	Pass
19	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	Pass
20	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	N/A
21	New Approach	HATS_0722	4x	Pass	Pass	Pass	Pass
22	New Approach	HATS_0722	4x	Pass	Pass	Pass	Pass
23	New Approach	HATS_0722	4x	Pass	Pass	Pass	Pass
24	New Approach	HATS_0722	4x	Pass	Pass	Pass	Pass
25	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
26	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
27	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
28	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
29	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
30	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
31	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
32	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
33	New Approach	HATS_0722	As is	Pass	Pass	Pass	Pass
34	New Approach	HATS_0722	As is	Pass	Pass	Pass	Pass
35	New Approach	HATS_0722	As is	Pass	Pass	Pass	Pass
36	New Approach	HATS_0722	As is	Pass	Pass	Pass	Pass

Table 7

Summary of IST testing for High Tg FR4 laminate and prepreg **Testing done by PWB Interconnect Solutions Inc.**									
Description / Pre-condition	**IST Cycles to Failure - All Data**								
	Coupon	**P1**	**%**	**S1**	**%**	**S2**	**%**	**Comb**	**Result**
New Approach - 4X260°C	**SL08041A_1**	1000	-1.1	1000	0	1000	-1.1	1000	Accept
New Approach - 4X260°C	**SL08041A_2**	1000	-0.1	1000	1.5	1000	-0.1	1000	Accept
New Approach - 4X260°C	**SL08041A_3**	1000	-0.1	1000	1	1000	-0.5	1000	Accept
IPC Class 2 - 4X260°C	**SL08040A_1**	1000	-0.1	1000	-0.1	1000	0.1	1000	Accept
IPC Class 2 - 4X260°C	**SL08040A_2**	627	10	627	-0.3	627	-0.2	627	Post
IPC Class 2 - 4X260°C	**SL08040A_3**	1000	0.1	1000	0	1000	-0.6	1000	Accept
IPC Class 3 - 4X260°C	**SL08040A_1**	1000	0	1000	0	1000	0	1000	Accept
IPC Class 3 - 4X260°C	**SL08040A_2**	1000	0	1000	0	1000	0	1000	Accept
IPC Class 3 - 4X260°C	**SL08040A_3**	1000	0	1000	0	1000	0	1000	Accept
New Approach - 6X260°C	**SL08040A-1**	1000	0.5	677	10	1000	-0.1	677	S1
New Approach - 6X260°C	**SL08040A-2**	1000	1	594	10	1000	-0.1	594	S1
New Approach - 6X260°C	**SL08040A_3**	1000	1	923	10	1000	0	923	S1
IPC Class 2 - 6X260°C	**SL08040A_1**	1000	1.7	1000	1.3	1000	1.4	1000	Accept
IPC Class 2 - 6X260°C	**SL08040A_2**	397	10	397	-0.2	397	0.1	397	Post
IPC Class 2 - 6X260°C	**SL08040A_3**	1000	0.5	1000	0.6	1000	0.8	1000	Accept
IPC Class 3 -6X260°C	**SL08040A_1**	1000	0.9	1000	0.8	1000	1.3	1000	Accept
IPC Class 3 - 6X260°C	**SL08040A_2**	1000	6	1000	0.4	1000	1.1	1000	Accept
IPC Class 3 - 6X260°C	**SL08040A_3**	1000	0.8	1000	0.8	1000	1.1	1000	Accept
New Approach - 4X260°C	**SL08041A_1**	1000	1.1	1000	1.6	1000	1.4	1000	Accept
New Approach - 4X260°C	**SL08041A_2**	1000	3.6	1000	1	1000	1.5	1000	Accept
New Approach - 4X260°C	**SL08041A_3**	1000	2.2	1000	4.3	1000	3.5	1000	Accept
New Approach - 6X260°C	**SL08041A_1**	1000	-0.1	1000	2.5	1000	0.1	1000	Accept
New Approach - 6X260°C	**SL08041A_2**	1000	-0.6	1000	-0.2	1000	-0.4	1000	Accept
New Approach - 6X260°C	**SL08041A_3**	1000	1.8	1000	0.5	1000	0	1000	Accept
Summary		**Mean**		**Std Dev**		**Min cycles**		**Max cycles**	
Conventional IPC Class 2, P1		837.3		262.3		397		1000	
Conventional IPC Class 3, P1		1000		0		1000		1000	
New Approach, P1		1000		0		1000		1000	
Conventional IPC Class 2, S1		837.3		262.3		397		1000	
Conventional IPC Class 3, S1		1000		0		1000		1000	
New Approach, S1		932.83		141.72		594		1000	
Conventional IPC Class 2, S2		837.3		262.3		397		1000	
Conventional IPC Class 3, S2		1000		0		1000		1000	
New Approach, S2		1000		0		1000		1000	
Coupon SL08040A, S1 = L1-L8 PTH with CB100 and S2 = L1-L7 with non-conductive via fill									

Coupon SL08041A, S1 = L1-L8 PTH with CB100 and S2 = L1-L6 with non-conductive via fill

Table 8

Summary of HATS testing for Polyimide laminate and prepreg
Testing done by MICROTEK Laboratories

Coupon #	**Description**	**Coupon**	**REFLOW pre-condition @ 260°C**	**HATS test to 500 cycles**			
				Net 1 - Through Vias L1-L8	**Net 2 - Through Vias L1-L8**	**Net 3 – Blind Vias L1-L6**	**Net 4 – Blind Vias L1-L7**
1	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
2	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
3	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
4	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
5	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
6	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
7	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
8	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
9	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
10	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
11	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
12	New Approach	HATS_0722	As Is	Pass	Pass	Pass	Pass
13	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
14	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
15	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
16	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
17	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
18	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
19	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
20	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
21	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
22	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
23	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
24	New Approach	HATS_0722	4X	Pass	Pass	Pass	Pass
25	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
26	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
27	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
28	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
29	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
30	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
31	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
32	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
33	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
34	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
35	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass
36	New Approach	HATS_0722	6X	Pass	Pass	Pass	Pass

Table 9

Summary of IST testing for Polyimide laminate and prepreg **Testing done by PWB Interconnect Solutions Inc.**									
Description / Pre-condition	**IST Cycles to Failure - All Data**								
	Coupon	**P1**	**%**	**S1**	**%**	**S2**	**%**	**Comb**	**Result**
New Approach - As Is	**SL08040A_6**	1000	0.1	1000	-0.4	1000	0.1	1000	Accept
New Approach - As Is	**SL08040A_5**	1000	0.1	1000	-0.4	1000	0	1000	Accept
New Approach - As Is	**SL08040A_4**	1000	0	1000	-0.3	1000	-0.1	1000	Accept
New Approach - 3X260°C	**SL08040A_9**	1000	0	1000	0.3	1000	0	1000	Accept
New Approach - 3X260°C	**SL08040A_3**	1000	0.1	1000	-1.1	1000	0	1000	Accept
New Approach - 3X260°C	**SL08040A_1**	1000	0	1000	-1.3	1000	-0.1	1000	Accept
New Approach - 6X260°C	**SL08040A_7**	1000	0.9	1000	2.2	1000	0.7	1000	Accept
New Approach - 6X260°C	**SL08040A_2**	1000	1.1	1000	-0.4	1000	1	1000	Accept
New Approach - 6X260°C	**SL08040A_8**	1000	0.5	1000	0	1000	0.4	1000	Accept
New Approach - As Is	**SL08041A_3**	1000	0.2	1000	0.6	1000	0.2	1000	Accept
New Approach - As Is	**SL08041A_8**	1000	0.2	1000	1.2	1000	0.1	1000	Accept
New Approach - As Is	**SL08041A_9**	1000	0.2	1000	0.2	1000	0.2	1000	Accept
New Approach - 3X260°C	**SL08041A_1**	1000	0.6	1000	0.3	1000	1.2	1000	Accept
New Approach - 3X260°C	**SL08041A_2**	1000	0.3	1000	-1.1	1000	1.9	1000	Accept
New Approach - 3X260°C	**SL08041A_5**	1000	0.6	1000	-0.5	1000	0.5	1000	Accept
New Approach - 6X260°C	**SL08041A_4**	464	10	464	1.1	463	2.3	464	Post
New Approach - 6X260°C	**SL08041A_6**	1000	0.5	1000	-0.6	1000	0.4	1000	Accept
New Approach - 6X260°C	**SL08041A_7**	1000	0.2	1000	-0.7	1000	0.2	1000	Accept
Summary	**Mean**	970	1	970	0	970	1	970	
	Std Dev	126.3	2.3	126.3	0.9	126.6	0.7	126.3	
	Min	464	0	464	-1.3	463	-0.1	464	
	Max	1000	10	1000	2.2	1000	2.3	1000	
Coupon SL08040A, S1 = L1-L8 PTH with CB100 and S2 = L1-L7 with non-conductive via fill									
Coupon SL08041A, S1 = L1-L8 PTH with CB100 and S2 = L1-L6 with non-conductive via fill									

<u>Summary of benefits</u>

- This technology allows the measurement of copper wrap thickness easily with a surface probe. This non-destructive method allows measurements to be taken anywhere on the board and does not require coupon correlation.
- Thickness of initial external surface copper determines the thickness of the copper wrap plate. Overall, surface copper thickness is independent of number of copper wrap plate cycles on any common layer for different filled plated hole structures. This benefit allows fabricators to build HDI designs that are difficult to produce with the increased surface copper resulting from conventional copper wrap plate.
- This technology provides IPC Class 3 copper wrap thickness starting with half-ounce copper foil.
- Copper wrap plate thickness has improved consistency within the panel and from panel-to-panel within a lot. This reduces the overall variation in etched feature dimensions.
- This technology provides thinner overall copper on plated layers, which allows more consistent and predictable dielectrics. This leads to improved impedance control and reduced thickness variation.
- The new process requires less additive plating and subtractive copper etching. This reduces generation of hazardous waste making it a more environmentally responsible process.
- The new technology reduces the overall weight of the PCB's, which can be a benefit in some applications.

Conclusion

There is an increasing need to produce HDI-PCB's with smaller form factors that have higher functionality, better signal integrity and improved thermal management. Designers have adopted the use of blind, buried and through-hole vias as a method to satisfy this growing need. The advent of PCB's designed with via structures coupled with a variety of laminate materials, via fill materials and assembly thermal profiles led to new requirements for ensuring reliability. To address the reliability concern, IPC revised 6012 to Rev B with clarification in amendment 1 to include requirements for copper wrap plating.

The IPC amendment for copper wrap plating improves reliability of via structures. However, conventional techniques for copper wrap plate increase the surface copper thickness restricting fabricators from producing HDI designs with fine line features. The restrictions increase with the number of copper wraps required on common layers for different via-hole structures. In some cases, designs fabricated before the wrap plate amendment was put in place, can no longer be fabricated with the new IPC guidelines for copper wrap plate.

This Technology provides a solution to the Copper Wrap Plate problems. The new technology allows for copper wrap plate without the build up of surface copper thickness. This aspect of this technology provides the benefit of producing highly reliable PCB's without sacrificing fabrication capability.

Acknowledgements

The author wants to thank the members of Technology Team, Operations and Management Groups at DDI, Corp. who all played an integral part to develop this new technology. The author also wants to thank the IPC 6012 committee for the opportunity to present this technology at the 2007 IPC Midwest conference in Chicago and IPC technical publications committee for the opportunity to present this paper at IPC/APEX Expo 2009 conference.

A Novel Approach to Copper Wrap Plate

Author: RAJWANT SIDHU

Copper Wrap Plate - Background Review

- Reliability concerns led to the implementation of wrap plating requirements for via filled plated holes (ref. IPC 6012B Amendment 1 p. 3.6.2.11.1)
  - Class 2 - 0.000197” (5 micron) min. wrap plating
  - Class 3 - 0.000472” (12 micron) min. wrap plating
- Conventional processing methods to satisfy Class 2 and 3 wrap plating requirements limit the FAB suppliers capability for producing surface feature packaging density (LWS)
- The LWS limitations are magnified with designs requiring multiple wrap plating/sequential lamination steps
- As packaging requirements become more dense, the need for sequential laminations and denser LWS is growing
- Constant dialog between design and fab regarding process capabilities to maintain minimum wrap plating thicknesses often lead to design compromises and/or deviations

IPC 6012 SPEC REFERENCES – Copper Wrap Plate

3.6.2.11.1 Copper Wrap Plating Copper wrap plating minimum as specified in Table 3-2 **shall** be continuous from the filled plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] where an annular ring is required (see Figures 3-13 and 3-14). Reduction of wrap-plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed (see Figure 3-15).

Add new Figure 3-13 as follows:

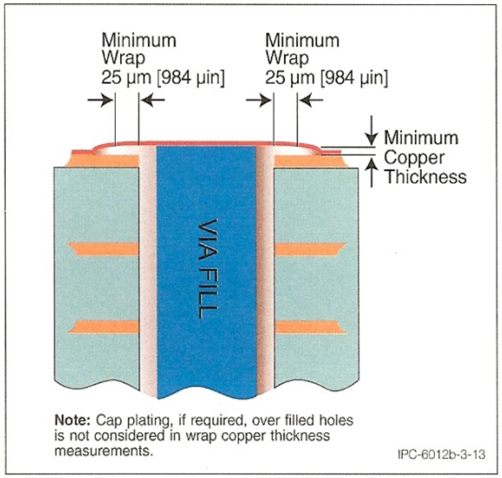


Figure 3-13 Surface Copper Wrap Measurement (Applicable to all filled plated-through holes)

Add new Figure 3-14 as follows:

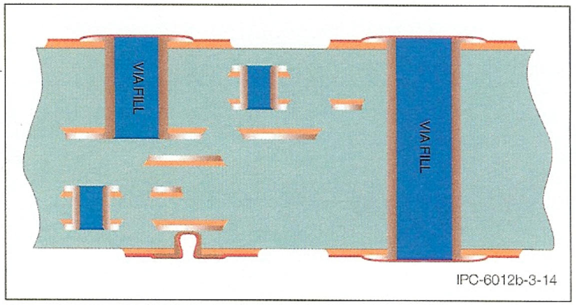


Figure 3-14 Wrap Copper in Type 4 PCB (Acceptable)

Add new Figure 3-15 as follows:

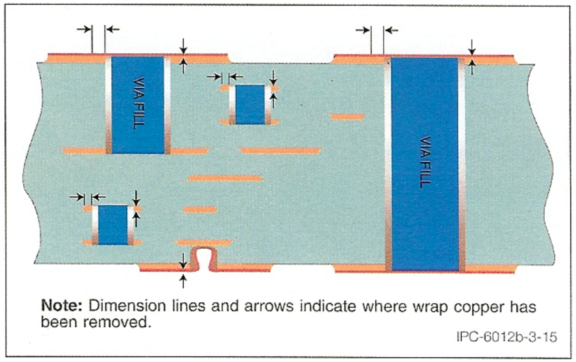


Figure 3-15 Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)

3.6.2.13 Minimum Surface Conductor Thickness The minimum total (copper foil plus copper plating) conductor thickness after processing **shall** be in accordance with Table 3-8. When the procurement documentation specifies a minimum copper thickness for external conductors, the test coupon or production board **shall** meet or exceed that minimum thickness. The minimum surface conductor thickness after processing values given in Table 3-8 are determined by the following equation:

Minimum Surface Conductor Thickness = a + b - c

Where:

a = Absolute copper foil minimum (IPC-4562 nominal less 10% reduction).

b = Minimum copper plating thickness (20 µm [787 µin] for Class 1 and 2; 25 µm [984 µin] for Class 3).

c = A maximum variable processing allowance reduction.

3.2.6.2 Additive Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification.

Common Problems with Conventional Copper Wrap Plate Processing (cont.)

- Example of plating separation following thermal stress - (Fig. 1)
- Wrap plating was removed due to excessive sanding / planarization
- Process control techniques are costly and time consuming
- Current process control techniques are not 100% representative of the entire panel
- Even with wrap plating – evidence of starter cracks and full separation have been observed - (Fig. 2 and Fig. 3)
- Experience has shown that choice of via fill material and wrap plating thickness are key factors in ability to withstand thermal stress
- Due to surface density requirements often times design compromises are implemented
  - Reduced wrap thickness, class 2 vs. class 3
  - Alternate packaging with wider LWS
  - Reduced starting foil thickness

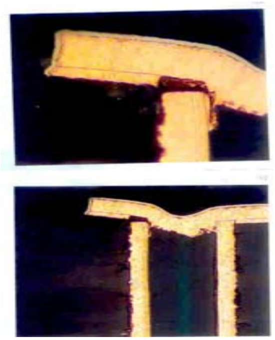


Fig. 1

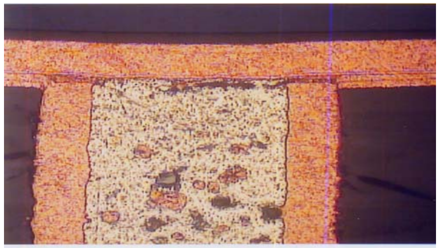


Fig. 2

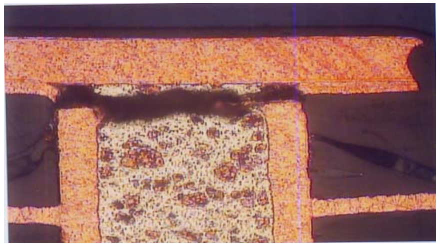
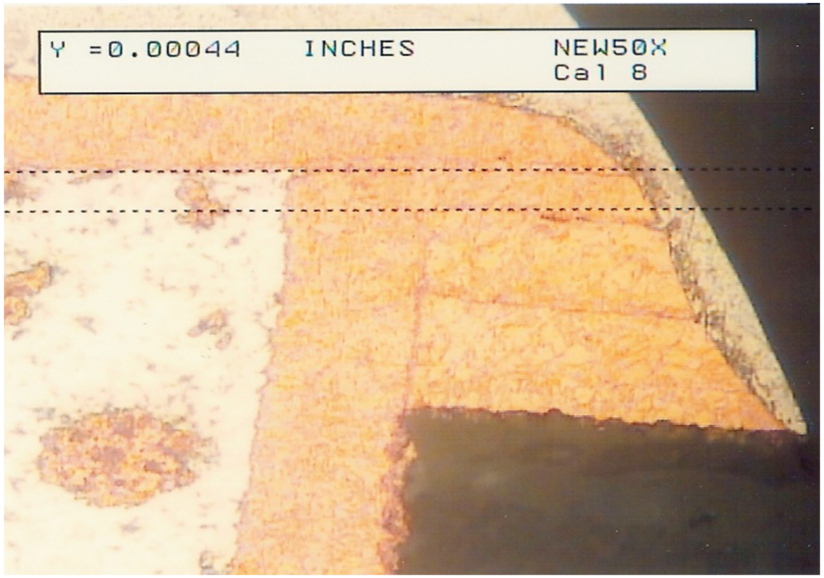
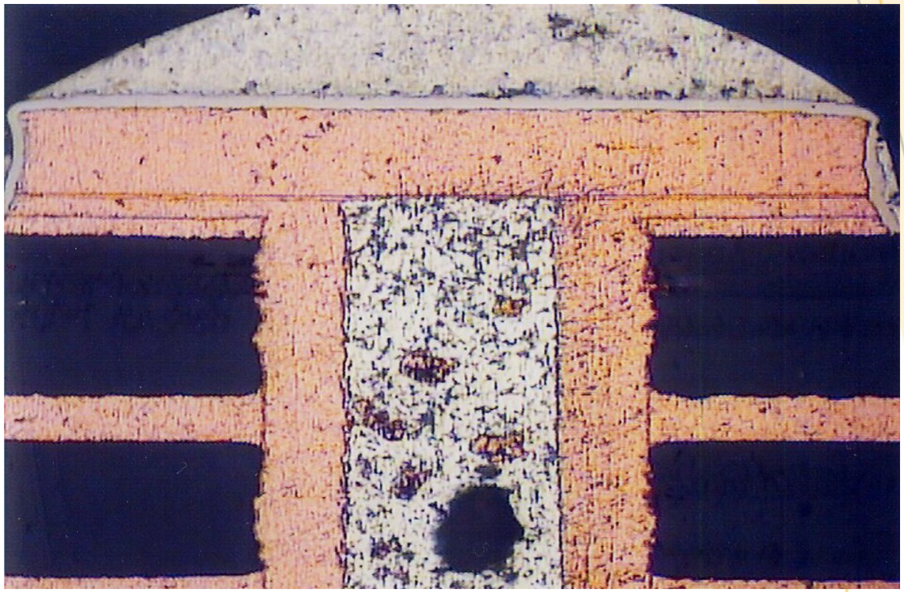


Fig. 3

Common Problems with Conventional Copper Wrap Plate Processing

- Wrap plating onto the surface increases panel copper thickness
- Increased etch factors / process allowances are required due to thicker finished surface copper





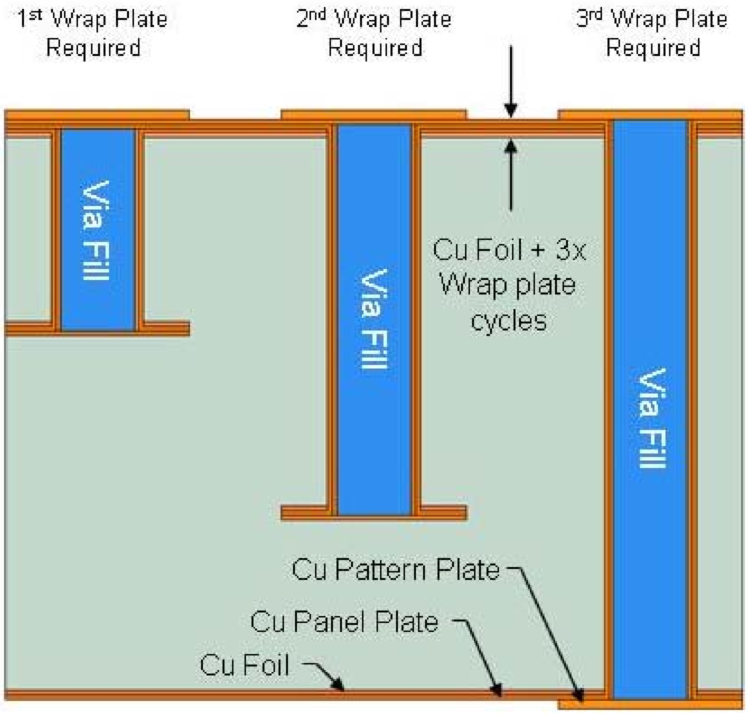
- Issue is magnified on products requiring multiple lamination steps
- Third wrap plating thickness is below 0.000472” (12 micron) min. Class 3 requirement

A *Novel* APPROACH to *Copper Wrap Plate*

The technology developed by DDI Corporation offers a wrap copper solution that does not require the build-up of surface copper. This allows the desired improvement in reliability without sacrificing the ability to manufacture designs with fine features. ***This technology*** *also improves quality control and production reproducibility by permitting non-destructive real time thickness measurements during fabrication. Copper Wrap thickness for* ***this system*** *can be measured with a standard surface copper probe instead of the current conventional method that requires destructive micro-section analysis. PCB fabrication using* ***this technology*** *also allows wrap thickness to be controlled and varied by simply changing the outer copper foil thickness. In PCB designs requiring multiple Copper Wrap Plates, the benefits of this technology are increasingly attractive.*

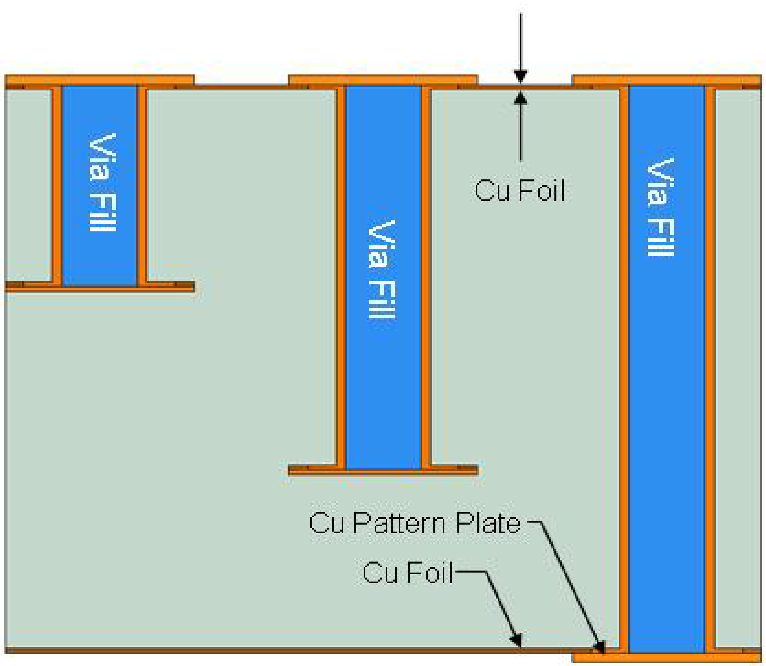
Conventional vs. *NEW APPROACH*
Surface Copper Build-up Comparison (Schematic)

Conventional Wrap Plating
(3x wrap on a common layer)



Total surface copper after 3x wrap

FLAT-WRAP™
(Patent Pending)
(3x wrap on a common layer)

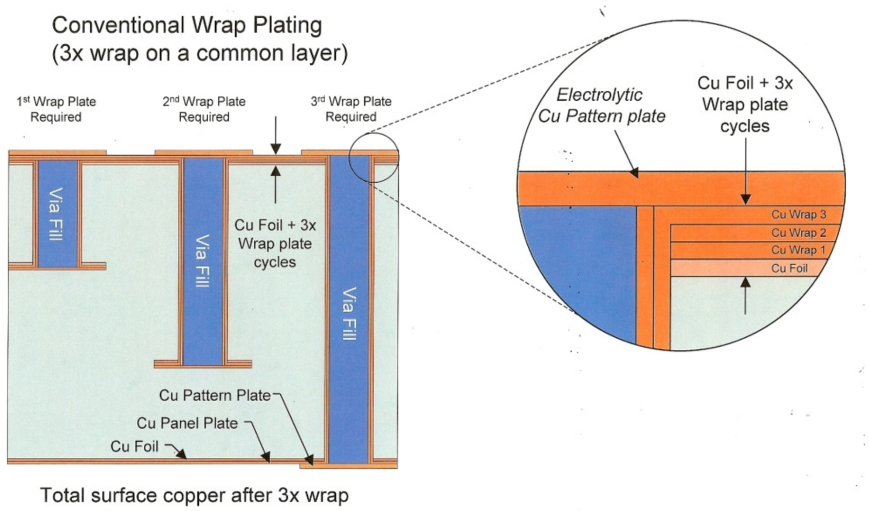


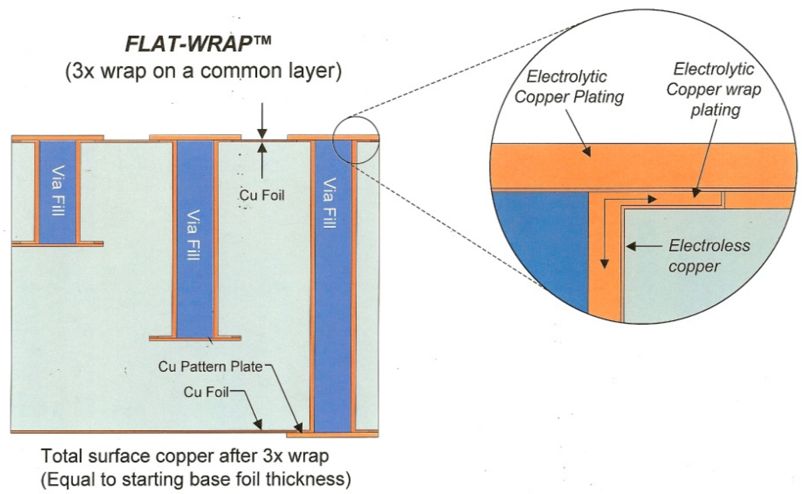
Total surface copper after 3x wrap

Conventional vs. *NEW APPROACH*
Surface Copper Build-up Comparison (Schematic)

Conventional Wrap Plating
(3x wrap on a common layer)

FLAT-WRAP™
(Patent Pending)
(3x wrap on a common layer)





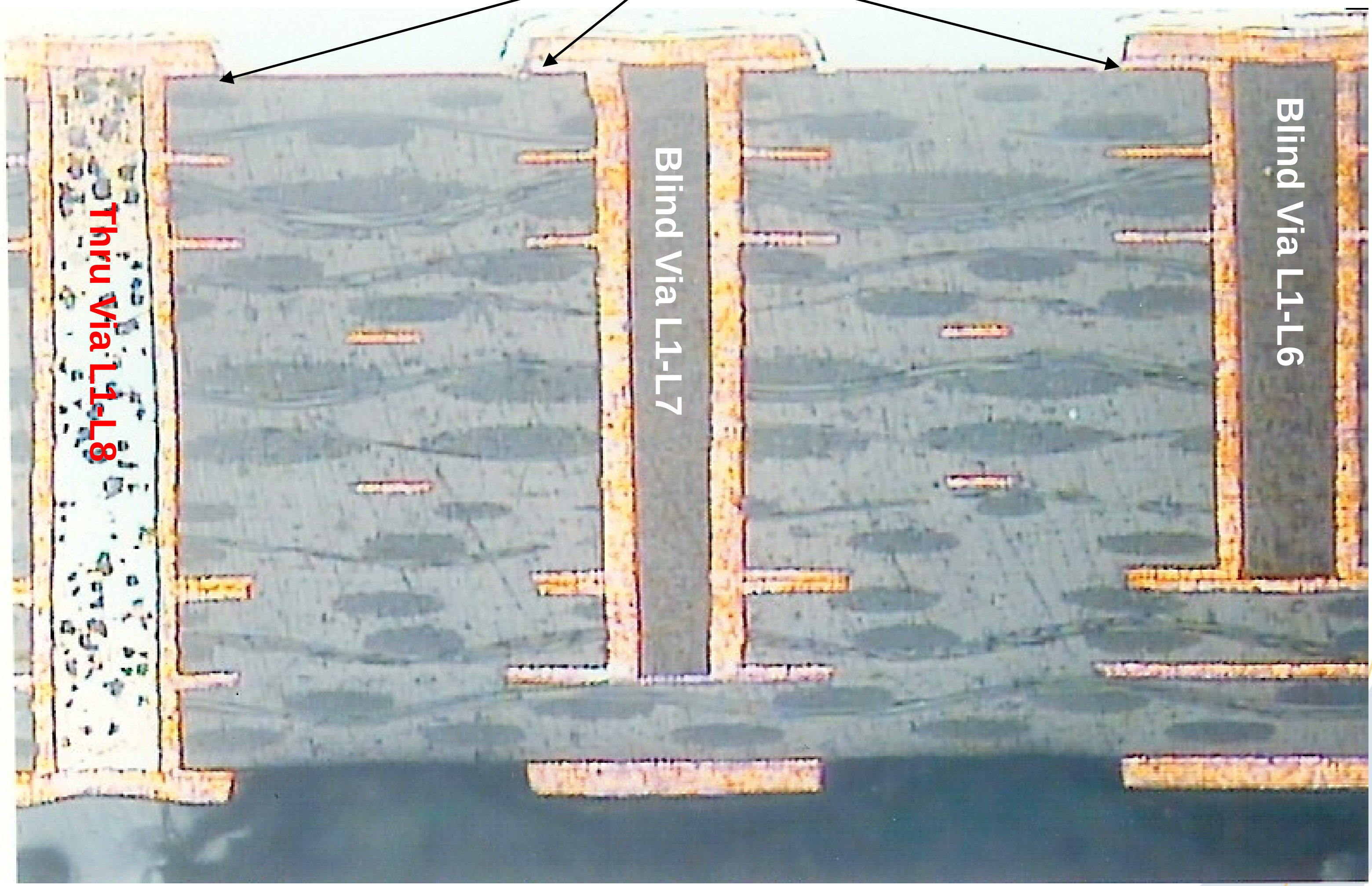
Conventional vs. *NEW APPROACH*
Surface Measurement Reading comparison

New Approach Measurement reading

Conventional Wrap Measurement reading

New Copper Wrap Plate Technology – In Process

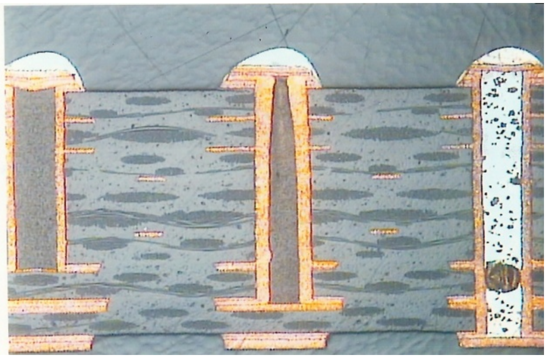
Copper Foil / Copper Wrap Plate

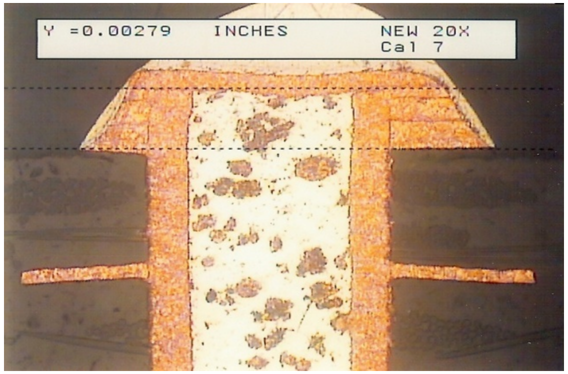


Thermal Stress 6X @ 550 F, 10 seconds each

Conventional vs. *NEW APPROACH*
Surface Copper Build-up Comparison – In Process

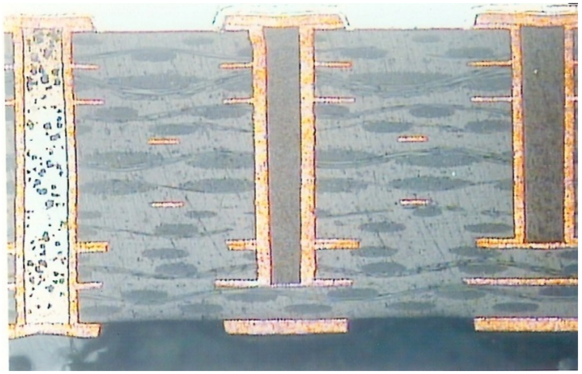
Conventional Copper Wrap Plate
(3x wrap on a common layer)

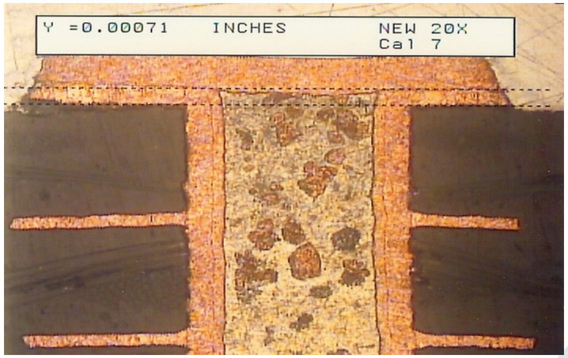




0.012” (305 micron) finished pad dia.

New Copper Wrap Plate Technology
(3x wrap on a common layer)

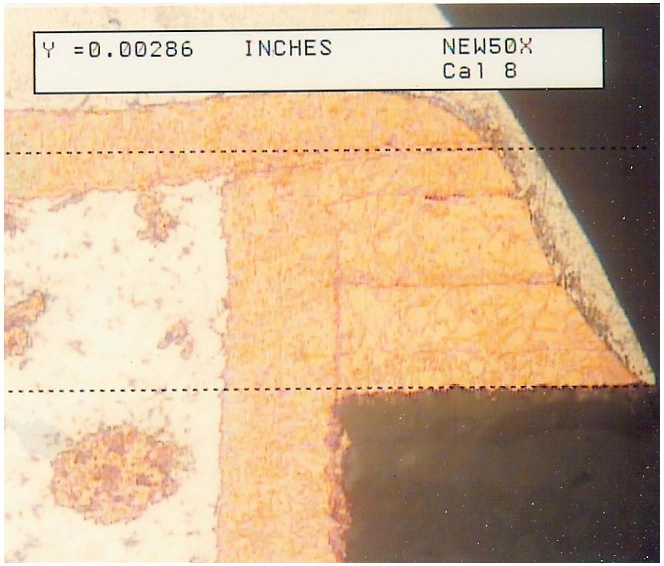




0.018” (457 micron) finished pad dia.

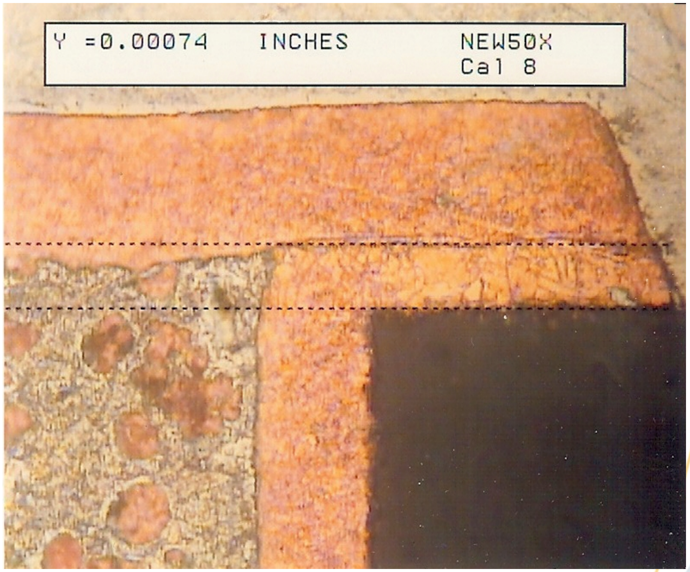
Conventional vs. *NEW APPROACH*
Surface Copper Build-up Comparison - In Process

Conventional Copper Wrap Plate
(3x wrap + Foil on a common layer)



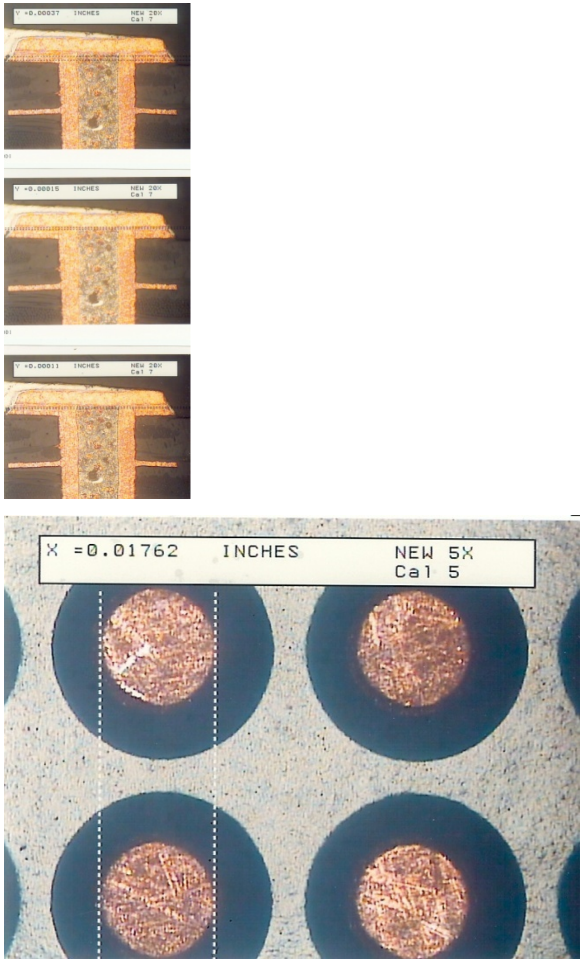
Surface Copper Thickness
~ 0.0022” (56 micron) minimum
~ 0.003” - 0.004”
(75 - 100 micron) typical

New Copper Wrap Plate Technology
(3x wrap + Foil on a common layer)

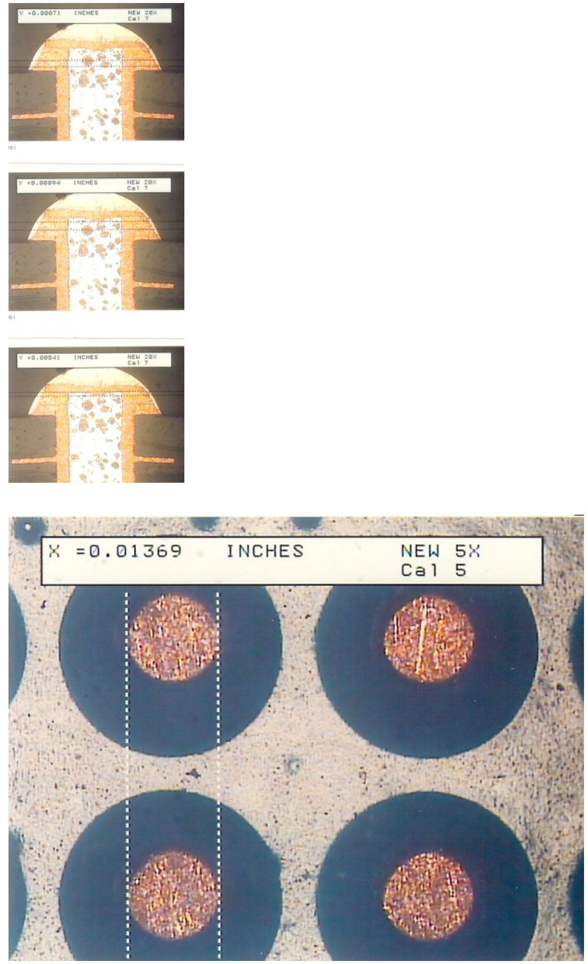


Surface Copper Thickness
~ 0.0007” (18 micron) typical

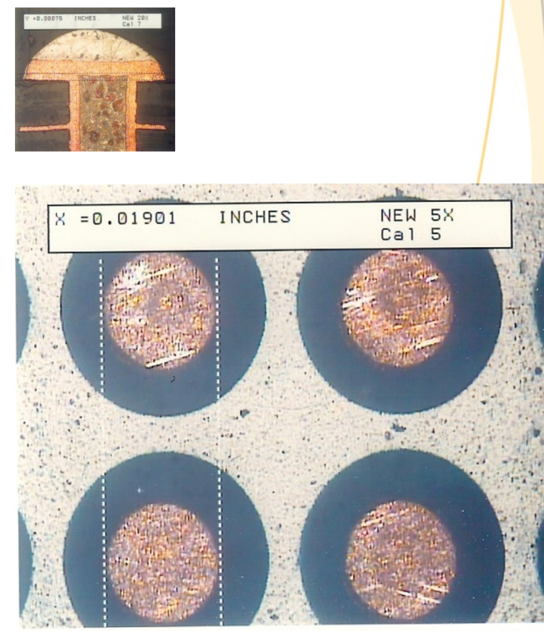
Conventional vs. New Technology Pad Size & Pad Height Comparison



CONVENTIONALCLASS 2 WRAP

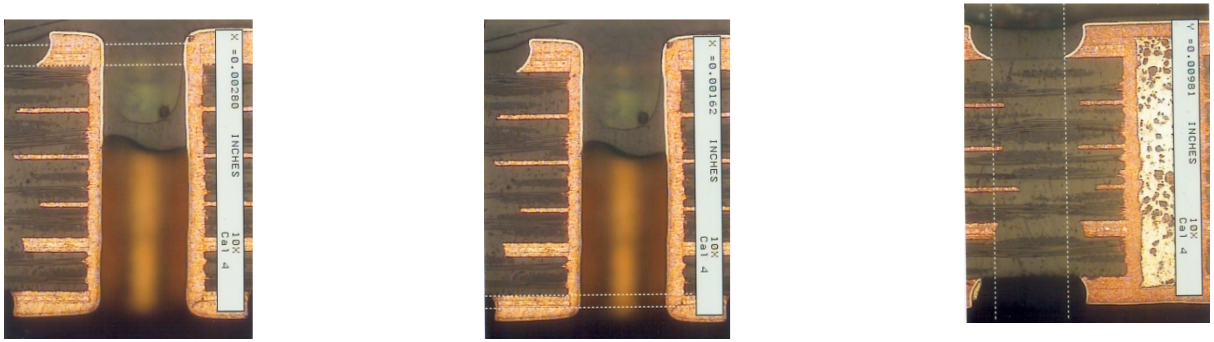


CONVENTIONALCLASS 3 WRAP



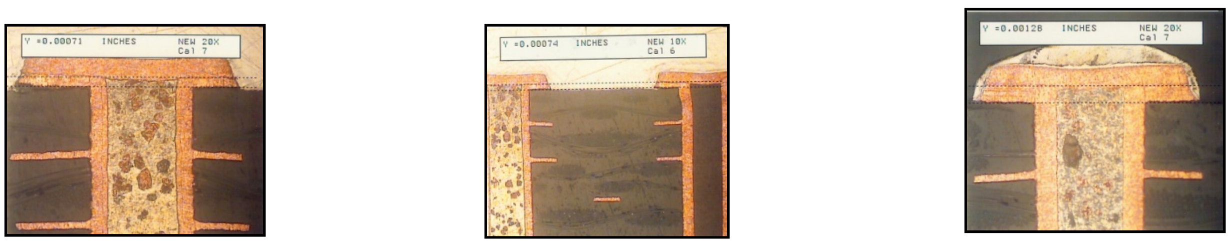
NEW TECHNOLOGY CLASS 3 WRAP

Pictures from New Technology and Conventional Copper Wrap Plate (Cont.)



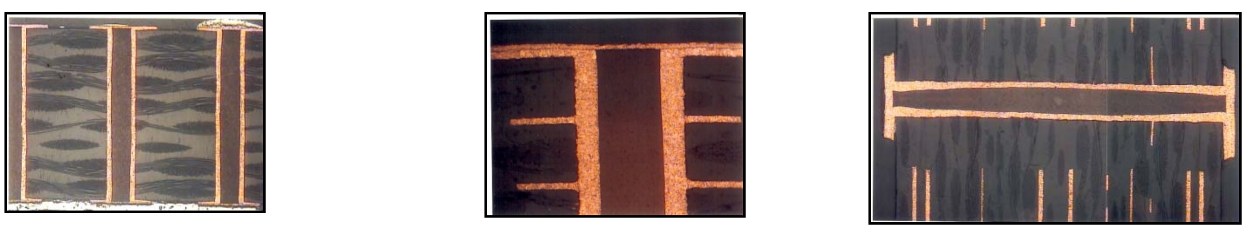
Conventional Wrap 2x-Side 1/1x-Side 2

Copper height to etch through - Side 1 vs. Side 2) & Reduced Spacing on 2x Wrap Side



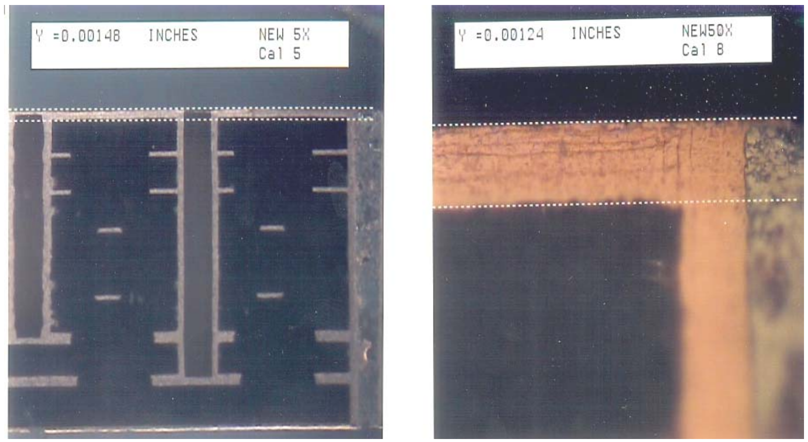
New Technology 3x Wrap – No Copper Build up over Foil

(Copper Height to etch for 1x, 2x, 3x, or nx wrap remains the same)



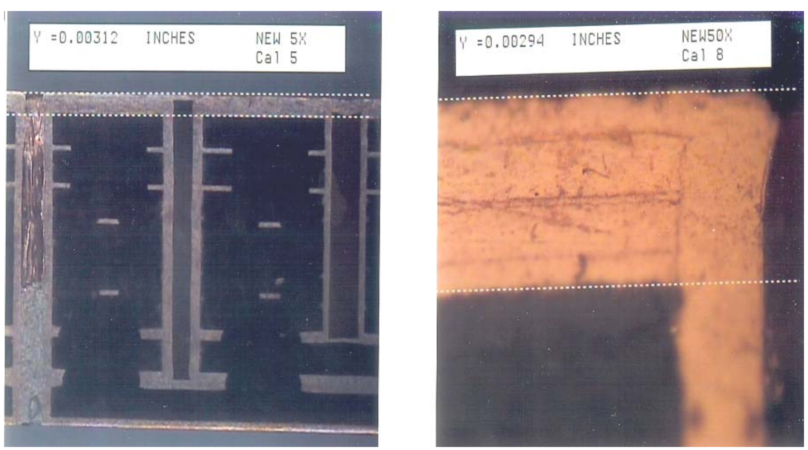
New Technology 1x Wrap – No Copper Build up over surface copper

Pictures from New Technology and Conventional Copper Wrap Plate



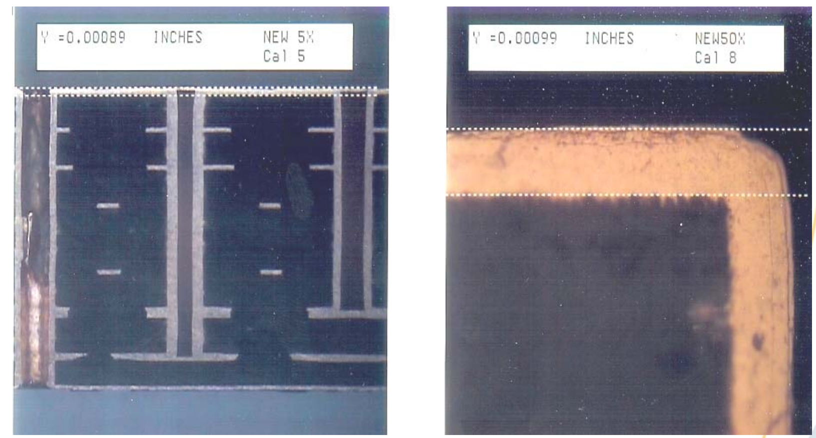
3 Via sets with a common Layer Class 2 Wrap

(Conventional Wrap)



3 Via sets with a common Layer Class 3 Wrap

(Conventional Wrap)



3 Via sets with a common Layer Class 3 Wrap

(New Technology)

Wrap Plating Design Guidelines Comparison

Conventional Wrap Plate Design Guidelines

Design Rule	IPC 6012B Class 2 - assume a starting copper foil of 3/8 oz				IPC 6012B Class 3 - assume a starting copper foil of 3/8 oz			
	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater
Preferred	0.003" Line	0.005" Line	0.006" Line	0.006" Line	0.003" Line	0.005" Line	0.006" Line	Call
	0.0035" Space	0.005" Space	0.007" Space	0.009" Space	0.0035" Space	0.00575" Space	0.0085" Space	
Advanced capability = reduced yield (call engineering prior to quote)	0.003" Line	0.004" Line	0.005" Line	0.006" Line	0.003" Line	0.005" Line	0.006" Line	Call
	0.003" Space	0.005" Space	0.006" Space	0.008" Space	0.003" Space	0.0055" Space	0.0075" Space	

Note: Due to the overhang (caused by undercut during etch) all Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012B, Class 2 or 3 specification, will need engineering approval prior to quote……no exceptions

FLAT-WRAP™ Technology Design Guidelines

Design Rule	IPC 6012B Class 2 - Starting copper weight 3/8 oz				IPC 6012B Class 3 - Starting copper weight 1/2 oz			
	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater
Preferred	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.0035" Line	0.0035" Line	0.0035" Line	0.0035" Line
	0.0035" Space	0.0035" Space	0.0035" Space	0.0035" Space	0.004" Space	0.004" Space	0.004" Space	0.004" Space
Advanced capability = reduced yield (call engineering prior to quote)	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line
	0.003" Space	0.003" Space	0.003" Space	0.003" Space	0.0035" Space	0.0035" Space	0.0035" Space	0.0035" Space

Note: Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012B, Class 2 or 3 specification, will not need engineering approval if PCB's are fabricated with **this new t**echnology

New Technology - Solution for fine pitch features on Buried Vias
16 Layer, 2+N+2

Microsection After Buried Via (New Technology) Cycled To Failure

# of HATS cycles passed = 0.008" – 2,604 & 0.010" – 3,278

Lyr# Type:	Lam Cycles:	Description:	Copper:	Laminate / PrePreg:	Base Material:
	21				
1 Sig		Foil (T oz)	.00045		
		Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
		Sub Plating	.00100		
2 Sig		Foil (T oz)	.00045		
		Preg(1x1080)		.0025 +/- 0.0005	Polyclad FR370 HR
3 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
4 Mix			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
5 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
6 Sig			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
7 Mix		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
8 Sig			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
9 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
10 Mix			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
11 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
12 Sig			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
13 Mix		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
14 Sig			.00060		
		Preg(1x1080)		.0025 +/- 0.0005	Polyclad FR370 HR
15 Sig		Foil (T oz)	.00045		
		Sub Plating	.00100		
		Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
16 Sig		Foil (T oz)	.00045		
	21				

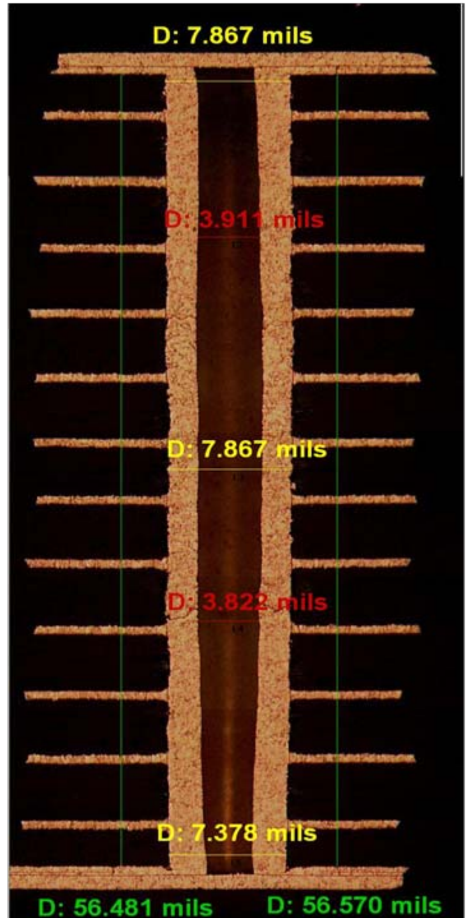
Drill: Plated / CondFill / NonCond — Laser: Plated / SMV — Impedance Layers

Impedance Requirements: L# / Impedance Type	Original Line	Finish Line	1st Ref. Pln.	2nd Ref. Pln.	Z-Ohms (Calc'd)	Z Ohms & Tolerances (+/-%) (Required)	Diff Center to Center	Coplanar Spacing (Original)	Coplanar Spacing (Finished)

Controlled Impedance Notes:

Stackup Notes:

- CAUTION: MIN. DIELECTRICS BETWEEN 1-2, 2-3, 14-15 & 15-16 ARE .0019.

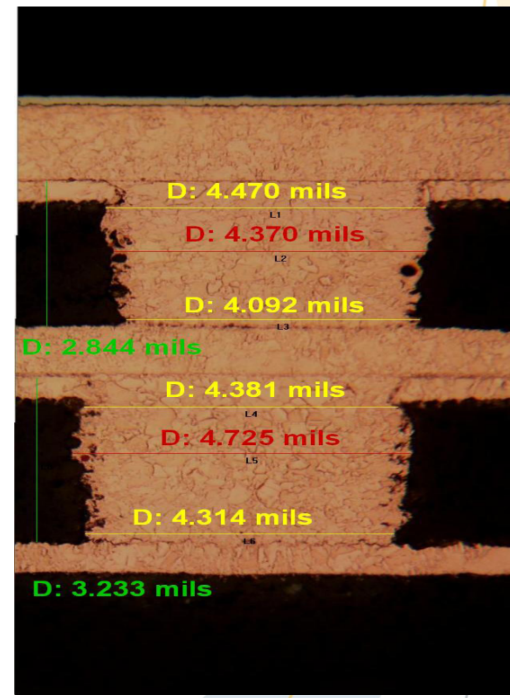


Stacked MicroVia

L1-L2/L2-L3

0.004" & 0.005" vias

Passed 5,000 HATS cycle



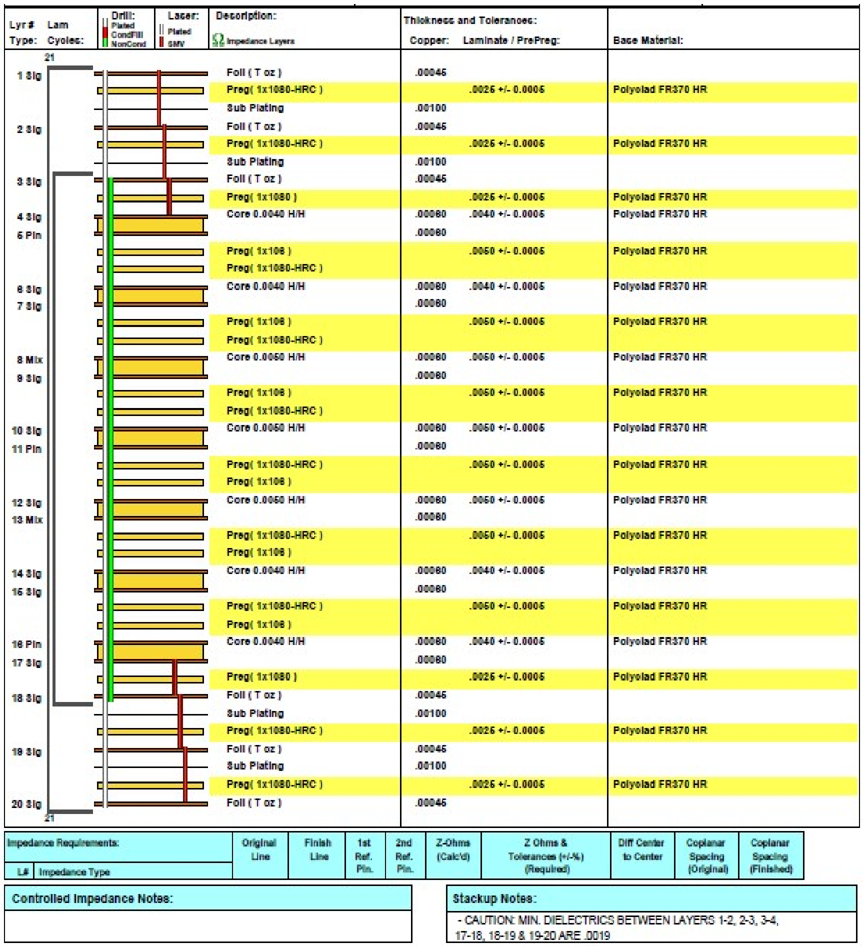
16 Layer, 2+N+2, Stacked MicroVia / Staggered Buried Via

PCB Thickness 0.072" +/- 10%

New Technology - Solution for fine pitch features on Buried Vias
20 Layer, 3+N+3

Microsection After Buried Via (New Technology) Cycled To Failure

# of HATS cycles passed = 0.010” – 1,337 & 0.012” – 1,716



Lyr # Type:	Lam Cycles:	Description:	Copper:	Laminate / PrePreg:	Base Material:
	21				
1 Sig		Foil (T oz)	.00045		
		Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
		Sub Plating	.00100		
2 Sig		Foil (T oz)	.00045		
		Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
		Sub Plating	.00100		
3 Sig		Foil (T oz)	.00045		
		Preg(1x1080)		.0025 +/- 0.0005	Polyclad FR370 HR
4 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
5 Pln			.00060		
		Preg(1x106)		.0050 +/- 0.0005	Polyclad FR370 HR
		Preg(1x1080-HRC)			
6 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
7 Sig			.00060		
		Preg(1x106)		.0050 +/- 0.0005	Polyclad FR370 HR
		Preg(1x1080-HRC)			
8 Mix		Core 0.0050 H/H	.00060	.0050 +/- 0.0005	Polyclad FR370 HR
9 Sig			.00060		
		Preg(1x106)		.0050 +/- 0.0005	Polyclad FR370 HR
		Preg(1x1080-HRC)			
10 Sig		Core 0.0050 H/H	.00060	.0050 +/- 0.0005	Polyclad FR370 HR
11 Pln			.00060		
		Preg(1x1080-HRC)		.0050 +/- 0.0005	Polyclad FR370 HR
		Preg(1x106)			
12 Sig		Core 0.0050 H/H	.00060	.0050 +/- 0.0005	Polyclad FR370 HR
13 Mix			.00060		
		Preg(1x1080-HRC)		.0050 +/- 0.0005	Polyclad FR370 HR
		Preg(1x106)			
14 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
15 Sig			.00060		
		Preg(1x1080-HRC)		.0050 +/- 0.0005	Polyclad FR370 HR
		Preg(1x106)			
16 Pln		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
17 Sig			.00060		
		Preg(1x1080)		.0025 +/- 0.0005	Polyclad FR370 HR
18 Sig		Foil (T oz)	.00045		
		Sub Plating	.00100		
		Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
19 Sig		Foil (T oz)	.00045		
		Sub Plating	.00100		
		Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
20 Sig		Foil (T oz)	.00045		
	21				

Impedance Requirements: L#	Impedance Type	Original Line	Finish Line	1st Ref. Pln.	2nd Ref. Pln.	Z-Ohms (Calc'd)	Z Ohms & Tolerances (+/-%) (Required)	Diff Center to Center	Coplanar Spacing (Original)	Coplanar Spacing (Finished)

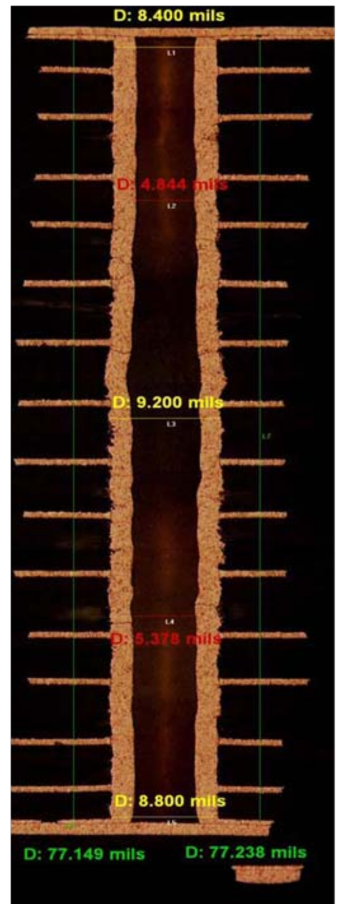
Controlled Impedance Notes:

Stackup Notes:

- CAUTION: MIN. DIELECTRICS BETWEEN LAYERS 1-2, 2-3, 3-4, 17-18, 18-19 & 19-20 ARE .0019

20 Layer, 3+N+3, Stacked MicroVia / Staggered Buried Via

PCB Thickness 0.097” +/- 10%



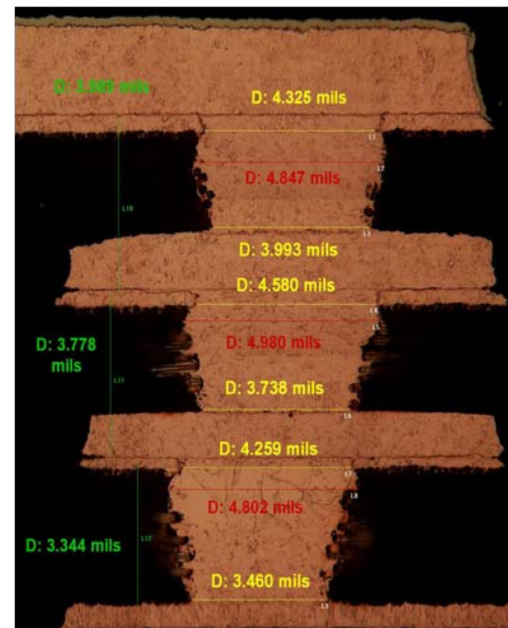
Stacked MicroVia

L1-L2/L2-L3/L3-L4

# of HATS cycle passed

0.004” vias – 3,513

0.005” vias – 5,000



New Copper Wrap Plate - Reliability Test Matrix
High Tg FR4 Laminate Material

<table>
<tr><th colspan="5">Description of Tests</th><th>Remarks</th><th>Test Status</th><th>Test Results</th></tr>
<tr><td>Manufacturability Tests</td><td>As received - Microsection PTH Quality</td><td>Plated Barrel Copper Thickness</td><td colspan="2">Record Avg Plating Thickness</td><td>Microsection analysis performed by DDi</td><td>Completed</td><td>Passed</td></tr>
<tr><td rowspan="6">Pb-Free Assy Process Compatibility</td><td rowspan="4">Solder Float Test - Microsection PTH Quality</td><td rowspan="4">Temperature Deg C (Deg F)</td><td rowspan="2">260 (500)</td><td>3X</td><td>BGA coupons - DDi</td><td>Completed</td><td>Passed</td></tr>
<tr><td>6X</td><td>BGA coupons - DDi</td><td>Completed</td><td>Passed</td></tr>
<tr><td rowspan="2">288 (550)</td><td>3X</td><td>BGA coupons - DDi</td><td>Completed</td><td>Passed</td></tr>
<tr><td>6X</td><td>BGA coupons - DDi</td><td>Completed</td><td>Passed</td></tr>
<tr><td rowspan="2">Pb Free Reflow Assembly Simulation</td><td rowspan="2">Temperature Deg C (Deg F)</td><td rowspan="2">260 (500)</td><td>4X</td><td rowspan="2">Microtek Labs to process BGA coupons through Pb Free profile through IR Reflow oven and DDi to do microsection analysis</td><td rowspan="2">Completed</td><td>Passed</td></tr>
<tr><td>6X</td><td>Passed</td></tr>
<tr><td rowspan="7">Reliability Tests</td><td rowspan="4">IST - Interconnect Stress Test</td><td rowspan="2">IST Pre-conditioning cycles at 260 C</td><td colspan="2">4X</td><td rowspan="2">3 coupons / preconditioning (Total of 18 coupons). Dual sense test performed by DDi VA. Two different test conditions with conductive and non-conductive via fill materials</td><td rowspan="2">Completed & Reported by Avg Cycles</td><td rowspan="2">Blind Vias No Failure & Thru Vias Pass 864 @ 6X & 1176 @ 4X</td></tr>
<tr><td colspan="2">6X</td></tr>
<tr><td rowspan="2">Pb Free Assembly Profile Pre-conditioning, peak temp 260 C</td><td colspan="2">4X</td><td rowspan="2">IST testing to be perfromed by PWB Corp, Dual Sense to 1000 cycles</td><td rowspan="2">Completed & Reported by Avg Cycles</td><td rowspan="2">Blind Vias No Failure & Thru Vias Pass 731 @ 6X & No Failure @ 4X</td></tr>
<tr><td colspan="2">6X</td></tr>
<tr><td rowspan="3">HATS - Highly Accelerated Thermal Shock</td><td rowspan="3">Pb Free Assembly Profile Pre-conditioning, peak temp 260 C</td><td colspan="2">0</td><td rowspan="3">12 coupons tested. Test performed by Microtek Labs. Two different test conditions with San-Ei & CB100 via fill materials</td><td rowspan="3">Coupons tested by MicroTek to 1000 cycles</td><td>Passed</td></tr>
<tr><td colspan="2">4X</td><td>Passed</td></tr>
<tr><td colspan="2">6X</td><td>987 average cycles</td></tr>
</table>

Reliability Test Data (FR4) – HATS & IST with Pb Free pre-conditioning

Summary of HATS testing for High Tg FR4 laminate and prepreg. Testing done by Microtek Labs

Coupon #	Description	Coupon	Reflow pre-condition @ 260 C	HATS test to 500 cycles			
				Net 1 - Through Vias L1-L8	Net 2 - Through Vias L1-L8	Net 3 - Blind Vias L1-L6	Net 4 - Blind Vias L1-L7
1	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	3
2	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	Pass
3	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	Pass
4	Conventional IPC Class 2	HATS_0722	6x	Pass	Pass	Pass	Pass
5	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
6	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
7	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
8	Conventional IPC Class 3	HATS_0722	6x	Pass	Pass	Pass	Pass
9	*New Approach*	HATS_0722	6x	Pass	Pass	Pass	Pass
10	*New Approach*	HATS_0722	6x	Pass	Pass	Pass	Pass
11	*New Approach*	HATS_0722	6x	Pass	Pass	Pass	Pass
12	*New Approach*	HATS_0722	6x	Pass	Pass	Pass	Pass
13	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	123
14	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	Pass
15	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	Pass
16	Conventional IPC Class 2	HATS_0722	4x	Pass	Pass	Pass	Pass
17	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	Pass
18	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	Pass
19	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	Pass
20	Conventional IPC Class 3	HATS_0722	4x	Pass	Pass	Pass	N/A
21	*New Approach*	HATS_0722	4x	Pass	Pass	Pass	Pass
22	*New Approach*	HATS_0722	4x	Pass	Pass	Pass	Pass
23	*New Approach*	HATS_0722	4x	Pass	Pass	Pass	Pass
24	*New Approach*	HATS_0722	4x	Pass	Pass	Pass	Pass
25	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
26	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
27	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
28	Conventional IPC Class 2	HATS_0722	As is	Pass	Pass	Pass	Pass
29	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
30	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
31	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
32	Conventional IPC Class 3	HATS_0722	As is	Pass	Pass	Pass	Pass
33	*New Approach*	HATS_0722	As is	Pass	Pass	Pass	Pass
34	*New Approach*	HATS_0722	As is	Pass	Pass	Pass	Pass
35	*New Approach*	HATS_0722	As is	Pass	Pass	Pass	Pass
36	*New Approach*	HATS_0722	As is	Pass	Pass	Pass	Pass

Summary of IST testing for High Tg FR4 laminate and prepreg. Testing done by PWB Corp.

Description / Pre-condition	IST Cycles to Failure - All Data								
	Coupon	P1	%	S1	%	S2	%	Comb	Result
New Approach - 4X260C	SL08041A_1	1000	-1.1	1000	0	1000	-1.1	1000	Accept
New Approach - 4X260C	SL08041A_2	1000	-0.1	1000	1.5	1000	-0.1	1000	Accept
New Approach - 4X260C	SL08041A_3	1000	-0.1	1000	1	1000	-0.5	1000	Accept
IPC Class 2 - 4X260C	SL08040A_1	1000	-0.1	1000	-0.1	1000	0.1	1000	Accept
IPC Class 2 - 4X260C	SL08040A_2	627	10	627	-0.3	627	-0.2	627	Post
IPC Class 2 - 4X260C	SL08040A_3	1000	0.1	1000	0	1000	-0.6	1000	Accept
IPC Class 3 - 4X260C	SL08040A_1	1000	0	1000	0	1000	0	1000	Accept
IPC Class 3 - 4X260C	SL08040A_2	1000	0	1000	0	1000	0	1000	Accept
IPC Class 3 - 4X260C	SL08040A_3	1000	0	1000	0	1000	0	1000	Accept
New Approach - 6X260C	SL08040A-1	1000	0.5	677	10	1000	-0.1	677	S1
New Approach - 6X260C	SL08040A-2	1000	1	594	10	1000	-0.1	594	S1
New Approach - 6X260C	SL08040A_3	1000	1	923	10	1000	0	923	S1
IPC Class 2 - 6X260C	SL08040A_1	1000	1.7	1000	1.3	1000	1.4	1000	Accept
IPC Class 2 - 6X260C	SL08040A_2	397	10	397	-0.2	397	0.1	397	Post
IPC Class 2 - 6X260C	SL08040A_3	1000	0.5	1000	0.6	1000	0.8	1000	Accept
IPC Class 3 -6X260C	SL08040A_1	1000	0.9	1000	0.8	1000	1.3	1000	Accept
IPC Class 3 - 6X260C	SL08040A_2	1000	6	1000	0.4	1000	1.1	1000	Accept
IPC Class 3 - 6X260C	SL08040A_3	1000	0.8	1000	0.8	1000	1.1	1000	Accept
New Approach - 4X260C	SL08041A_1	1000	1.1	1000	1.6	1000	1.4	1000	Accept
New Approach - 4X260C	SL08041A_2	1000	3.6	1000	1	1000	1.5	1000	Accept
New Approach - 4X260C	SL08041A_3	1000	2.2	1000	4.3	1000	3.5	1000	Accept
New Approach - 6X260C	SL08041A_1	1000	-0.1	1000	2.5	1000	0.1	1000	Accept
New Approach - 6X260C	SL08041A_2	1000	-0.6	1000	-0.2	1000	-0.4	1000	Accept
New Approach - 6X260C	SL08041A_3	1000	1.8	1000	0.5	1000	0	1000	Accept
Summary		**Mean**		**Std Dev**		**Min cycles**		**Max cycles**	
Conventional IPC Class 2, P1		837.3		262.3		397		1000	
Conventional IPC Class 3, P1		1000		0		1000		1000	
New Approach, P1		1000		0		1000		1000	
Conventional IPC Class 2, S1		837.3		262.3		397		1000	
Conventional IPC Class 3, S1		1000		0		1000		1000	
New Approach, S1		932.83		141.72		594		1000	
Conventional IPC Class 2, S2		837.3		262.3		397		1000	
Conventional IPC Class 3, S2		1000		0		1000		1000	
New Approach, S2		1000		0		1000		1000	
Coupon SL08040A, S1 = L1-L8 PTH with Conductive and S2 = L1-L7 with Non-Conductive Via Fill									
Coupon SL08041A, S1 = L1-L8 PTH with Conductive and S2 = L1-L6 with Non-Conductive Via Fill									

New Copper Wrap Plate - Reliability Test Matrix
Glass Reinforced Polyimide Laminate Material

Description of Tests					Remarks	Test Status	Test Results
Manufacturability Tests	As received - Microsection PTH Quality	Plated Barrel Copper Thickness	Record Avg Plating Thickness		Microsection analysis performed by DDi	Completed	Passed
Pb-Free Assy Process Compatibility	Solder Float Test - Microsection PTH Quality	Temperature Deg C (Deg F)	260 (500)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
			288 (550)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
	Pb Free Reflow Assembly Simulation	Temperature Deg C (Deg F)	260 (500)	4X	Microtek Labs to process BGA coupons through Pb Free profile through IR Reflow oven and DDi to do microsection analysis	Completed	Passed
				6X			Passed
Reliability Tests	IST - Interconnect Stress Test	IST Pre-conditioning cycles at 260 C	3X		6 coupons / preconditioning (Total of 18 coupons). Dual sense test performed by PWB Corp. Two different test conditions with conductive and non-conductive via fill materials	Completed & Reported by Avg Cycles	Blind Vias & Thru Vias Pass 1000 @ As Is & 4X and 970 @ 6X
			6X				
	HATS - Highly Accelerated Thermal Shock	Pb Free Assembly Profile Pre-conditioning, peak temp 260 C	0		36 coupons tested. Test performed by Microtek Labs. Two different test conditions with conductive and non-conductive via fill materials	Coupons tested by MicroTek to 500 cycles	Passed
			4X				Passed
			6X				Passed

Reliability Test Data (Polyimide) – HATS & IST with Pb Free pre-conditioning

Summary of HATS testing for Polyimide laminate and prepreg. Testing done by Microtek Labs.

Coupon #	Description	Coupon	REFLOW pre-condition @ 260 C	HATS test to 500 cycles			
				Net 1 - Through Vias L1-L8	Net 2 - Through Vias L1-L8	Net 3 - Blind Vias L1-L6	Net 4 - Blind Vias L1-L7
1	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
2	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
3	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
4	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
5	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
6	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
7	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
8	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
9	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
10	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
11	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
12	*New Approach*	HATS_0722	As Is	Pass	Pass	Pass	Pass
13	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
14	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
15	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
16	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
17	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
18	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
19	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
20	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
21	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
22	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
23	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
24	*New Approach*	HATS_0722	4X	Pass	Pass	Pass	Pass
25	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
26	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
27	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
28	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
29	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
30	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
31	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
32	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
33	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
34	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
35	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass
36	*New Approach*	HATS_0722	6X	Pass	Pass	Pass	Pass

Summary of IST testing for Polyimide laminate and prepreg. Testing done by PWB Corp.

Description / Pre-condition	IST Cycles to Failure - All Data								
	Coupon	P1	%	S1	%	S2	%	Comb	Result
New Approach - As Is	**SL08040A_6**	1000	0.1	1000	-0.4	1000	0.1	1000	Accept
New Approach - As Is	**SL08040A_5**	1000	0.1	1000	-0.4	1000	0	1000	Accept
New Approach - As Is	**SL08040A_4**	1000	0	1000	-0.3	1000	-0.1	1000	Accept
New Approach - 3X260C	**SL08040A_9**	1000	0	1000	0.3	1000	0	1000	Accept
New Approach - 3X260C	**SL08040A_3**	1000	0.1	1000	-1.1	1000	0	1000	Accept
New Approach - 3X260C	**SL08040A_1**	1000	0	1000	-1.3	1000	-0.1	1000	Accept
New Approach - 6X260C	**SL08040A_7**	1000	0.9	1000	2.2	1000	0.7	1000	Accept
New Approach - 6X260C	**SL08040A_2**	1000	1.1	1000	-0.4	1000	1	1000	Accept
New Approach - 6X260C	**SL08040A_8**	1000	0.5	1000	0	1000	0.4	1000	Accept
New Approach - As Is	**SL08041A_3**	1000	0.2	1000	0.6	1000	0.2	1000	Accept
New Approach - As Is	**SL08041A_8**	1000	0.2	1000	1.2	1000	0.1	1000	Accept
New Approach - As Is	**SL08041A_9**	1000	0.2	1000	0.2	1000	0.2	1000	Accept
New Approach - 3X260C	**SL08041A_1**	1000	0.6	1000	0.3	1000	1.2	1000	Accept
New Approach - 3X260C	**SL08041A_2**	1000	0.3	1000	-1.1	1000	1.9	1000	Accept
New Approach - 3X260C	**SL08041A_5**	1000	0.6	1000	-0.5	1000	0.5	1000	Accept
New Approach - 6X260C	**SL08041A_4**	464	10	464	1.1	463	2.3	464	Post
New Approach - 6X260C	**SL08041A_6**	1000	0.5	1000	-0.6	1000	0.4	1000	Accept
New Approach - 6X260C	**SL08041A_7**	1000	0.2	1000	-0.7	1000	0.2	1000	Accept
Summary	**Mean**	970	1	970	0	970	1	970	Accept
	Std Dev	126.3	2.3	126.3	0.9	126.6	0.7	126.3	Accept
	Min	464	0	464	-1.3	463	-0.1	464	Accept
	Max	1000	10	1000	2.2	1000	2.3	1000	Accept

Coupon SL08040A, S1 = L1-L8 PTH with Conductive and S2 = L1-L7 with Non-Conductive Via Fill

Coupon SL08041A, S1 = L1-L8 PTH with Conductive and S2 = L1-L6 with Non-Conductive Via Fill

New Copper Wrap Plate Technology - Benefits

- Consistent wrap plate thickness matching the thickness of the initial surface copper. Minimum wrap and copper thickness in accordance with IPC 6012B Class 2 or Class 3
- Non-Destructive surface copper thickness measurements to verify copper wrap thickness.
- Increased reliability due to verifiable wrap uniformity over the entire panel
- Eliminates copper thickness build-up during multiple wrap plate cycles on a common layer
- Consistent impedance values on the plated layers with filled holes due to improved surface plating distribution
- Improved dielectric thickness on all sub-laminations between the sub-outer plated layer and the subsequent laminated layer.
- Reduced surface copper thickness helps to manufacture designs with fine lines and tighter geometries
- Improved soldermask thickness uniformity due to reduced copper feature height