The Effect of Functional Pads and Pitch on Via Reliability using Thermal Cycling and Interconnect Stress Testing

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Abstract
European legislation has meant that lead-free solders now dominate mainstream electronics manufacturing. These replacement solders are all high tin alloys with significantly higher melting points compared to conventional tin-lead materials. Substrate technology has been developed around reinforced resin materials and concerns have been raised regarding the increased degradation caused by the associated higher processing temperatures. This is compounded by the interconnecting structures being brought into closer proximity as a result of increasing technology advances driven by miniaturisation. The removal of non-functional pads to facilitate signal routing and improved drilling conditions for high aspect ratio vias, may also affect substrate reliability.

The National Physical Laboratory and PWB Interconnect Solutions Inc. have undertaken a joint study following identical test structures through both thermal cycling, with constant electrical monitoring (event detecting) and Interconnect Stress Testing (IST). The test vehicles included patterns to monitor changes in interconnection spacing (pitch) and also the effect of removing non-functional pads. The failure modes generated with both techniques were similar as were the relative rankings of the effects. The results showed that the removal of non-functional pads tended to improve reliability for high aspect ratio plated through holes in thicker substrates, although increasing interconnection pitch had little effect on failure rate.

The results generated by both thermal cycling and IST showed extremely good correlation. Failures occurred at a slightly lower number of cycles for IST compared to thermal cycling due to the unique ability of a more stringent failure criterion possible with IST. The relative ranking of the level of failures is identical for both the thermal cycling and IST but the results were obtained in very different timescales. IST has been shown to give a fast comparable result to thermal cycle testing with constant monitoring, but thermal cycling may be more beneficial if a wider range of experimental parameters (E.g. Solder joints) are to be tested simultaneously.

Introduction
The requirement to comply with the European regulations in 2006 banning lead, has driven the adoption of new materials both in PCB assembly and bareboard manufacture. The electronics manufacturing industry has been using SnPb based solders for electrical and electronic interconnection for more than 60 years and the European ban on lead effectively discards all that experience and research into the reliability of soldered assemblies. Many organisations including NPL and PWB, are working hard to improve the knowledge and experience of lead-free reliability but many questions are still unanswered.

The alloy traditionally used for soldering in electronics manufacturing was SnPb, which has a melting point of approximately 183^{o}C. The replacement solders for SnPb are all high tin alloys with significantly higher melting points than conventional tin-lead materials; the preferred choice is now a tin/silver/copper alloy, which has a higher melting point of approximately 217^{o}C. Several workers have reported concerns that the increased processing temperatures associated with these new alloys, may affect the reliability of the printed circuit substrate. As soldering temperatures are increased, the substrate will expand more in the z-axis, which increases the corresponding strain on the copper barrel of the vias and potentially increased the risk of material damage.

Substrate technology, generally epoxy or phenolic-cured based materials have been developed; degradation at the higher process temperatures required by the new alloys is an issue. Reliability of plated through holes and μ-vias can be degraded, propensity for multi-layer substrates to delaminate may be increased and electrical insulation properties may be disrupted, due to increased risk of dielectric breakdown by cathodic or anodic electro-migration.

All this is compounded by the interconnect structures being brought into closer proximity as a result of increasing technology advances driven by miniaturisation. The decision to remove non-functional pads to facilitate signal routing,

by reducing the capacitance, increasing the impedance of a via and efforts to improve drilling conditions of fine vias, may also affect substrate reliability at lead-free soldering temperatures. The effect on reliability of removing non-functional pads has been as area of contention within the electronics industry for some time.

The work reported here forms part of a joint industry/UK government funded project to develop test methods for advanced electrical interconnect. An inter-comparison of Interconnect Stress Testing (IST) and thermal cycling of test substrates has been undertaken, using a test vehicle to explore the effects of removing non-functional pads and reducing the spacing between vias.

Methodology

Test Vehicle

A test panel was designed that included eight coupons of via chains and is shown in Figure 1. The board was a 2.5mm thick, 10 layer structure using a high Tg, phenolic-cured glass reinforced epoxy laminate with an immersion Ag surface finish. The overall size was 230mm x 180mm.

A single test coupon (G) was designed for thermal cycling; incorporating chains of 10:1 aspect ratio vias, on two different via grid pitches (1.0mm and 0.8mm). Some patterns included non-functional pads and another had the pads removed. There was also a test pattern for µ-vias. For IST testing, the test patterns of the thermal cycling board were duplicated on the same panel as individual test coupons with the addition of a different grid sizes for µ-vias (coupons A, C to F).

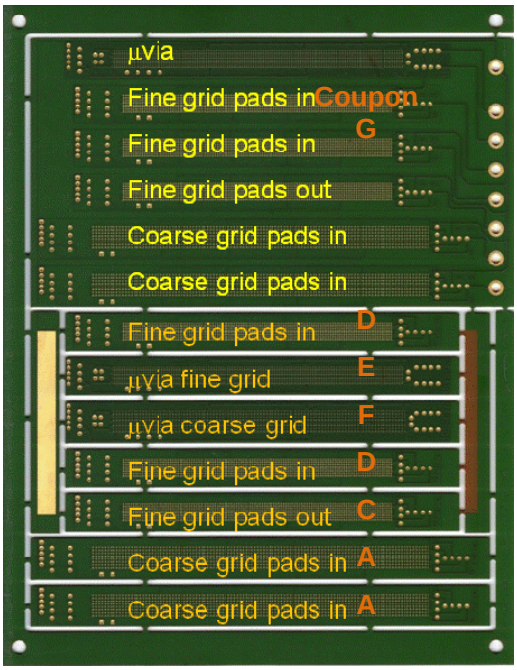

Figure 1: Test board showing individual test patterns for, at the top, thermal cycling (Coupon G), and lower down the individual IST test patterns (Coupons A, C through F)

Conditioning of Test Boards

To determine the worst case effects of lead-free reflow soldering on the reliability of the PCBs, test boards were reflowed in a 7-zone reflow oven with a peak reflow temperature of 260°C, achieving a molten solder time of approximately 70 seconds. The PCBs were reflowed 6 times, with the boards allowed to cool for 15 minutes before being re-profiled.

Thermal Cycling and Electrical Test

Thermal cycling was undertaken on coupon G. These chains of through vias and µ-vias on this coupon were connected to event detectors so that the resistance of the chains could be constantly monitored.
These registered a failure when the chain resistance increased to > 5kΩ for a period greater than 200ns. Thermal cycling was conducted in a single chamber system up to 3000 cycles, -55°C to 125°C with 5min dwells, ramps of 10°C per minute, giving a total cycle time of ~ 1 hour.

Interconnect Stress Testing

The IST was undertaken at PWB Interconnect Solutions Inc. and followed IPC TM650 standard methodology (Reference 3). This testing utilised coupon A, C and D of the test panel, with each test vehicle consisting of two independent test

circuits. The first, or "sense" circuit, was constructed to measure the reliability of plated through holes (PTH) barrel. The second, or "power" circuit, consists of internal interconnections between the copper foils and the upper/lower layers of the PTH barrels. The power circuit is also used to homogenously heat the coupon, by passing DC current through specifically designed circuits in the outer layers, which match the heating conditions created during component assembly and product operation. Throughout IST testing both circuits are continually monitored until a preset level of electrical degradation (structural damage) is achieved, at which point the temperature cycling for each individual coupon is suspended. For this study, IST testing was performed by heating coupons from ambient to 150°C in three minutes + 0/- 5 seconds followed by cooling to ambient. Testing continues until a circuit demonstrated a 10% increase in resistance or end of test at 2000 cycles (8 days).

Results

Effect of removing non-functional pads

The failures that were generated during thermal cycling for samples where non-functional pads were included or omitted are shown in Figure 2, as a Weibull plot. The plot shows similar gradients for both sample sets but where non-functional pads have been removed; the time to failure is greater than that for samples with the non-functional pads included. The number of cycles to 50% failures is around 700 cycles when the non-functional pads included, compared to around 930 cycles when the non-functional pads are removed.

The failures that were generated for similar samples during IST testing are shown in Figure 3 as a Weibull plot. These results mirror the thermal cycling results with the plot showing similar gradients for both sample sets, where non-functional pads have been removed, the time to failure is greater than that for samples with the non-functional pads included. The number of cycles to 50% failures is at around 550 cycles for non-functional pads included against around 700 cycles when the non-functional pads are removed.

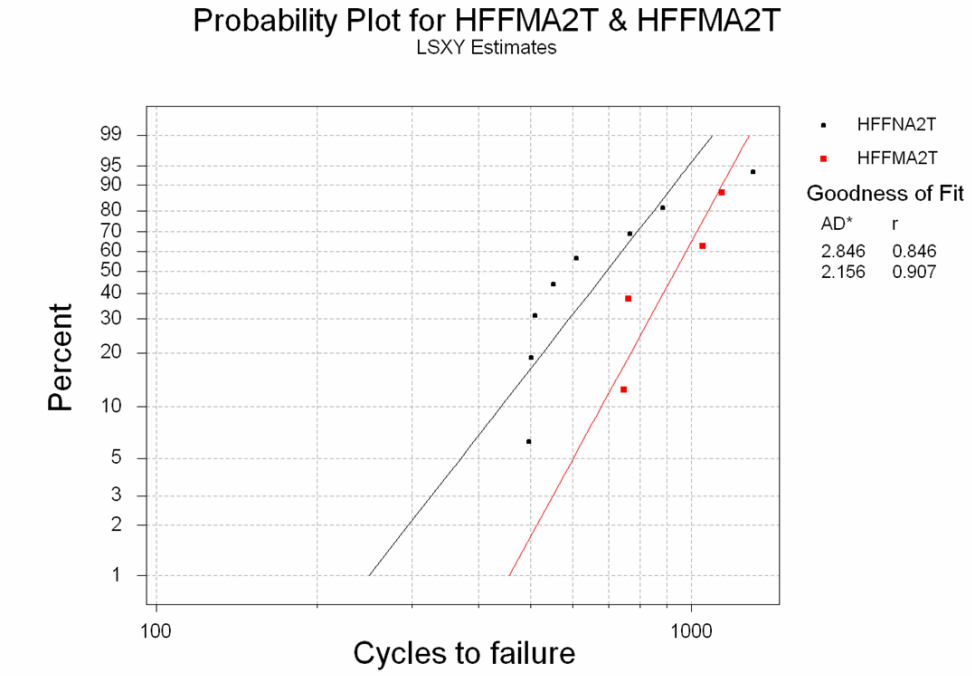

Figure 2: Weibull plot of thermal cycle failures for HFFNA2T (non-function pads included) and HFFMA2T (non-functional pads removed)

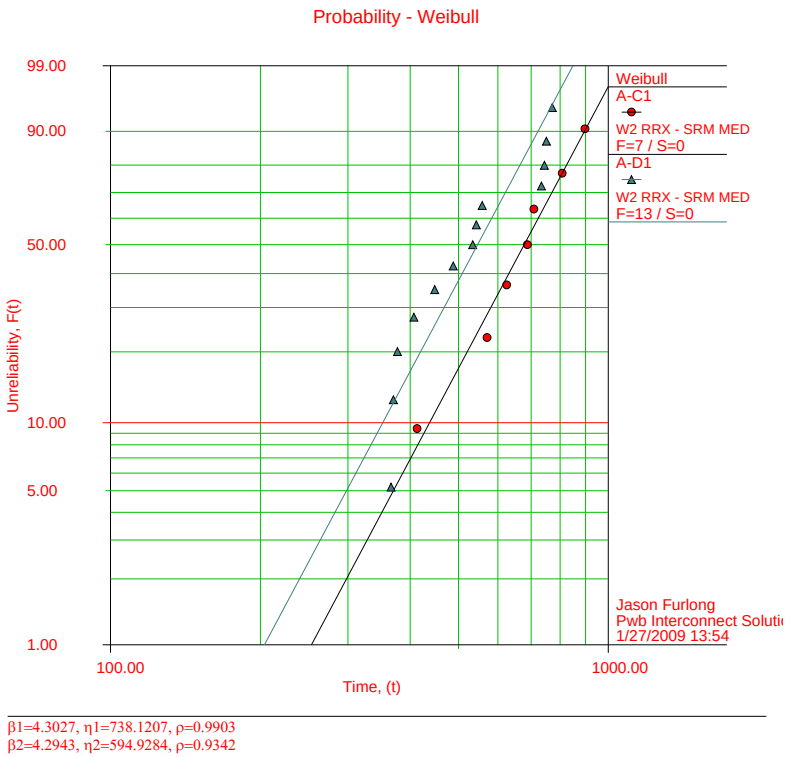

Figure 3: Weibull plot of IST failures for coupon D (non-function pads included) and coupon C (non-functional pads removed)

Effect of via proximity

The failures that were generated during thermal cycling for samples with via grid pitches of 1.0mm and 0.8mm pitches are shown in

Figure 4 as a Weibull plot. The plot shows the similar gradients for both sample sets, with little difference between the relative reliabilities of both sample sets. The number of cycles to 50% failures is similar at around 700 cycles**.**

The failures that were generated during IST testing for samples with via grid pitches of 1.0mm and 0.8mm pitches are shown in Figure 5 as a Weibull plot. The plot shows the similar gradients for both sample sets and little difference between the relative reliabilities of both sample sets. The number of cycles to 50% failures is similar at around 550 cycles.

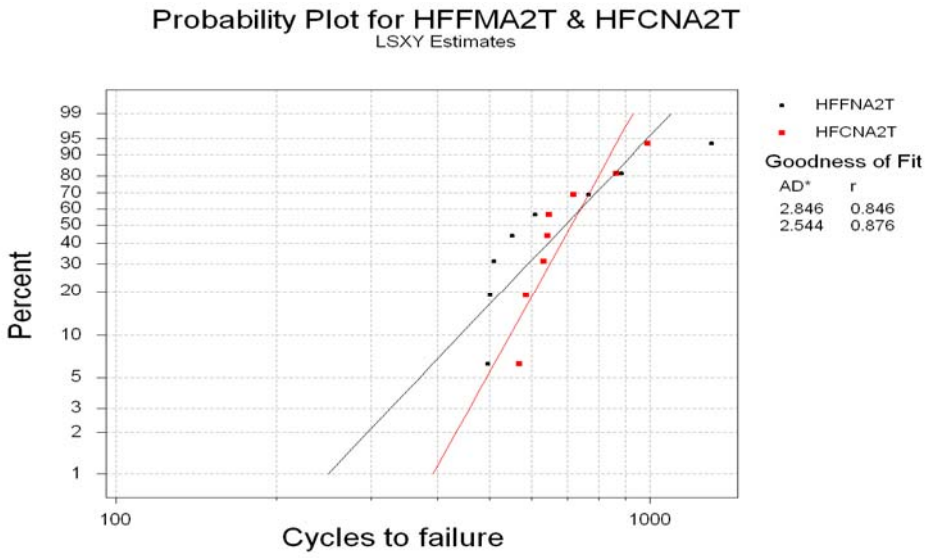

Figure 4: Weibull plot of thermal cycle failures for HFFNA2T (fine pitch grid) and HFCNA2T (coarse pitch grid)

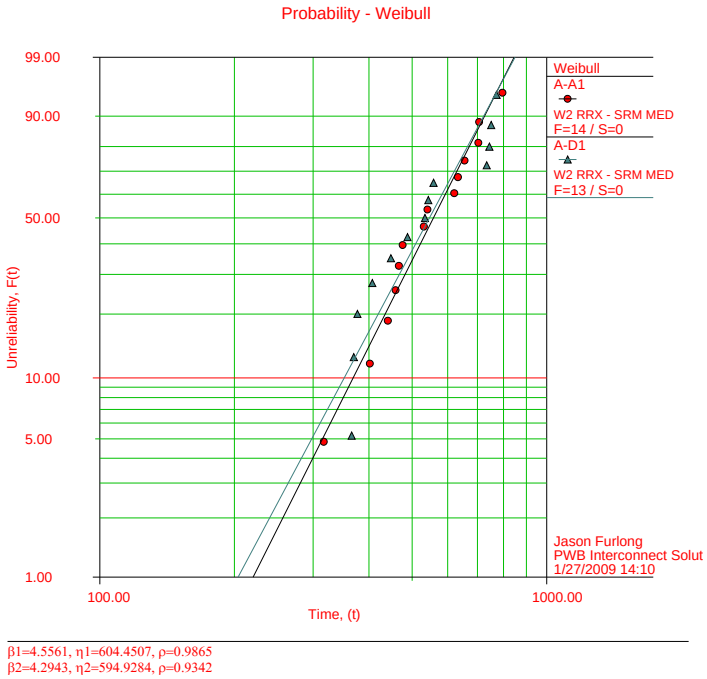

Figure 5: Weibull plot of IST failures for coupon D (fine pitch grid) and coupon A (coarse pitch)

Discussion

Comparison of the results for the functional pads evaluation shows similar results for both thermal cycling and IST. For both techniques, the inclusion of non-functional pads caused early failures of the 10:1 aspect ratio vias, after conditioning for six lead-free reflow profiles, giving approximately a 20% reduction in fatigue life. A comparison for the number of cycles to 50% failures is given in Figure 6. This difference, although significant, should be considered second order alongside such issues as PCB manufacturing quality (copper plating quality & thickness) and materials characteristics (Tg, z-axis CTE).

Reviewing micro-sections of failed vias indicates a high percentage of vias with non-functional pads included, have failed adjacent to the non-functional pads as shown in Figure 7 even though these are away from the central portion of the via, where failures would generally be expected to occur. These correlates well with other evaluations that have been undertaken by PWB (reference 4) and Kim et al (reference 5). It has been postulated that the inclusion of non-functional pads acted as stress concentrators, leading to the earlier failure.

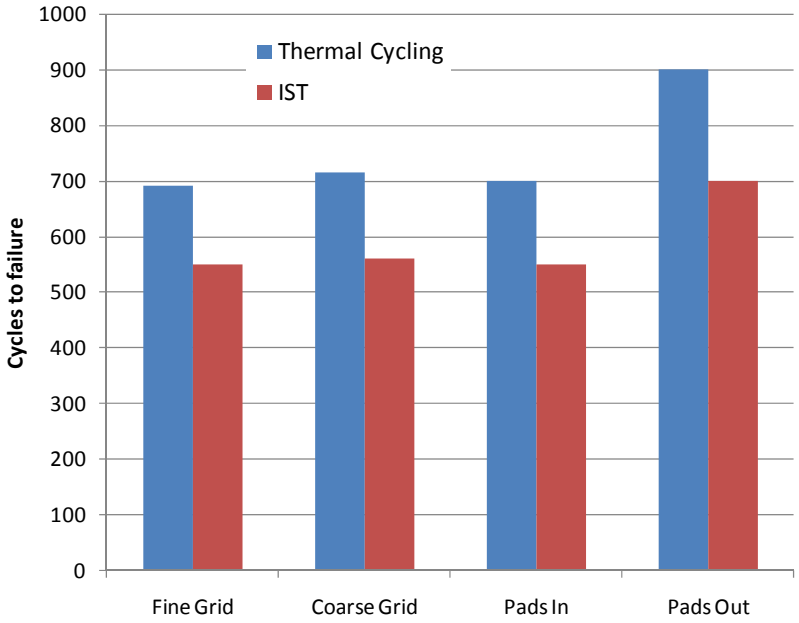

Figure 6: Comparison of number of cycles to 50% failures for thermal cycling and IST

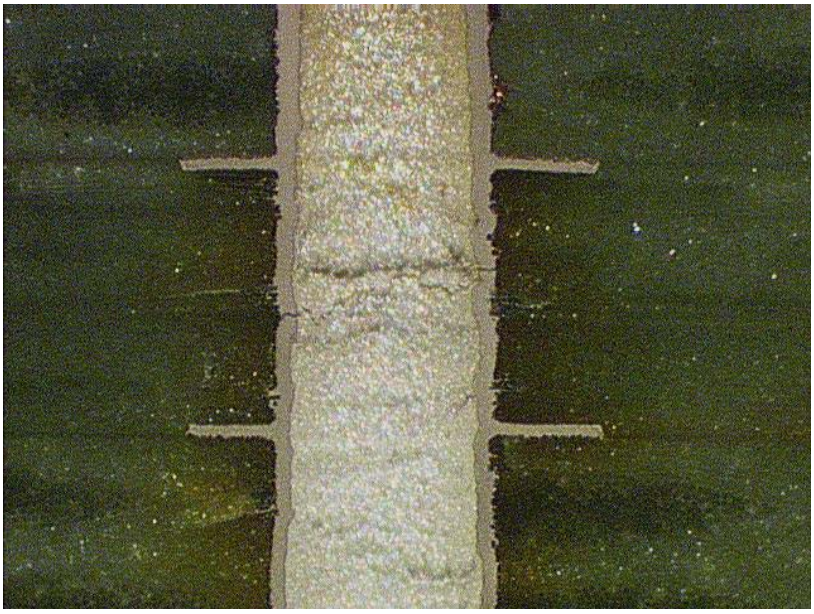

Figure 7: Micro section of via with failure in region where non-functional pads have been retained.

The results comparing the effect of reducing the via grid size from 1.0 mm to 0.8 mm showed little effect for both thermal cycling and IST. The Weibull plot for the thermal cycle results (

Figure 4) shows similar failure rates for both grid sizes. The number of cycles to 50% failures as shown in Figure 6 is also similar. Analysis of microsections of failed vias from each data set also indicated similar failure modes and locations. Typical failures are shown in Figure 8 for a coarse pitch via and Figure 9 for a fine pitch via. The results for the IST are similar with no differentiation between the data sets.

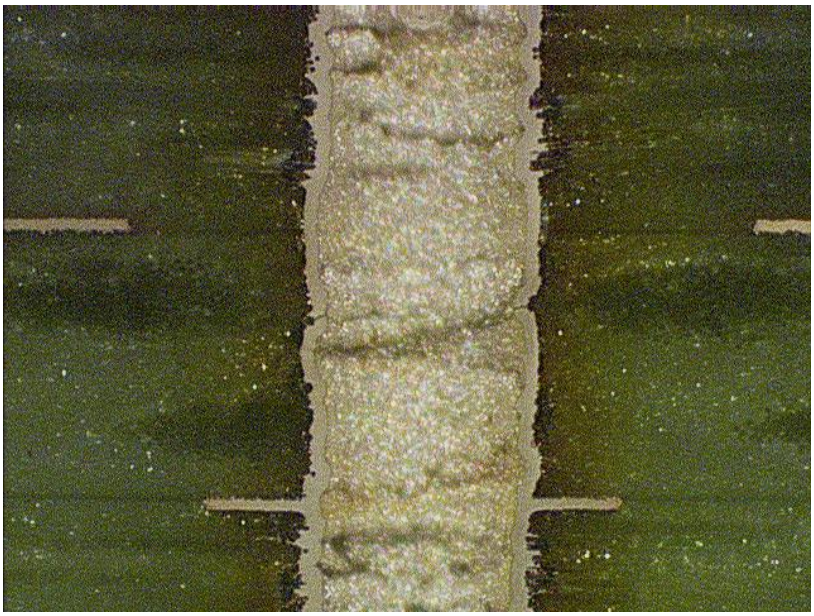

Figure 8: Microsection of failure for via on coarse (1.0mm) pitch

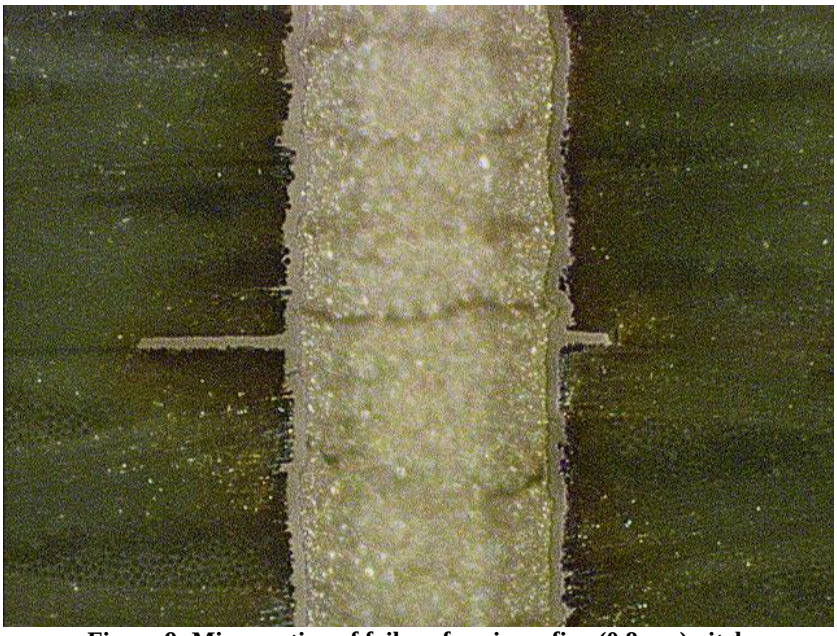

Figure 9: Microsection of failure for via on fine (0.8mm) pitch

The results generated by both thermal cycling and IST showed extremely good correlation. A comparison for the number of cycles to 50% failures is given in Figure 6 for the both sets of results. In all cases, failures occurred slightly earlier for IST than for thermal cycling. This is explained by the 25°C higher test temperature and the difference in failure criteria for each test method. For thermal cycling, a via chain is considered to have failed when the resistance increases to greater than 5kΩ □(approximately 1600%)□for a period greater than 200 ns. For IST, measuring a 10% increase in resistance of the via chain is considered a failure. Allowing for these differences, both techniques gave similar results with 50% failures occurring in the 500 to 900 cycles range. The relative ranking of the level of failures is identical for both the thermal cycling and IST. It should be noted that these results were obtained in very different timescales. For the thermal cycling, 1000 cycles takes about 40 days of testing although multiple circuits can be tested simultaneously. The test setup used here was capable of monitoring 480 circuits continuously during those 40 days. IST testing was undertaken in a much shorter time frame with 1000 cycles taking approximately 4 days to complete. However, during this period, each IST tester can only monitor 12 test circuits. Therefore, IST gives fast comparable results, but thermal cycling may be more beneficial if a wide range of experimental parameters are being tested simultaneously.

Conclusions

The National Physical Laboratory and PWB Interconnect Solutions Inc. successfully completed a joint reliability study following identical test structures through thermal cycling with constant electrical monitoring (event detecting) and IST Technology. The coupons included test patterns to monitor changes in interconnection pitch and also the effect of the removal of non-functional pads. The failure modes generated with both techniques were similar as were the relative rankings of the effects. The results showed that the removal of non-functional pads improved reliability by 20% for high aspect ratio plated through holes in thicker substrates. However this effect should be considered second order alongside such issues as PCB manufacturing quality (copper plating quality or thickness) and materials characteristics (Tg, z-axis CTE). Decreasing interconnection pitch from 1.0 mm to 0.8 mm had little effect on failure rate.

The results generated by both thermal cycling and IST showed extremely good correlation. Failures occurred slightly earlier for IST than for thermal cycling. This is explained by the 25°C higher test temperature and the more stringent failure criteria applied for IST test method. Allowing for these differences, both techniques gave similar results with 50% failures occurring in the 500 to 900 cycles range. The relative ranking of the level of failures is identical for both the thermal cycling and IST but the results were obtained in very different timescales. In this specific study results were achieved in 2 to 3 days with IST versus 20 to 40 days with the thermal oven. IST has been shown to give fast comparable results to thermal cycle testing with constant monitoring, but thermal cycling may be more beneficial if a wide range of experimental parameters is to be tested simultaneously.

References

1. Reliability evaluation of plated-through holes for high density PWB application; Donghyun Kim, Mudasir Ahmad, David Senk, Mason Hu, SMTA International Sept 2006
2. Via Optimization for Speed; Cuong Nguyen: SMT December 2008
3. IPC-Test Manual TM 650, Number 2.6.26
4. Discussion on non functional pad removal / backdrilling and PCB reliability: Bill Birch, PWB Corp.;
5. Reliability evaluation of plated through holes for high density PCBs; Donghyun Kim, Mudasir Ahmad, David Senk, Mason Hu; SMTA International 2006

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A Comparison of Via Reliability after Lead-Free Soldering using Thermal Cycling and Interconnection Stress Testing

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Background

- European legislation has meant that lead-free solders now dominate mainstream electronics manufacture.
- These replacement solders are all high tin alloys with significantly higher melting points than conventional tin-lead materials.
- Substrate technology has been developed around reinforced resin materials and degradation at the higher process temperatures required by the new alloys is an issue.
- This is compounded by the conducting features being brought into closer proximity as a result of increasing technology advances driven by miniaturisation.
- The removal of non-functional pads to facilitate signal routing and improve drilling of high aspect ratio vias, may also affect substrate reliability.

NPL Pb-contamination Studio

- Failures of vias in NPL project evaluating Pb contamination of LF
  - 5 assemblies per batch, 400μ via in 1.6mm FR4

Reflow Solder	Wave Solder	No.of via failures at 2000 thermal cycles
SAC	SAC	7/310
SAC	None	4/310
SnPb	SnPb	1/310
SnPb	SnPb	2/310

Objectives

- Evaluation of the effect of via proximity on reliability of LF PCBs
- Evaluation of relative performance of via including and excluding non-functional pads
- Evaluation of the relative performance of interconnection stress testing (IST) and thermal cycle testing

Test Board Design

- For thermal cycling, similar to phase 1 but restricted to 10:1 vias, with 2 via grid sizes (1.0 and 0.8mm) including non-functional pads and with non-functional pads removed. Also test patterns for vias.
- For IST testing, duplicate of thermal cycling board but with 2 μ-via grid sizes

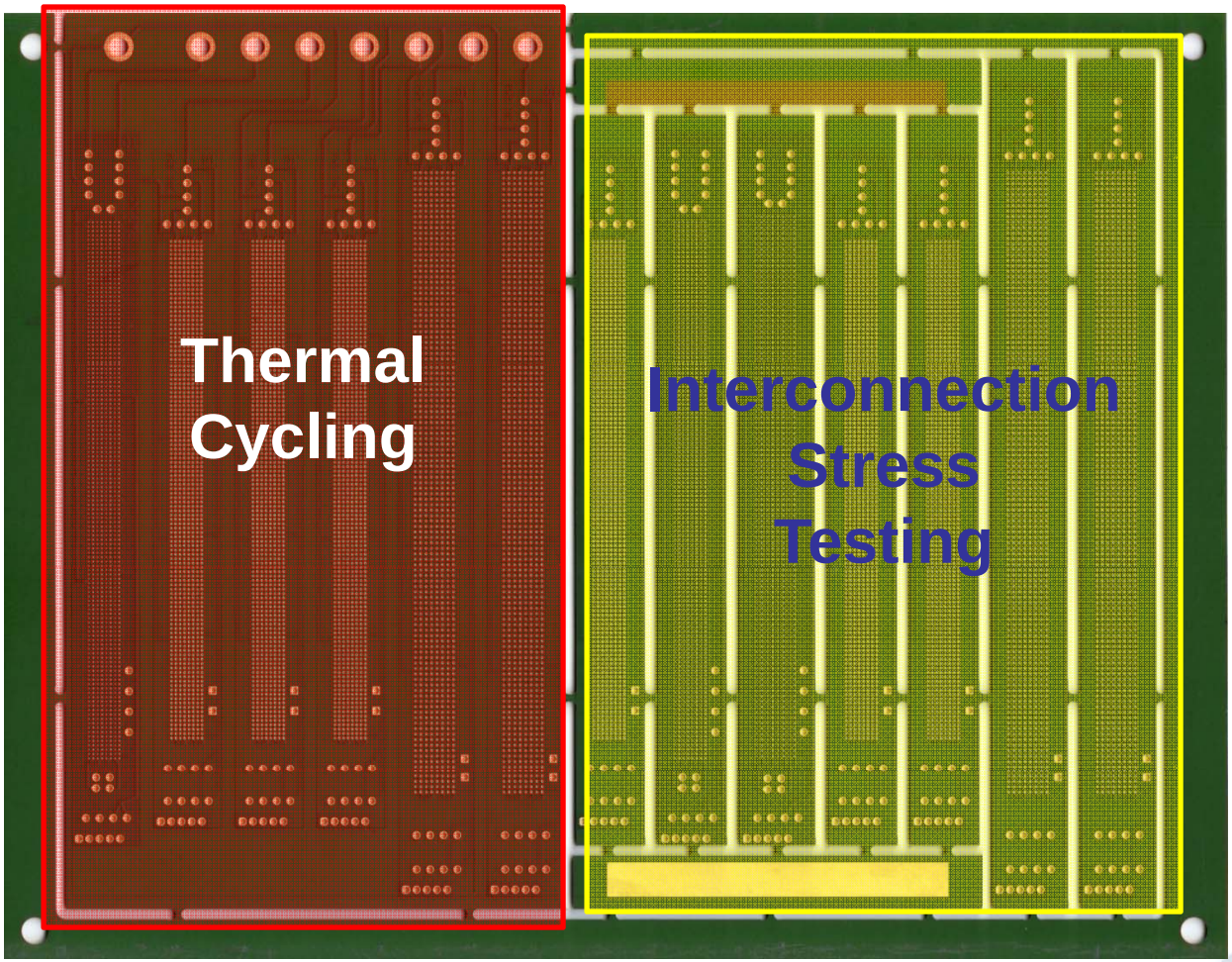
Each set consists 5 PCBs as follows:

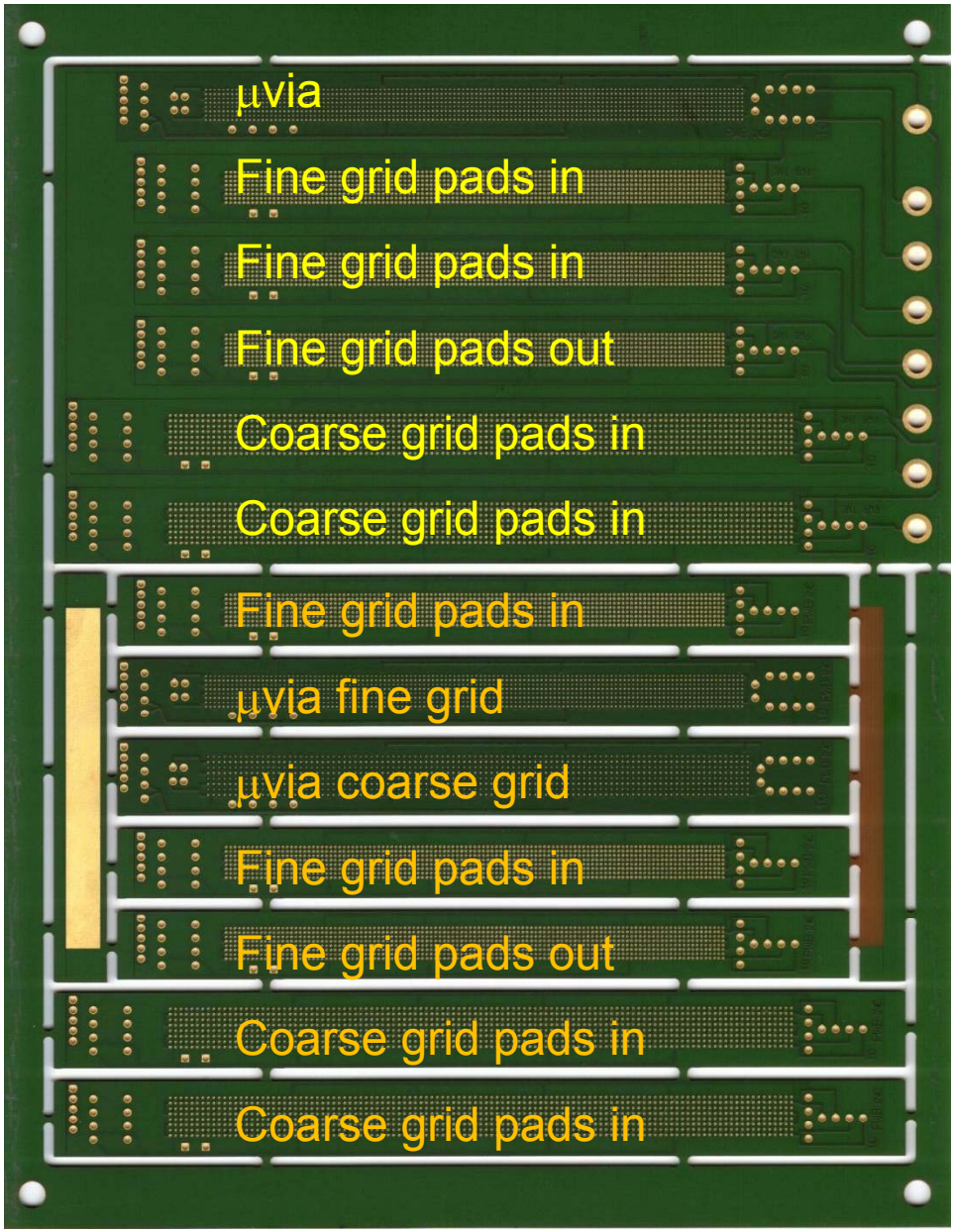
- Thermal cycling
  - 2 x 10:1 grid 1.0mm (non-functional pads in)
  - 2 x 10:1 grid 0.8mm (non-functional pads in)
  - 1 x 10:1 grid 0.8mm (non-functional pads out)
  - 1 x μ-via
- IST -
  - 2 x 10:1 grid 1.0mm (non-functional pads in)
  - 2 x 10:1 grid 0.8mm (non-functional pads in)
  - 1 x 10:1 grid 0.8mm (non-functional pads out)
  - 1 x μ-via grid 1.0mm
  - 1 x μ-via grid 0.8mm
- Materials testing area

Lay-up 2.5mm PCB

Layers	Qty	Type	Reference
1 / 0	1	Foil	12µM CAC
0 / 0	2	FR4 prepreg	FPP/1080
2 / 3	1	FR4	FR4/014/HH
0 / 0	2	FR4 prepreg	FPP/1080
4 / 5	1	FR4	FR4/014/HH
0 / 0	2	FR4 prepreg	FPP/2116
6 / 7	1	FR4	FR4/014/HH
0 / 0	2	FR4 prepreg	FPP/1080
8 / 9	1	FR4	FR4/014/HH
0 / 0	2	FR4 prepreg	FPP/1080
0 / 10	1	Foil	12µM CAC

Test Substrate – T/C & IST




μvia
Fine grid pads in
Fine grid pads in
Fine grid pads out
Coarse grid pads in
Coarse grid pads in
Fine grid pads in
μvia fine grid
μvia coarse grid
Fine grid pads in
Fine grid pads out
Coarse grid pads in
Coarse grid pads in

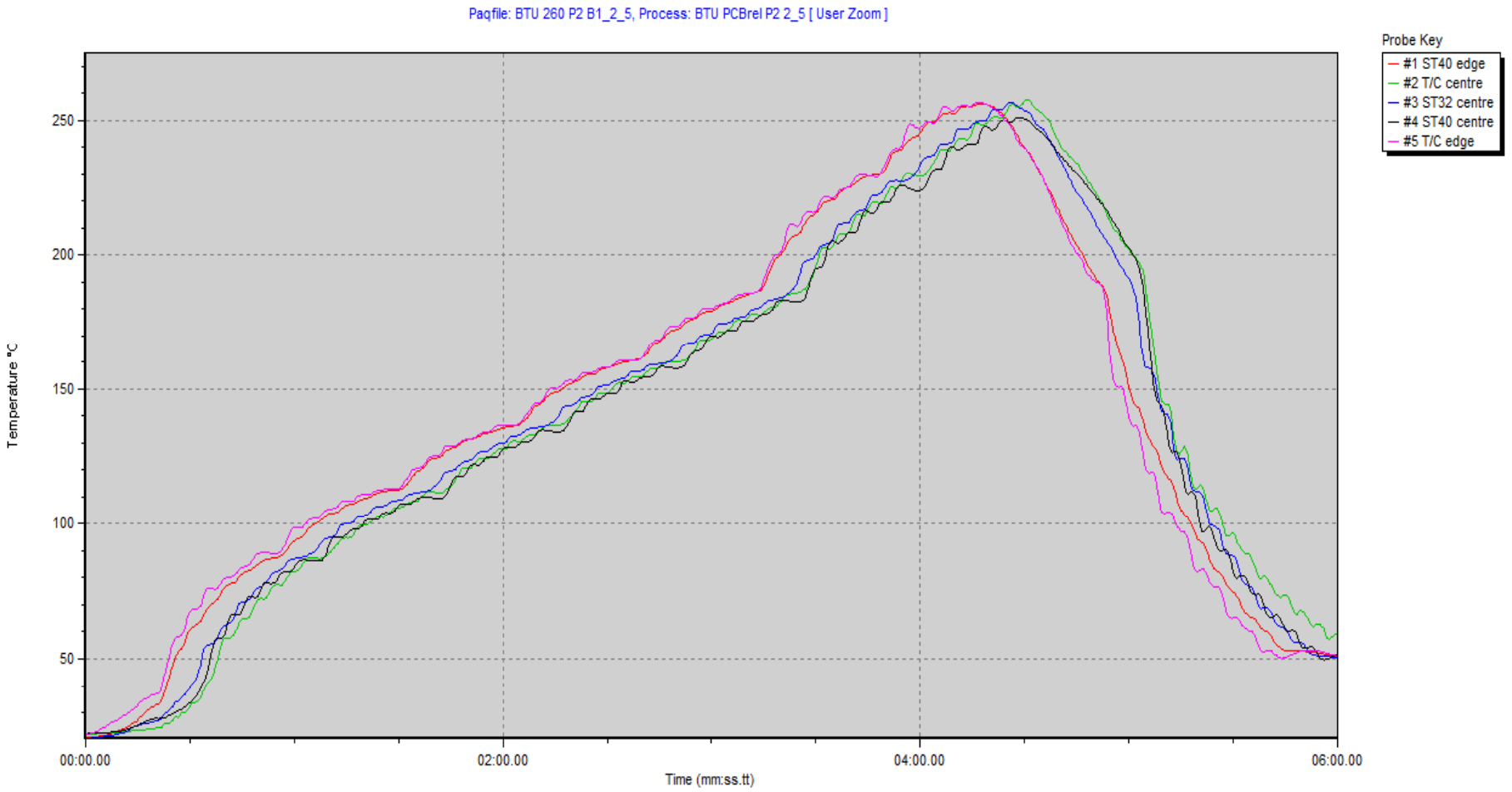
Reflow Conditioning

THE GLOBAL LEADER IN THERMAL TECHNOLOGY

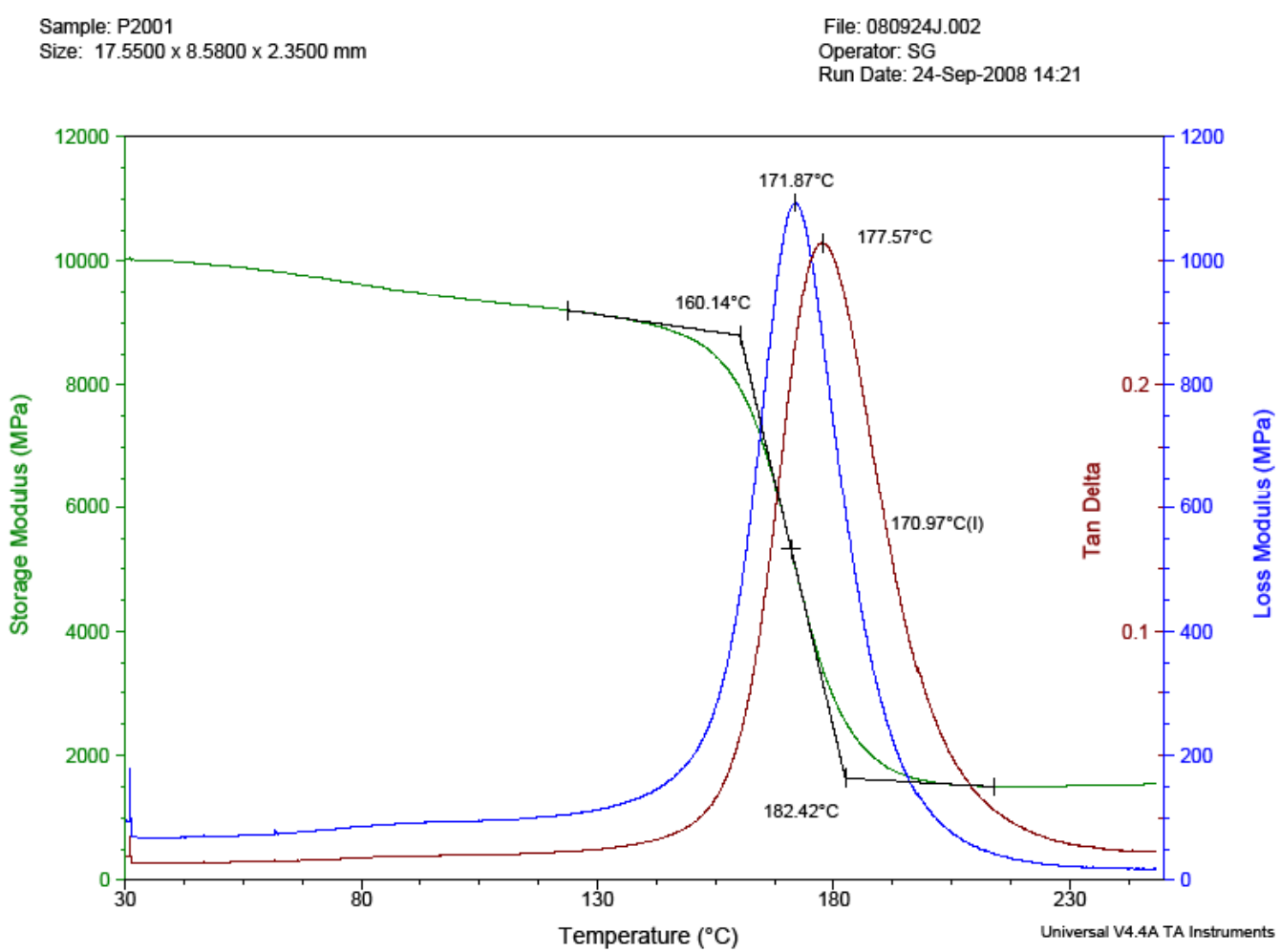
- Undertaken courtesy of BTU using 7 zone Pyramax 98
- Profiled using Datapaq
- Separate profiles set up for each board thickness
- Peak reflow 260 °C
- Boards allowed to cool to RT between reflows

DATAPAQ

Reflow Profiling – 2.5mm

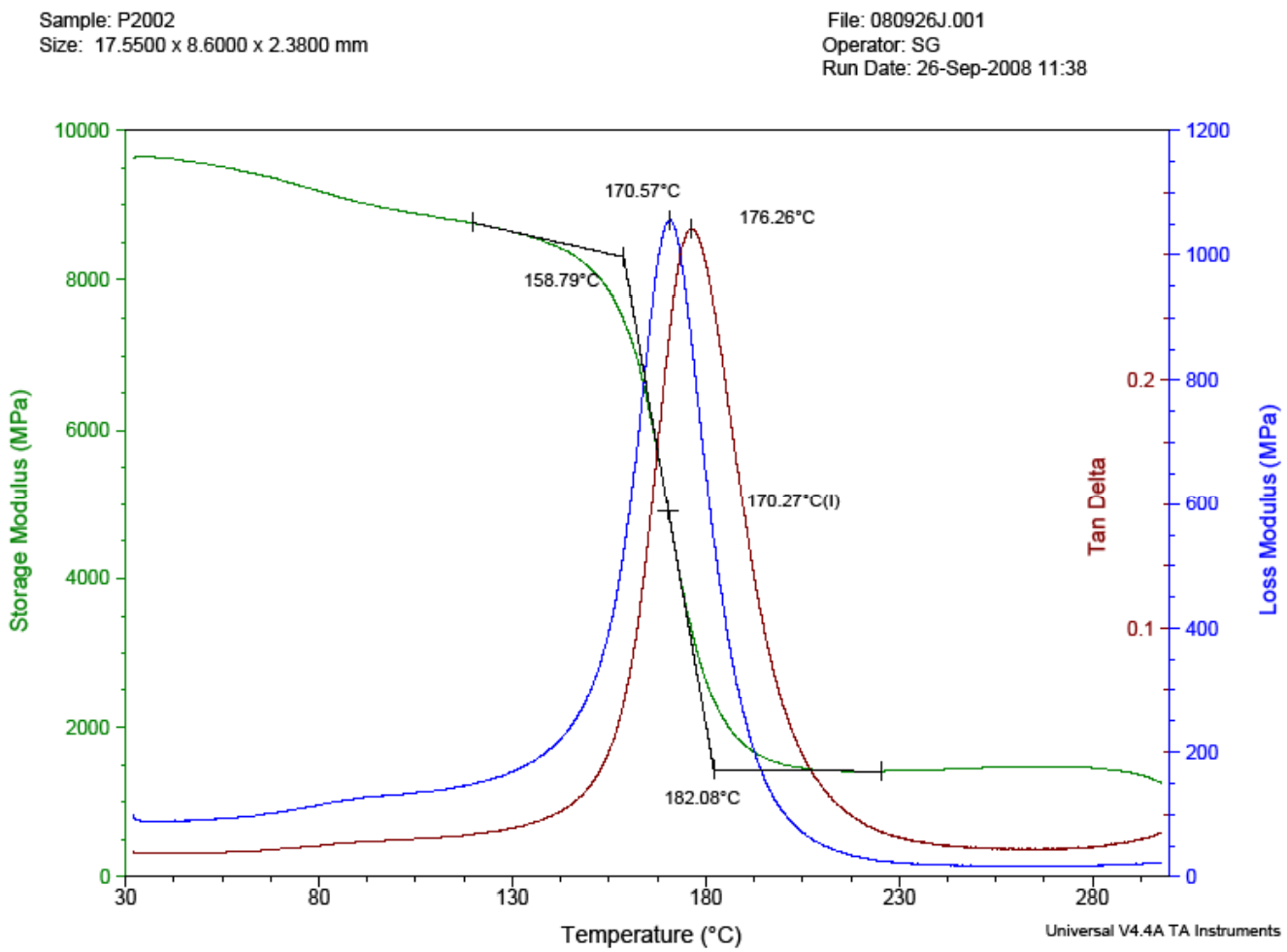


DMA – Unconditioned HP



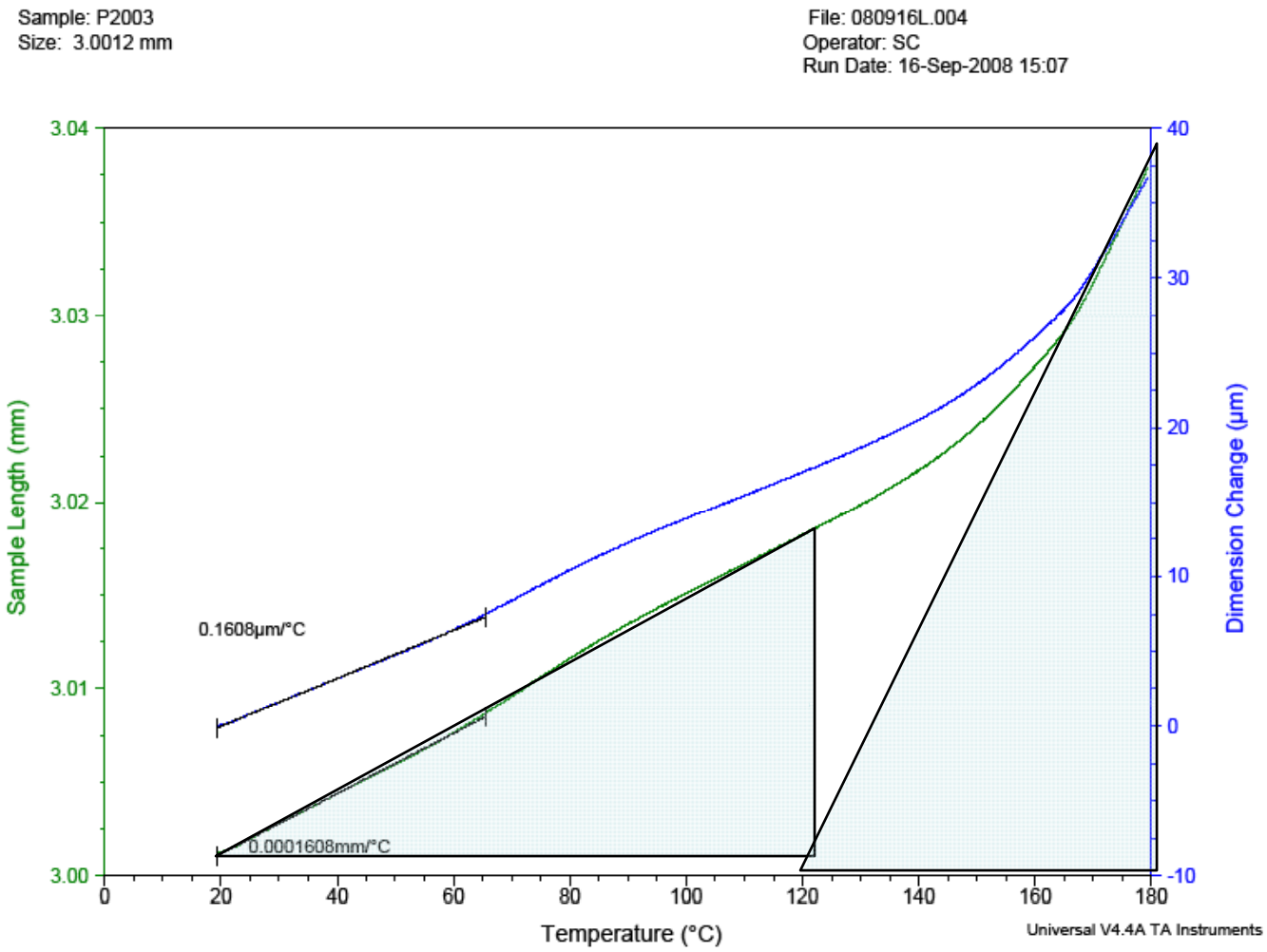
- As received
- 2.5mm thick
- Tg ~171°C

DMA – Conditioned HP



- 6 reflow profiles
- 2.5mm thick
- Tg ~170°C

TMA – Conditioned HP



- 6 reflow profiles
- 3.2mm thick
- Z-axis CTE below Tg
- $70 \times 10^{-6}/^{o}C$
- Above Tg
- $270 \times 10^{-6}/^{o}C$

Thermal Cycling

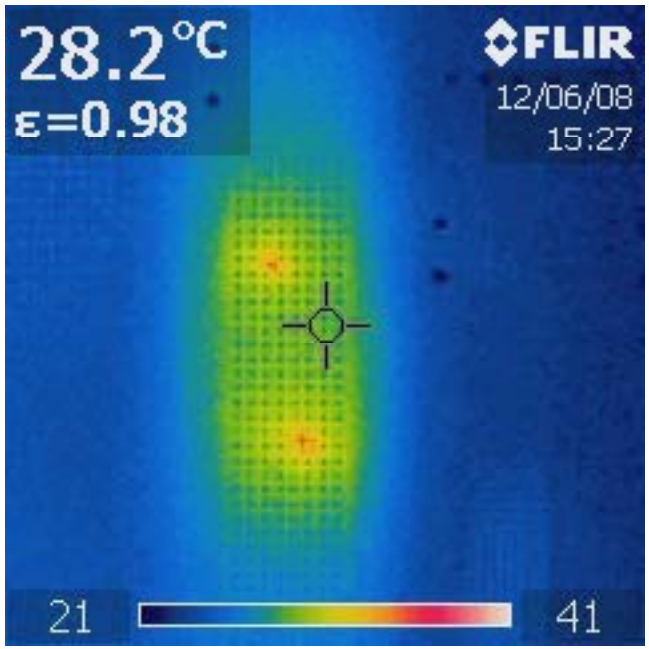
- 3000 cycles on all substrates
  - -55 to 125°C, 5 min dwells
- All substrates constantly monitored
  - Hard-wired to event detector
  - Failure increase of chain resistance to > 5KΩ

IST Testing

- Coupon heated from ambient to 150C in 3 mins, cooled down in 2 mins (1 day = 300 cycles)
- Continuous resistance monitoring throughout entire test
- System sensitivity 1 milliohm
- 10% rejection criteria = 100 milliohms
- Stressing stopped at point of failure

Failed Via Location

- Electrical test
- Thermal test for intermittents

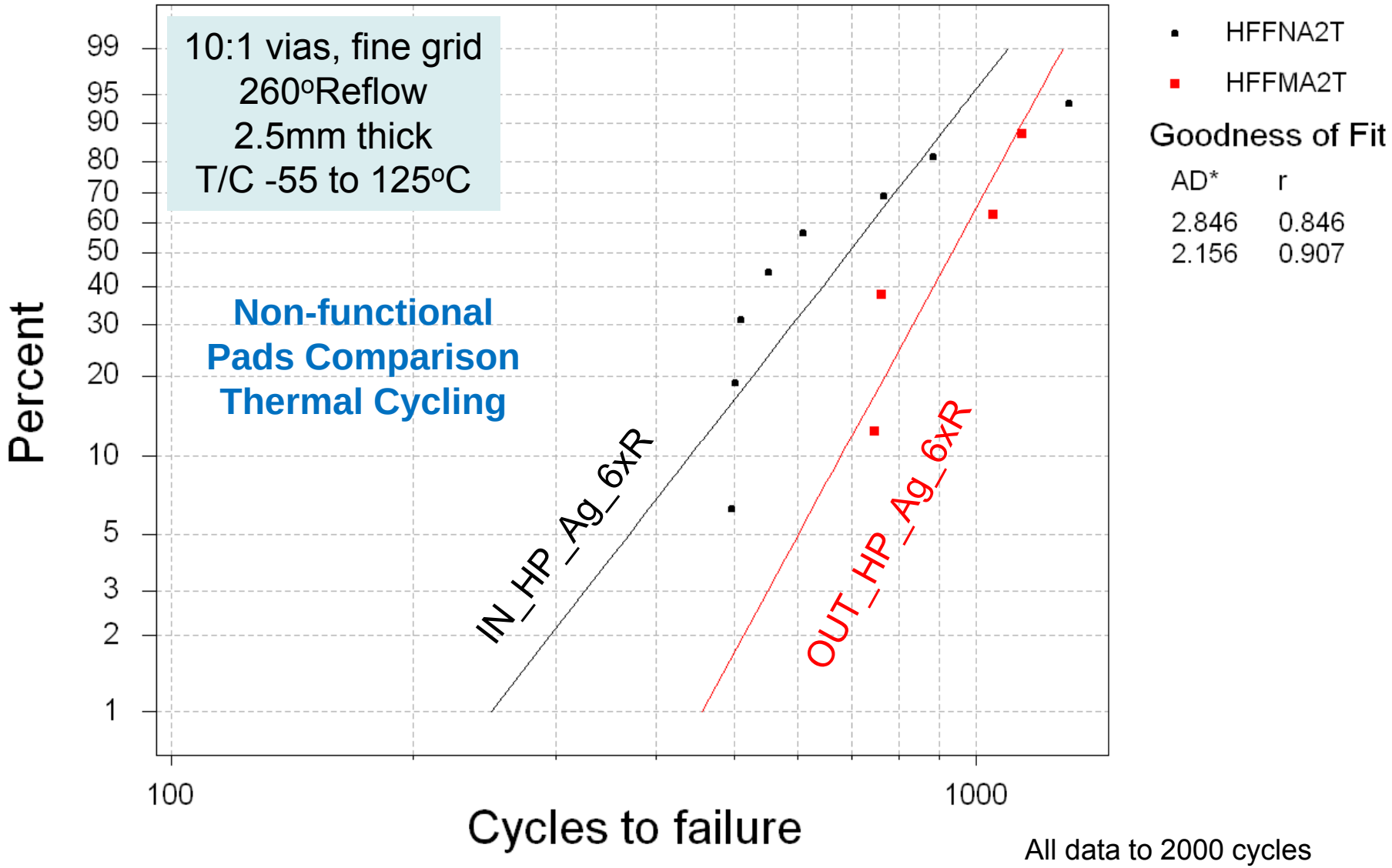


Comparison of Via Reliability

Inclusion/exclusion of non-functional pads

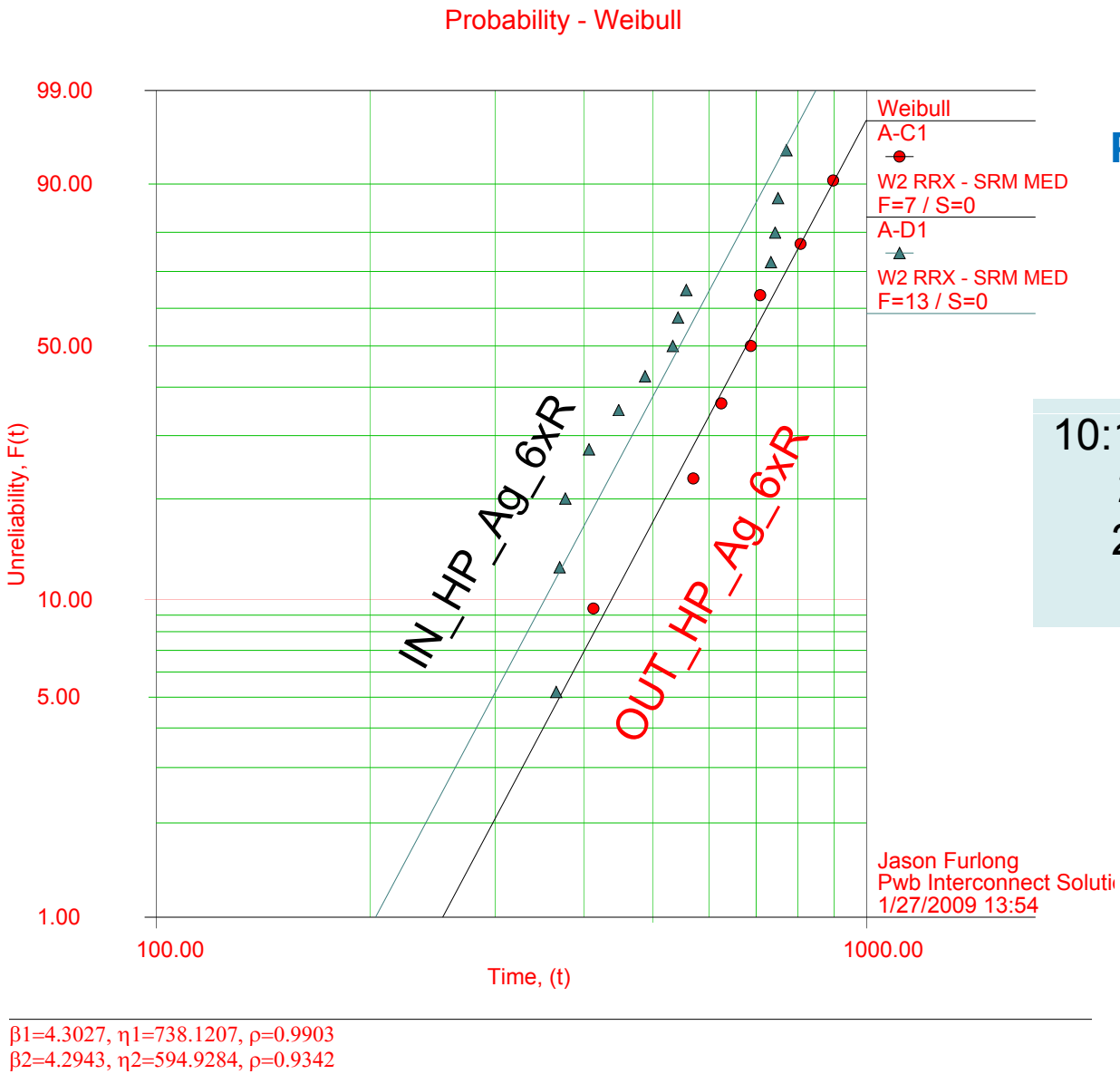
Probability Plot for HFFMA2T & HFFMA2T

LSXY Estimates



All data to 2000 cycles

Non-functional Pads comparison IST



10:1 vias, fine grid
260°Reflow
2.5mm thick
IST

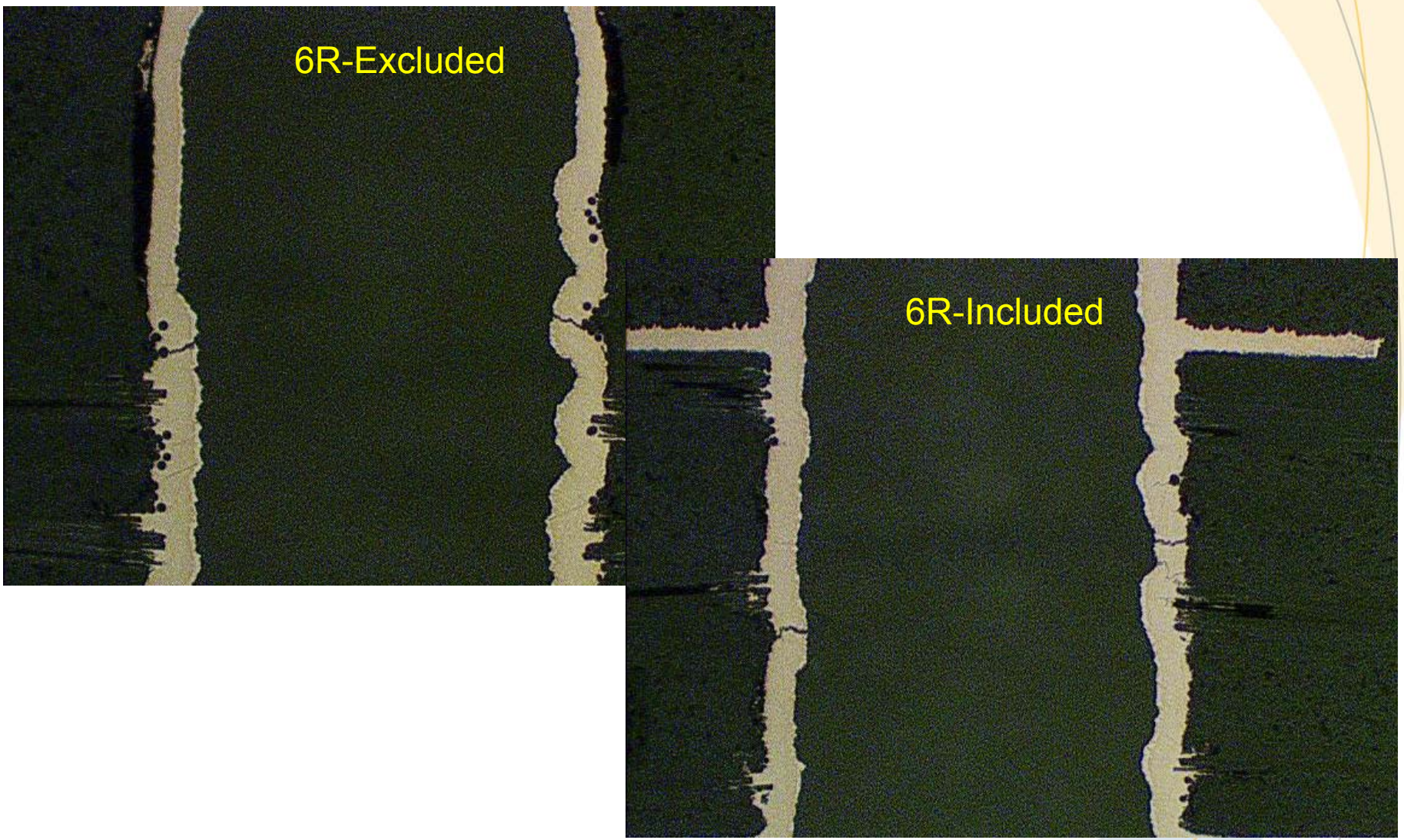
Non-functional Pads – Ag finish

- For Ag finish and high aspect ratio vias, earlier failures for non-functional pads included
- Similar results for both thermal cycling and IST
- This difference, although significant, should be considered second order alongside such issues as PCB manufacturing quality (copper plating quality) and materials characteristics (Tg, z-axis CTE)

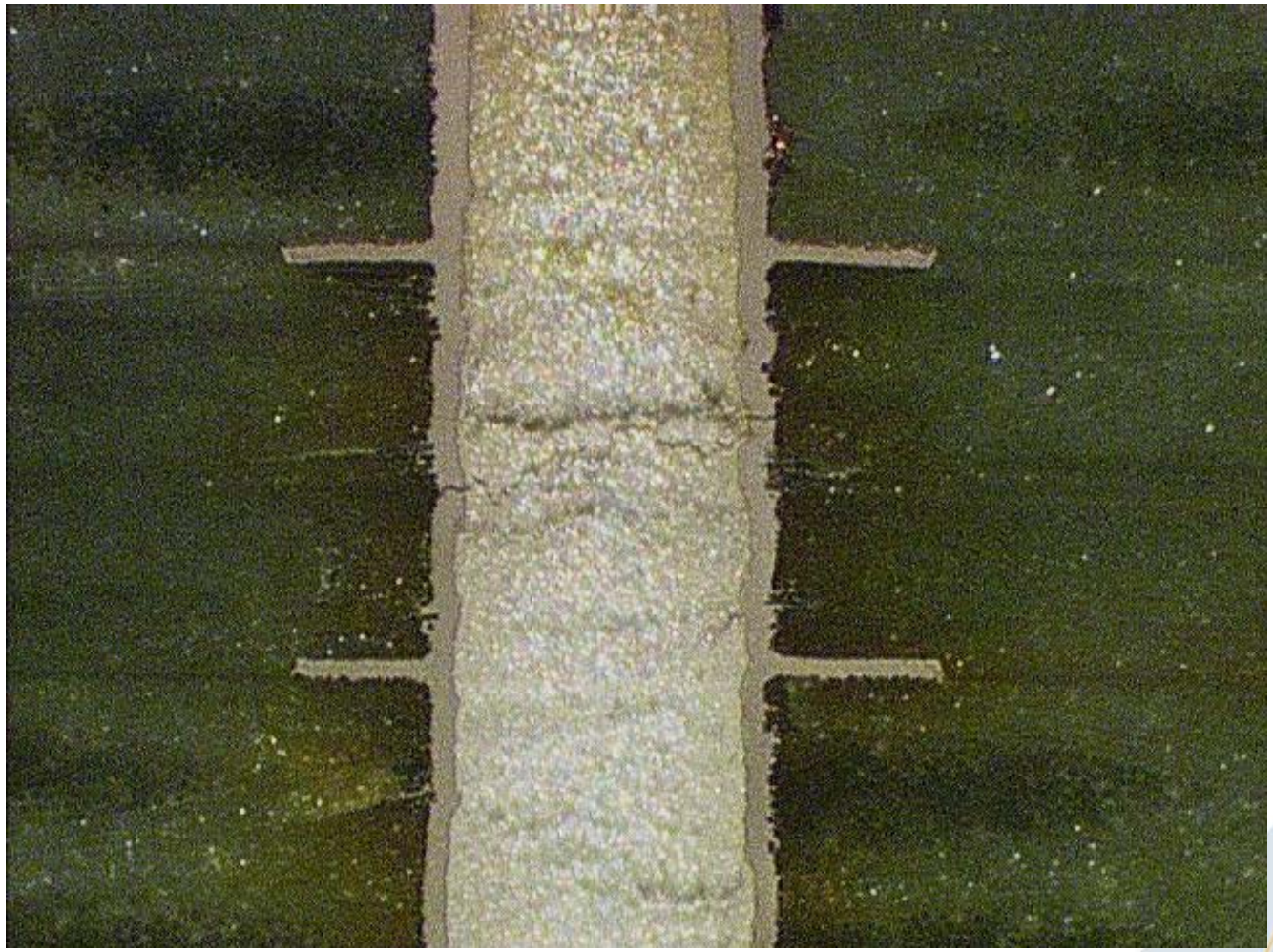
Non-functional Pads – Ag finish

- Micro-sections of failed vias showed high percentage of vias failed adjacent to the non-functional pads, even though these are away from the central portion of the via, where failures would normally occur.
- These correlates well with other evaluations that have been undertaken by PWB
- It has been postulated that the inclusion of non-functional pads acted as stress concentrators, leading to the earlier failure.

Comparison – 2.5mm Ag, 2000 cycles



Failure 2.5mm Ag, 2000 cycles, NF Pads included

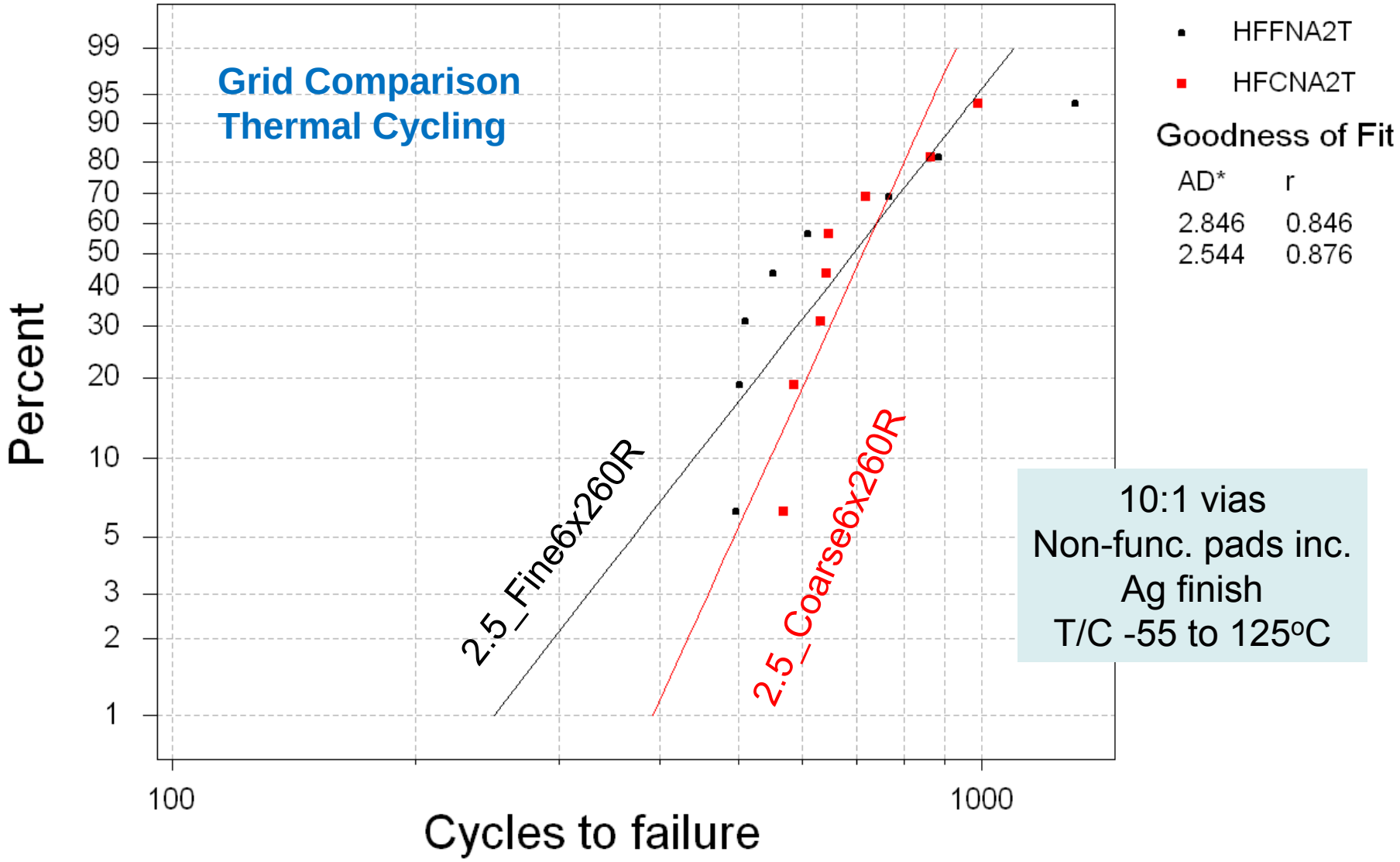


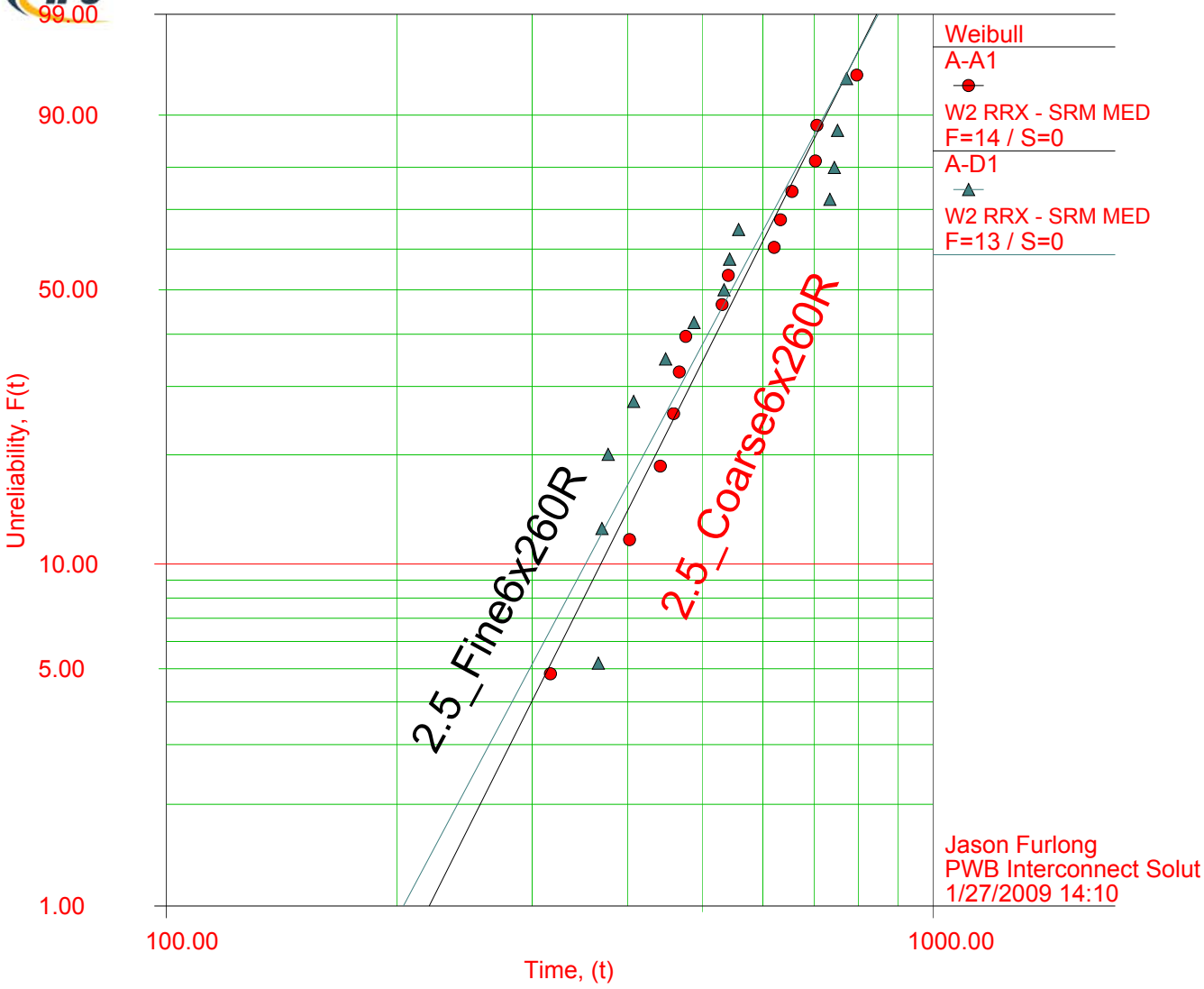
Comparison of Via Reliability

Grid Pitch Comparison
(Via proximity)

Probability Plot for HFFMA2T & HFCNA2T

LSXY Estimates



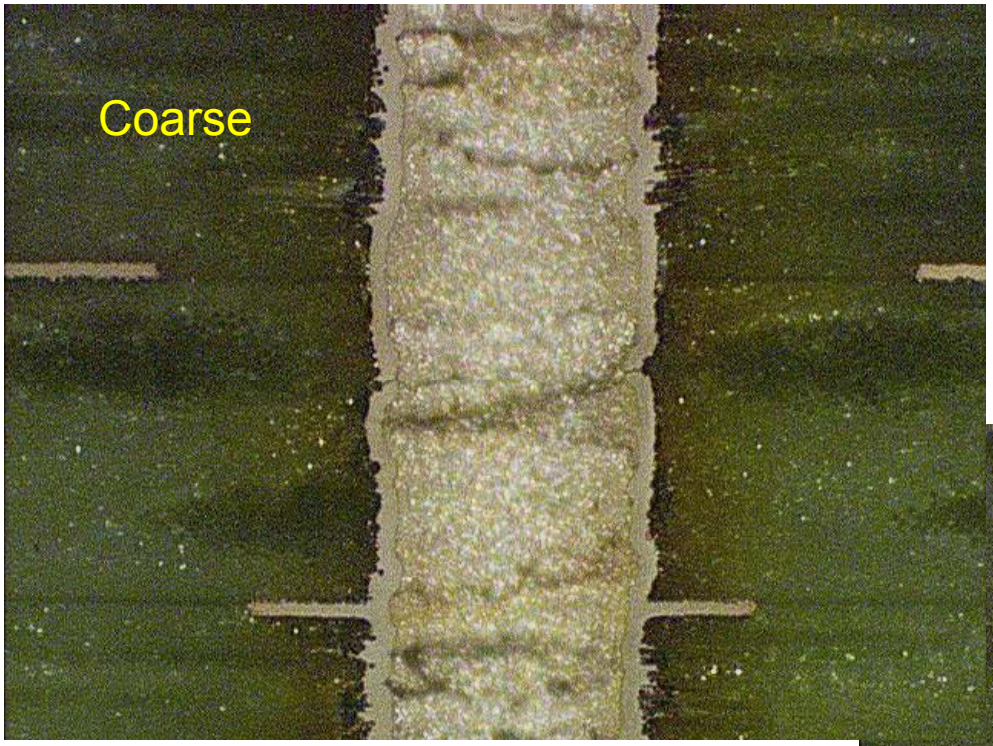


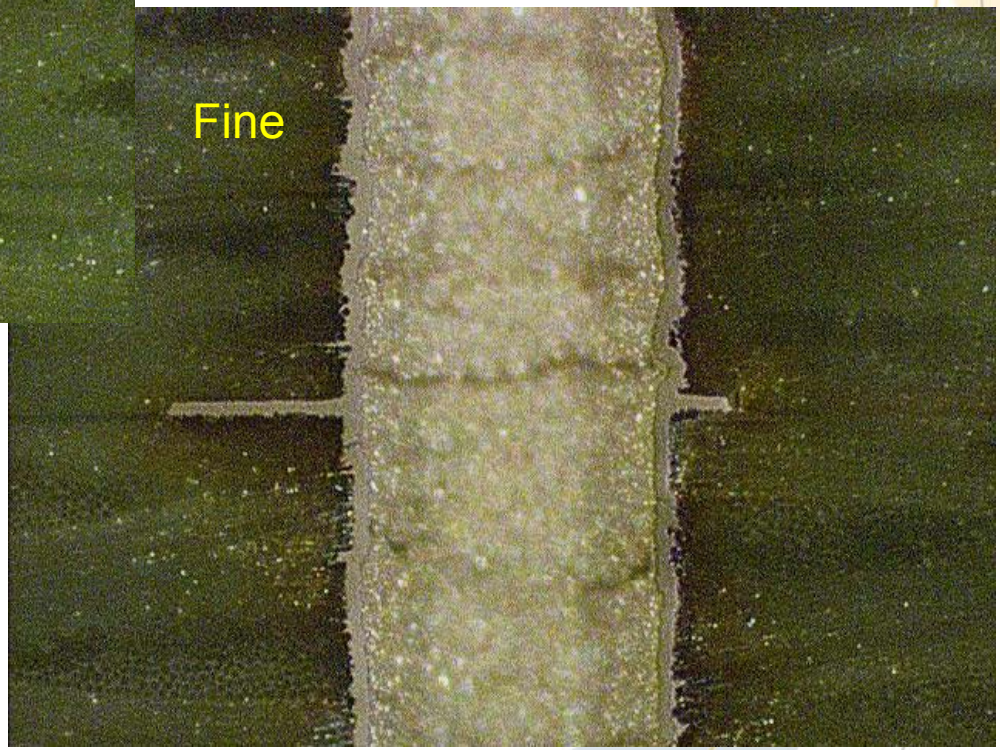
β1=4.5561, η1=604.4507, ρ=0.9865
β2=4.2943, η2=594.9284, ρ=0.9342

Grid Comparison IST

10:1 vias
Non-func. pads inc.
Ag finish
IST

Comparison – 2.5mm Ag, 2000 cycles

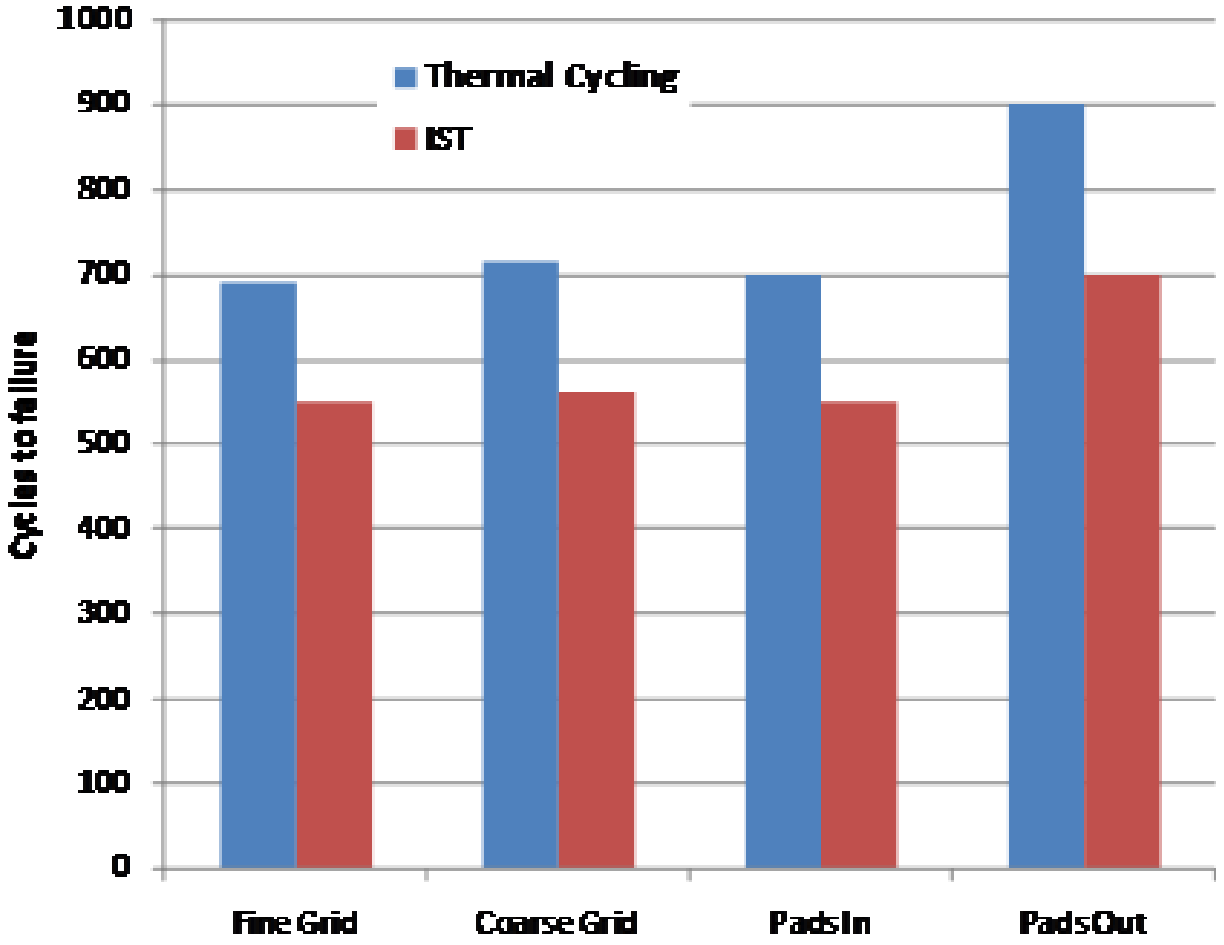




Grid Comparison

- No evidence to suggest different failure rate associated with different grid pitches

Comparison of Thermal Cycling/IST



Good correlation

Technique Comparison

- Failures occurred slightly earlier for IST than for thermal cycling.
  - More stringent failure criteria applied for IST
- Allowing for these differences, both techniques gave similar results with 50% failures occurring in the 500 to 900 cycles range.
- The relative ranking of the level of failures is identical for both the thermal cycling and IST but the results were obtained in very different timescales.

Technique Comparison

- IST has been shown to give fast comparable results to thermal cycle testing with constant monitoring
- Thermal cycling may be more beneficial if a wide range of experimental parameters are to be tested simultaneously

Conclusions

- Fine/Coarse grid comparison
  - No differences
- Inclusion of non-functional pads
  - For Ag finish and high aspect ratio vias, earlier failures for non-functional pads included
- T/C-IST Comparison

Thanks to

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- MBDA (UK) Ltd
- NEC
- Panda Europe
- Polar Instruments UK Ltd
- Polyclad Europe
- Rockwell Collins
- Rolls Royce Marine
- Substrate Systems Limited (SSL)
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