An Analytical Approach for the Design of Buried Capacitance PCBs

J. Lee Parker, Ph. D.
JLP Consultants, LLC

Introduction

There are presently several techniques for forming a buried capacitor in the core of a multilayer board. For purposes of this discussion, attention will be directed toward a sheet capacitor; although most of what is presented below can be extended to the other techniques as well.

A buried sheet capacitor is essentially a thin innerlayer. The core is composed of an organic material often reinforced with a woven glass structure. A classic example is FR-4. The laminate extends over the entire board and is essentially a very thin innerlayer. The copper weight is normally one ounce and the thickness of the dielectric is typically two mils or less.

The innerlayer is biased top to bottom thus creating a large capacitor in the interior of the multilayer board. Except for through hole connecting pads and antipads the innerlay is normally not imaged. A cross-section is depicted below:

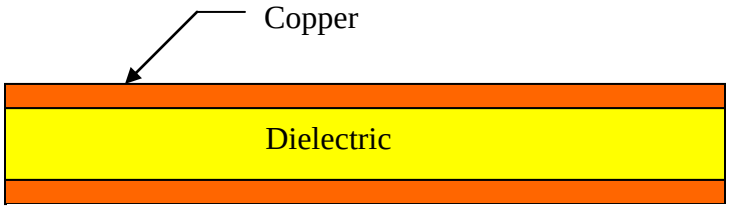

Fig 1 Sheet Capacitor Structure

The purpose of this technology is to offer the designer a technique for EMI suppression and an alternative to the by-pass capacitors normally mounted on the surface of the board to minimize "voltage sag" in the power being supplied to the active devices. A more complete discussion of the electrical performance will follow later.

Material Description

The parameter of primary interest in this construction is the capacitance per unit area of material. Typical values of unit capacitance and other parameters are shown in the Table (1) below.

Table 1. Electrical Properties of Typical Buried Capacitor Materials

Material	Dielectric Constant	Thickness Microns	Capacitance pF/cm^2
A	3.1	12.5	216
B	3.1	25	108
C	4.1	25	143
D	4.1	50	71
E	18	8	1962
F	18	16	981

Potential Advantages and Limitations to the OEM

There are potentially two major incentives for using a buried capacitance PCB design. The first is a reduction in EMI radiation. Buried capacitor innerlayers will reduce EMI radiation and often offer a simple solution to what can be a difficult and time consuming issue.

The second advantage is a reduction in the number of bypass capacitors required by a design to over come "droop" in the power delivered to an active device. Reducing the number of bypass capacitors obviously results in additional routing space on the outer layers of the board. This can result in a reduction of board size or even innerlayer count. Both of which reduce the cost of the board. Other advantages are a reduction in assembly cost, a decrease in the number of components, not to mention fewer solder joints which results in improved reliability.

The issues associated with buried capacitance are design tools, board material cost and fabrication. Also the number of potential fabricators is limited and some due diligence should be performed by the OEM to be certain any patent issues are resolved. The designer should also carryout "sanity checks" to verify the buried capacitance design will deliver the charge required to power the devices and that the design is compatible with the frequencies associated with the board. A few simple calculations will normally uncover any potential issues of this nature.

EMI Radiation

As frequencies increase, the EMI radiation becomes a serious problem. The amount of EMI radiation allowed by the different regulatory bodies is becoming more difficult for OEMs to satisfy. On occasions, OEMs have elected to use very expensive solutions to resolve this issue. Possibly the most extreme is to coat the entire rack that houses the electronic equipment with a material that will reduce the escaping radiation to an acceptable level. While this approach will overwhelm the issue, it will also drive the system cost to levels that are likely to be unmanageable.

Other OEMs have taken a less expensive approach which in many cases resolves the issue, but requires some upfront engineering analysis. In particular, the radiation is often emitted by only a few boards in the system. These can normally be identified by the speed of the board. Processor boards are especially suspected.

A procedure which normally identifies the offending boards is discussed below:

- Measure the EMI radiation from each of the suspected candidates; most likely this will identify the culprit.
- If this is the case, modify the design of these boards to include top and bottom buried capacitance innerlayers.
- Then measure the EMI radiation from these modified designs.
- If the radiation has been reduced to an acceptable level, then perform the system test for EMI acceptance.

This is a simple and cost effective procedure which is consistent with time to market considerations.

Replacement of Bypass Capacitors

As discussed in Reference (1) a popular solution to the so called "power sag" caused by the high inductance associated with most power distribution designs is the bypass capacitor. This issue is aggravated as the board's frequency is increased. Unfortunately, however, to combat this issue using bypass capacitors requires an array approach. This is particularly true on high frequency boards. In the array approach, many capacitors are connected in parallel with the power and ground connections of the device. While this approach is normally very effective, it requires a large amount of area on the outer layers; which in turn impacts routability. To compensate for this drawback, requires the use of additional layers and increased board area, all of which impact system cost.

A potential solution to this issue is buried capacitance. In many cases, where buried capacitance has been effectively used, the result has been reduced layer count and board size. Consequently, an appreciable cost savings has been realized.

Another advantage to the OEM is reduced assembly cost. Since board mounted bypass capacitors are no longer needed, the assembly cost is reduced. That is, the component cost and the labor required for assembly are diminished, not to mention the immediate yield improvement.

Design Issues

The paramount issue inhibiting the use of buried capacitance is a design procedure which will also predict at the outset the potential cost benefits of the technology. A proposed methodology is discussed below.

- The concerns that should be resolved at the outset are frequency issues and the available charge compatibility between the device and the buried capacitor. This is in the nature of a "sanity check" to verify there are no first order issues that will prohibit the use of buried capacitance. The bandwidth limitations and the amount of charge that can be delivered to an active device of a particular embedded capacitance design can be estimated by using the procedures in Reference (1) for sizing array capacitors. The additional information that is required to carry out these calculations for a buried capacitor design can be found in References (2) and (3). If these considerations do not present any limitations then the next step is to estimate the cost savings that can be realized by an embedded capacitance design.

  For example, one of the issues in a buried capacitance design is the current limiting effect of vias primarily caused by the inductance of the via. An analytical analysis of this issue is contained in Reference 2. One of the major results of this investigation is shown below in Figure 2. In this analysis, the time to discharge a buried capacitor innerlayer through a 13 mil through hole via and a 5 mil blind via is calculated for a particular board design.

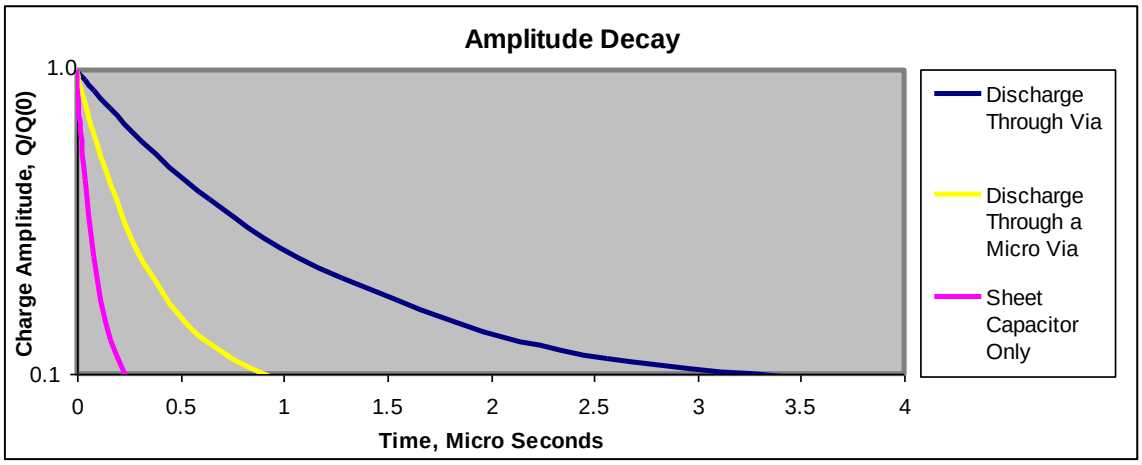

Figure 2

  The information in Reference 2 provides an analog for calculating the time for any buried capacitor design to discharge through a via and into a device.

  On toe other hand; Reference 1 contains the analogs for calculating the time available for the discharge to take place based upon the speed of the device. Taken together, a designer can perform a first order analysis to determine the suitability of a buried capacitance structure for a particular design. This and other considerations will determine if the proposed buried capacitor design is technically feasible.

- Supposing the design is technically feasible, a cost savings analysis should then follow. A procedure is discussed in Reference (4). There are also some user groups with software that reportedly performs the same calculations. The analysis is outlined below:

  - Calculate the area occupied by the bypass capacitors.
  - Estimate the additional routing that can be placed on the outer layer in the space originally occupied by the bypass capacitors.
  - Determine the potential cost savings that can be realized by reducing the board's form factor and layer count.
  - Determine, probably from a fabricator, a budgetary estimate for the additional cost of buried capacitance layers.
  - At this point, a judgment can be made of the potential cost savings that can be realized by incorporating embedded capacitance into the design. This should include reduction in board cost, assembly cost, cost of removed components and the additional cost of buried capacitance innerlayers.
  - This judgment should be quantified by an estimate of the confidence in the potential savings Vis a Vis the amount of savings.
  - If the amount of savings justifies the cost of a redesign using embedded capacitance then the redesign should be attempted.

Admittedly, judgment and some risk are involved in the process, which is the case in nearly all management decisions. According to numerous antidotal reports, however, the cost savings can be huge.

There is also a time to market component here as well. In a conventional design, it is often necessary to go through several design iterations of a part number until the power sag is overwhelmed. Each redesign normally requires new model boards (at a quick turn price) and a bench test; all of which are expensive and increases the time to market. Very often this redesign impediment can be largely avoided by incorporating an embedded sheet capacitor package. This in turn streamlines the product introduction process from conceptual design to market and thereby undercutting the competition.

Summary

Just as with most engineering issues, there is not a procedure to absolutely determine if a buried capacitor approach is best for a particular application. Choosing a buried capacitance approach will always involve some risk. An overview which may be of help understanding the risk to potential reward ratio for this technology is contained in the IPC white paper in Reference 5. This Reference is a high level discussion of the utility of both buried capacitors and resistors

At this point in the evolution of the buried capacitance technology there does not exist a rule of thumb for deciding if a board design will be enhanced by the inclusion of buried capacitance inner layers. The merits of each design should be evaluated on a case by case basis.

In the work above, we have presented a systematic approach for making this decision. A procedure for estimating the potential financial impact is included as well.

References

1. Johnson and Graham, High-Speed Digital Design, Prentice Hall PTR
2. Parker, J. Lee "Buried Capacity Analysis" Printed Circuit Design & Manufacture, June 2006
3. Bergstresser,T. et al "Embedded Capacitance Materials and Their Applications in High Speed Designs" IPC Expo 2003
4. Devenish and Palczewski (Harris Corporation), The Embedded Passives Journey, IPC APEX, 2007
5. An IPC White Paper – Embedded Passives: An Overview of Implementation, Benefits and Costs, V. St. Cyr, et.al.

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by

J. Lee Parker Ph. D.
JLP Consultants
Mechanicsville, VA
leep001@MSN.COM

Extent of this Analysis

- Buried sheet capacitors
- Advantages and limitations
  - EMI radiation
  - Replacement of by pass-capacities
- Design issues
  - Frequency limitations
  - Power requirements
  - Pulse time requirements
- A decision procedure for using buried capacitance

Design Purpose of Embedded Capacitance

- EMI suppression
- Minimize “power droop” in power signal delivered to active devices
- Thereby provide an alternative to placing by-pass SMT capacitors on the outer layers

Potential Advantages

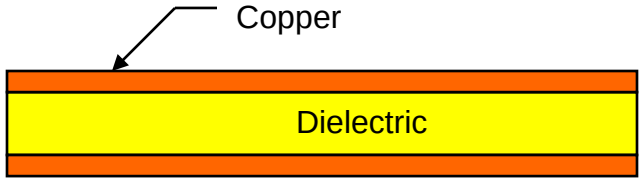
- Additional routing space becomes available on the outerlayers
- Potential Result
  - Decrease in board size
  - Decrease in number of innerlayers
- Reduction in number of components
- Reduced assembly cost
- Reduction in number of solder joints

Potential Issues

- Availability of design tools
- Limited number of fabricators especially in Asia
- Patent issues (some due diligence should be practiced by OEM)

Material

- Dielectric is usually an organic material
  - Often using a woven glass
  - *i.e.* FR4
- Each side of laminate is bonded to a continuous sheet of copper
- Imaging is typically connecting pads and anti-vias



Sheet Capacitor Structure

Material Performance

- The capacitance is:
  - $C \sim \varepsilon A/t$
  - Directly proportional to the dielectric constant
  - Inversely proportional to the thickness
- Thin innerlayers are more difficult to process
- Drilling and chemical processing are often acerbated by high dielectric materials

Material Properties

$C \sim \varepsilon A/t$

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EMI Suppression

- EMI radiation is in most cases proportional to board frequency
- Often most of the EMI radiation is caused by a few boards in the system
- Solutions
  - Insulate entire system -- expensive
  - Insulate selective boards with buried capacitance innerlayers – less expensive but requires engineering talent

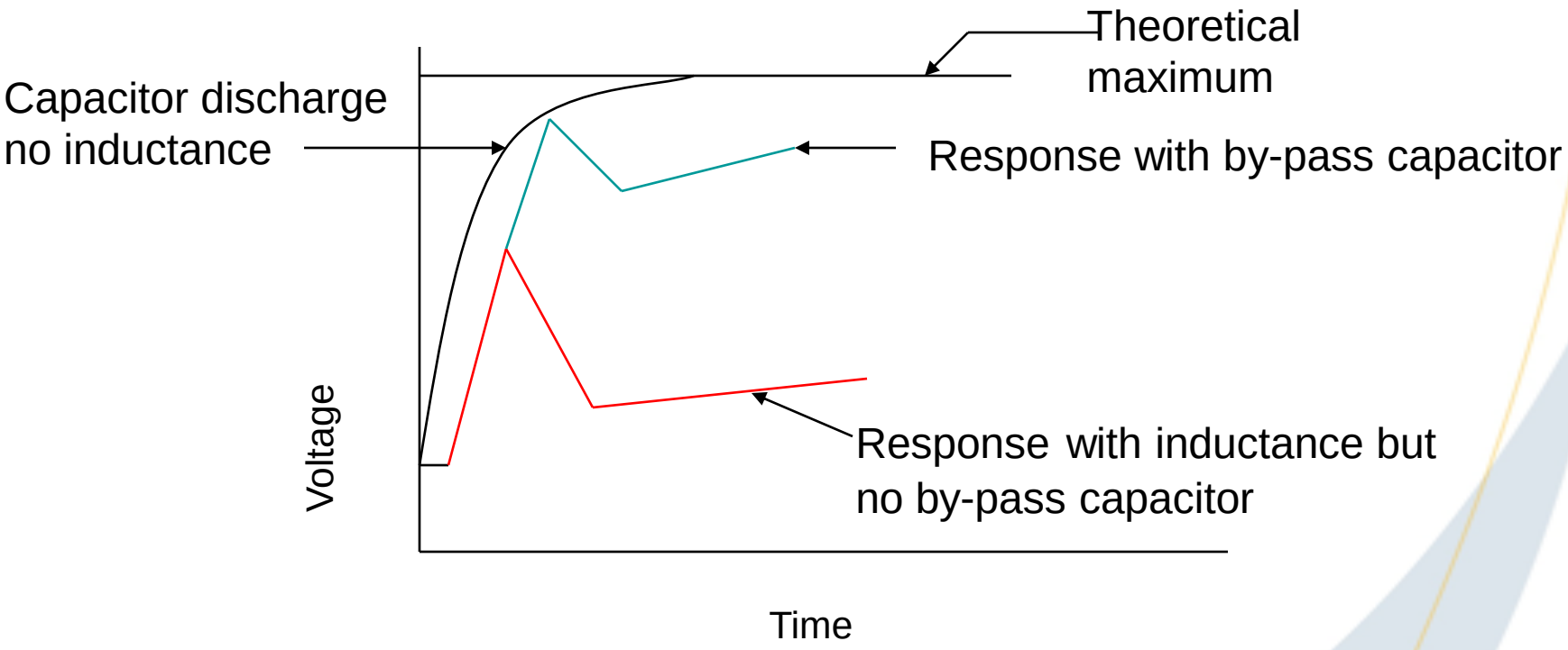
Design Procedure for EMI Suppression Using Buried Capacitance

- Identify high frequency boards within the system
- Verify selection by EMI measurements
- Add buried capacitor innerlayers to suspect boards
- Verify EMI reduction:
  - At board level
  - Then system level

By-Pass Capacitors

Purpose of Bypass Capacitors

- Minimize sag of power signal at active devices
- Principal cause: inductor reactance ~ 2πfL



By-Pass Capacitor Design Concept

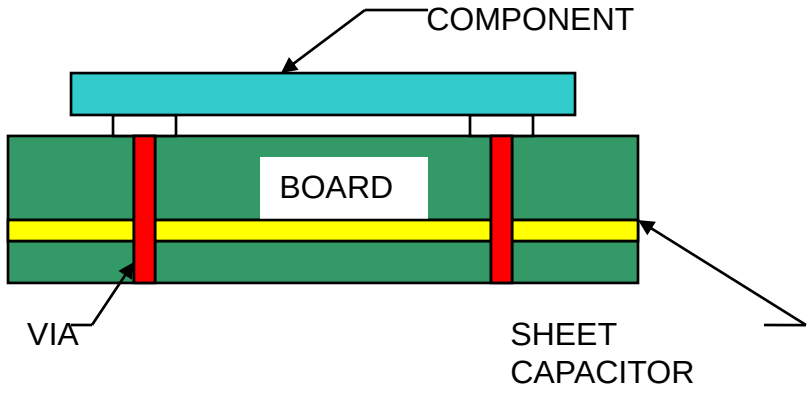
Bolster the power signal

- By using an array of outerlayer capacitors
- Array is located very close to device
- Connected in parallel to power and ground connections of the device

- Drawbacks
  - Often requires a large number of capacitors
  - Occupies space on outerlayer blocking routing options

Alternative Solution Embedded Capacitance

- Form a capacitor using power and ground planes
- Place vias directly from device connection to power and ground planes



Embedded Capacitor Feasibility Analysis

- Technical feasibility
- Economic feasibility

Embedded Capacitance Performance

- Connection is composed entirely of vias
  - No lead inductance
- Most power loss caused by via inductance
  - Impact of via inductance can be appreciable
  - Inductance is ~ to the length of via
  - Impact can be reduced using blind vias

Typical Electrical Values (via)

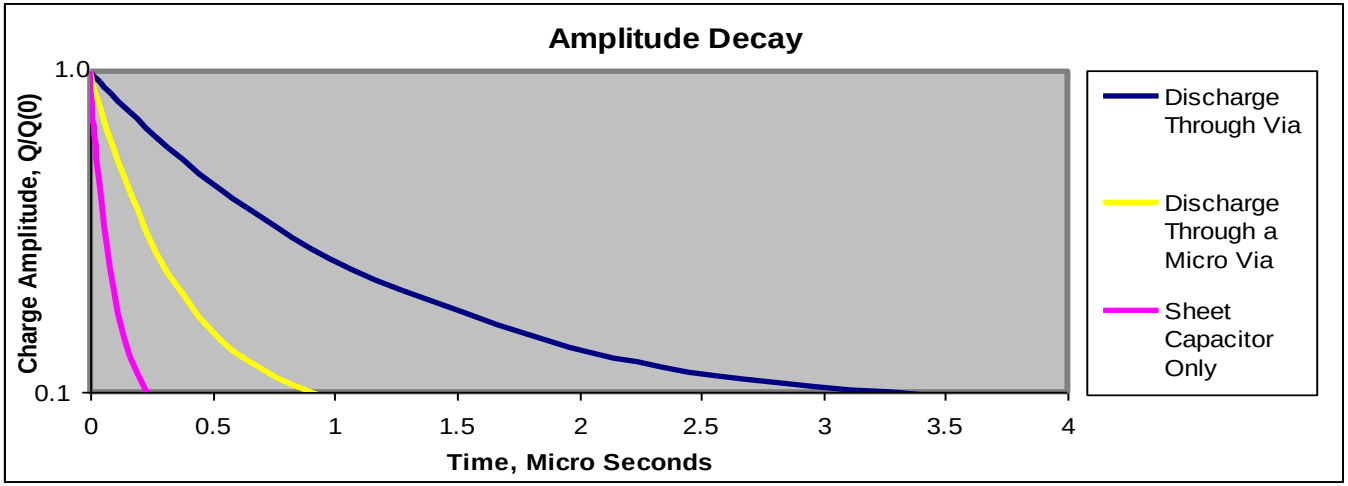
- The resistance of a 13 mil via with 1.0 mil of copper in a 62 mil thick board is
  - $R_V = 1.4 \times 10^{-3}$ Ohms
- The inductance (in nH) is

$$L_V = 5.08h\left[\ln\left(\frac{4h}{d}\right)+1\right]$$

- h is the length of the via and d the diameter
- $L_V = 1.2$ nH
- Notice the inductance is primarily controlled by the length of the via while a weak function of the diameter

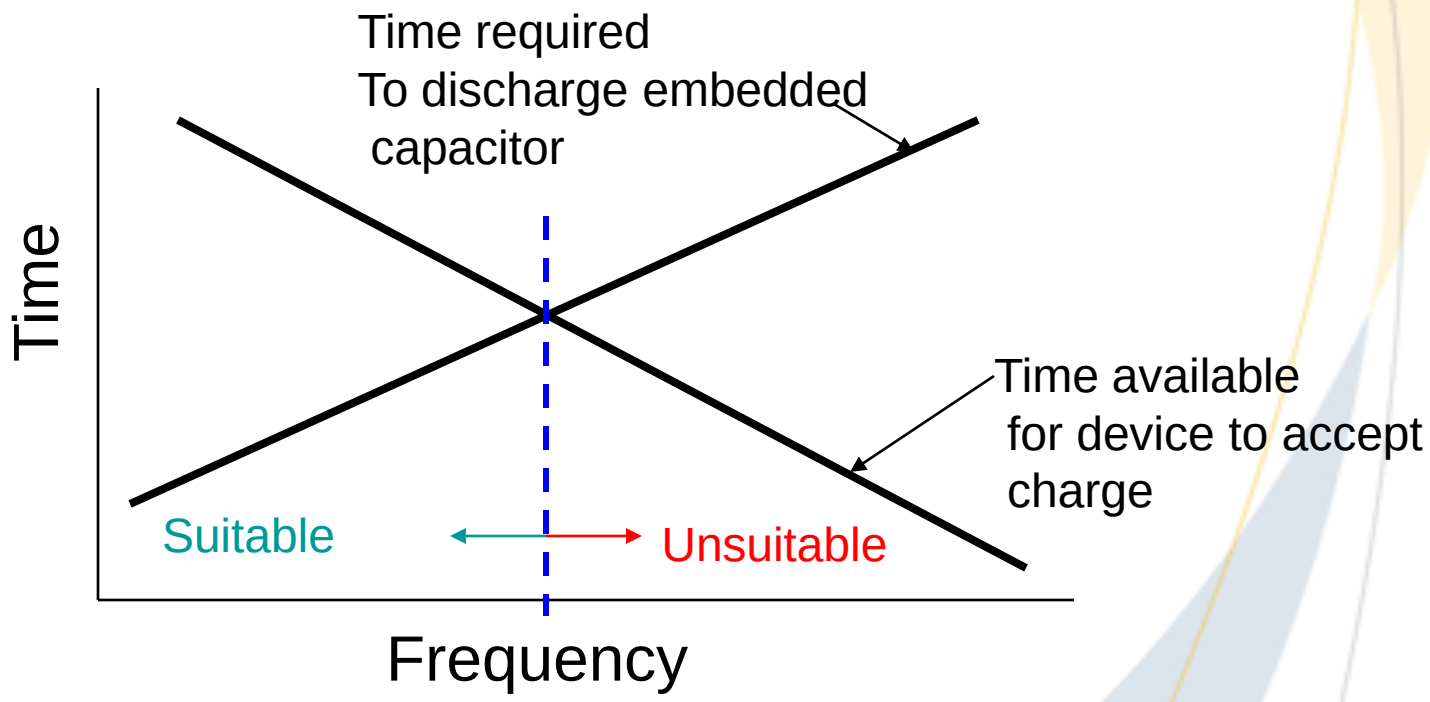
Effect of Via Construction on Buried Capacitance

- The discharge time of a typical embedded capacitor capacity is given below
- This needs to be compared to the available pulse time to charge device (See Johnson and Graham “High Speed Digital Design”)



- See PC Fab June, 2006 for details

Embedded Capacitor “Sanity Check” for Technical Feasibility



Buried Capacitance Economic Analysis

- Start with the conventional design
  - Determine area required for by-pass capacitors
  - Estimate additional routing that can be placed on outerlayers if all by-pass capacitors are removed
  - Estimate savings by reducing layer count or form factor
  - Estimate assembly and component cost savings
  - Estimate additional fab cost for embedded capacitance
- Estimate cost impact
- If justified, design an alternative using embedded capacitance
- See paper by Devenish and Palczewski APEX 2007
- There will be risk

Additional Overview of Several Embedded Technologies

- IPC white paper
  - Embedded Passives: an Overview of Implementation, Benefits and Cost, V. St. Cyr,*et.al*
  - Discusses embedded resistors and capacitance
  - Includes various fab techniques
  - See Susan Filz @ IPC office

Thank you

J. Lee Parker Ph. D.
JLP Consultants
Mechanicsville, VA
leep001@MSN.COM