Virtual Access Technique Extends Test Coverage on PCB Assemblies

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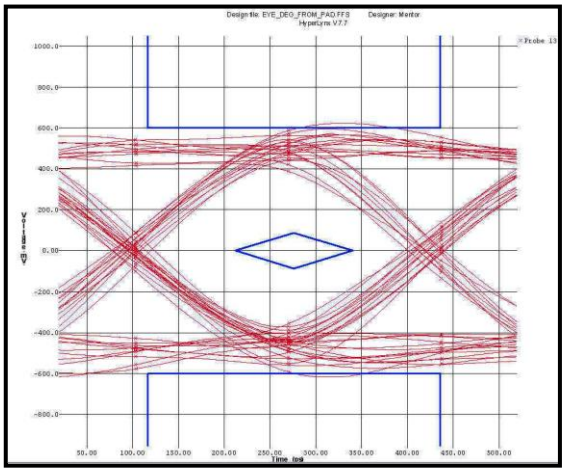
Abstract
With greater time to market and time to volume pressures, manufacturers of populated printed circuit boards have traditionally relied upon un-powered vectorless testing to quickly and reliably identify open pins on integrated circuit devices and connectors that reside on populated PCB assemblies. Unfortunately with the advent of higher speed signals, PCB designers can no longer tolerate the negative transmission line effects of test pads that are used to gain electrical access during in-circuit testing. An improved vectorless test method has been developed to address the loss of test coverage on high speed signals that reside on contemporary printed circuit board assemblies. This technology can quickly and effectively identify open connections between a boundary scan based device and other connected devices including a non-boundary scan device, a connector, or a socket. A discussion of this new vectorless test method, employing virtual access, is the focus of this paper.

Introduction
Detecting open solder connections on printed circuit board (PCB) assemblies continues to be a major challenge on today's manufacturing floor. Capacitive based vectorless techniques such as FrameScan FX™ have met the demand of finding such manufacturing defects on the majority of a PCB's solder connections. However, yesterday's slower signals and parallel bus architectures are being steadily replaced by much higher speed serial busses. Examples of these new busses include PCI Express 2.0 which operates at a speed of 5 Gb/second [1] and SATA 3.0 which operates at a speed of 6 Gb/second [2].

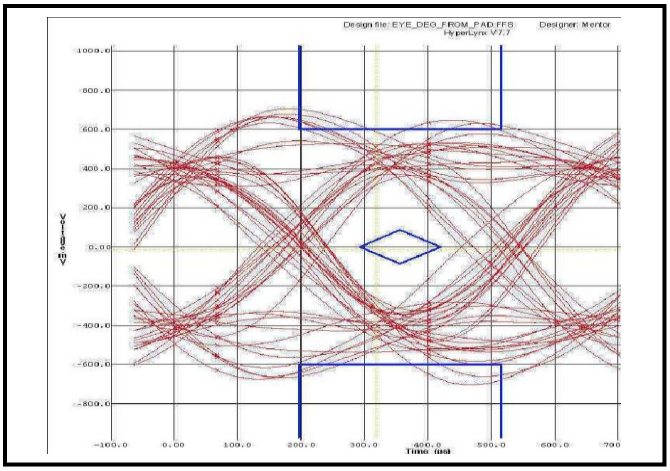
These higher speed signals and busses require a transmission path that is as uniform as possible in terms of the characteristic impedance. The characteristic impedance of a transmission line is equal to the square root of the per unit length of the conductor's inductance divided by the per unit length of the conductor's capacitance.

Adding a test pad to a given length of signal etch increases the capacitance at that particular location, causing a discontinuity on the signal path. This added capacitance effectively lowers the characteristic impedance at that physical location and imposes non-uniform impedance for the signal path that can cause waveform fidelity issues.

Figure 1 illustrates the effect of a high speed differential without and with test pads. As can be seen from this illustration, the differential signal without the test pads has a large open "eye" which indicates a cleaner signal than the diagram to the right where the signal "eye" appears more closed. In this test case at a 0.32ns bit interval rate, the addition of 35 mil pads to high speed signals results in a negative result with regard to waveform fidelity and can increase inter-symbol interference.



Differential signal without test pads



Differential signal with test pads

Figure 1.

Removing the test pads from the signals will solve the operational issues with these signals; however the loss of test access will negatively impact the manufacturer's production yields. As a result, a new method of testing the signal connections for connectivity defects that does not require test pads needs to be devised.

This paper describes a novel technique of harnessing the capacitively coupled opens technique in combination with the built-in testability features of modern integrated circuits to identify this class of open and short pin defects.

Test Method

The new method of identifying open and shorted pins on IC devices, connectors and IC sockets is based upon the concept of combining a virtual signal generator with traditional capacitive coupling technologies. This technique is called "Powered Opens". The virtual signal generator can take the form of an 1149.1 compliant boundary scan based device [3] on the unit under test or some other digital part. All boundary scan IC devices are controlled by a test access port, or TAP. This TAP is used to properly initialize the device and to generate the necessary digital stimulus for the capacitive opens based detection plate which is located proximate to the second interconnected device. In practice, the output signal for each tested connection is digitized and then analyzed in the time domain to determine potential connectivity issues.

There are two basic processes involved in identifying open or shorted pins. The first is called the learn phase, whereby a known good PCB assembly is tested to "learn" the characteristics of the assembly during the test program development. Typically several known good PCB assemblies are learned and an average profile is used as reference. The second phase is the actual production test phase whereby boards of unknown quality are tested for open and short defect conditions.

Time Domain Analysis Method

During the software "learn" process, the tester properly conditions the boundary scan device to output a positive and a negative going transition for every pin that is to be tested for connectivity defects. Each signal edge for each pin being tested has its own unique time slot that is non-overlapping with any other pin activity.

Although the rising and falling edges can have some short dwell time, resulting in a narrow digital pulse, the opposite edges can be substantially apart from each other with other pins being tested in between this long dwell time. A sensor plate, located proximate to the device being tested is used to detect the capacitively coupled transient signals that are caused by the rising and falling stimulus signal edges. This resultant signal is digitized by an instrument that is preferably part of the in-circuit tester's analog measurement system. The digitizer is synchronized to the in-circuit tester's digital system that is controlling the output signal actions of the on-board boundary scan component. In this way, it is possible to know when to start sampling the resultant signal and to have knowledge of which digitized samples correspond to which stimulus edge of which pin.

In the preferred embodiment of the technique, the capacitive plate will also contain an active buffer that sends the signal to a multiplexer module that selects which probe plate to use for each specific test as shown in figure 2.

The data is analyzed in a method that is different from other traditional vectorless techniques in that the analysis is performed in the time domain, rather than in the frequency domain.

When in production testing, an open pin connection will typically yield a signal that is considerably smaller than the learned value making open connections readily detectable. Shorted pin conditions are traditionally easy to identify without ambiguity with full electrical access using analog measurement techniques [4]. These same short defects are typically more difficult to accurately diagnose with virtual pin access due to a metrology difference. However, utilizing boundary scan cells that have self-monitoring capability can be used to help diagnose these shorted pin conditions as sited in reference [5].

Figure 3 illustrates the typical signal difference between a connected and an open pin. Figure three depicts measurements taken on three pins of a 20 mil pitch SOIC device. Pins 12 and 19 have open connections while pin 27 is connected. As can be seen in the relative pin responses, there is clear differentiation in the relative response of a connected pin and the two open pins.

Note that the plot of the three different pin measurements appears continuous in nature, but it is not. This is because the plot represents the data stored in the digitizer's memory that was triggered three times for the three pin measurements. Between pin measurements, there is dead time not shown that was required to load toggle data into the boundary scan chain.

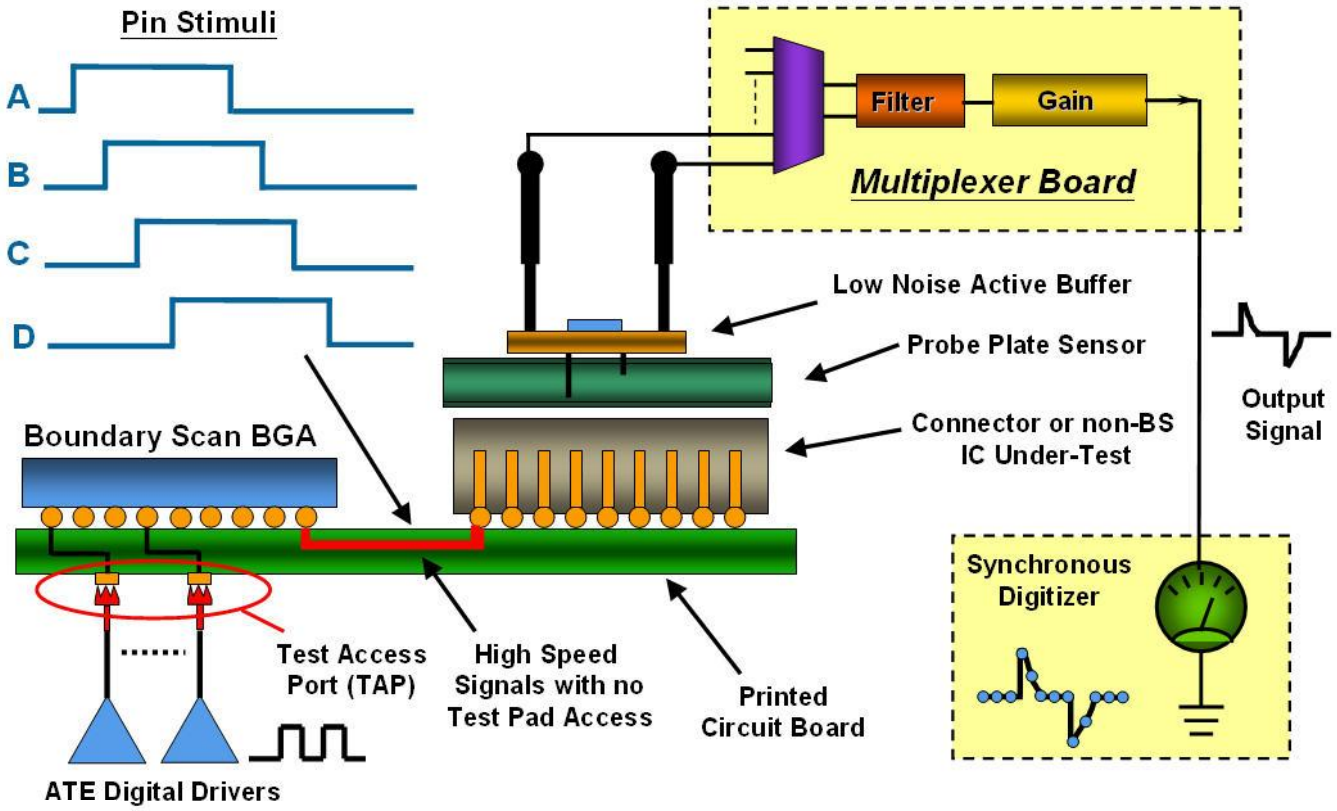


Figure 2.

Frequency Domain Techniques:
Many of today's contemporary vectorless opens techniques [6] rely upon applying a sine wave stimulus of several cycles to the device under test for the express purpose of finding open and short electrical connections on integrated circuit devices, connectors and sockets. The resultant signal is then typically analyzed in the frequency domain and may be digitally processed through a Discrete Fourier transform to help eliminate much of the noise in the signal.

With the advent of techniques that combine capacitively coupled vectorless test methods with boundary scan methods [7], [8] there is an desire from the original equipment manufacturer (OEM) to continue to use a known working metrology by using a stream of square wave excitations from the output of an active boundary scan part, as this most closely mimics the attributes of using a sine wave excitation. For suppliers of in-circuit test equipment, this minimizes the changes in the analysis software and also minimizes technology risk.

Generating this square wave stimulus via the boundary scan chain has a practical limitation however. This is because most opens test technologies rely upon applying a particular narrow range of sine wave stimulus for the purpose of performing opens measurements.

The opens test frequency is typically in the range of approximately 10HKz. This is because lower frequencies will result in lower resultant signal amplitude which will lower fault coverage. Frequencies in excess of 10KHz tend to couple into the opens detector plate from the PCB as well as well as from the part being tested, resulting in false pass opportunities.

This narrow range of useable frequencies becomes problematic when the stimulus is being synthesized through a boundary scan chain. This is because the square wave output frequency on a boundary scan output pin is a function of the TAP TCK clock frequency as well as the number of scan cells that are in the scan chain [5].

As a result, with the vast variety of board types with varying boundary scan IC content and large number of scan cells, it is difficult for the ICT supplier to provide a stimulus frequency that is within the range of their hardware operating envelope. However, the time domain analysis technique described in this paper will work with any boundary scan device and is not limited to the deployment of custom silicon that relies upon the addition of custom boundary scan commands.

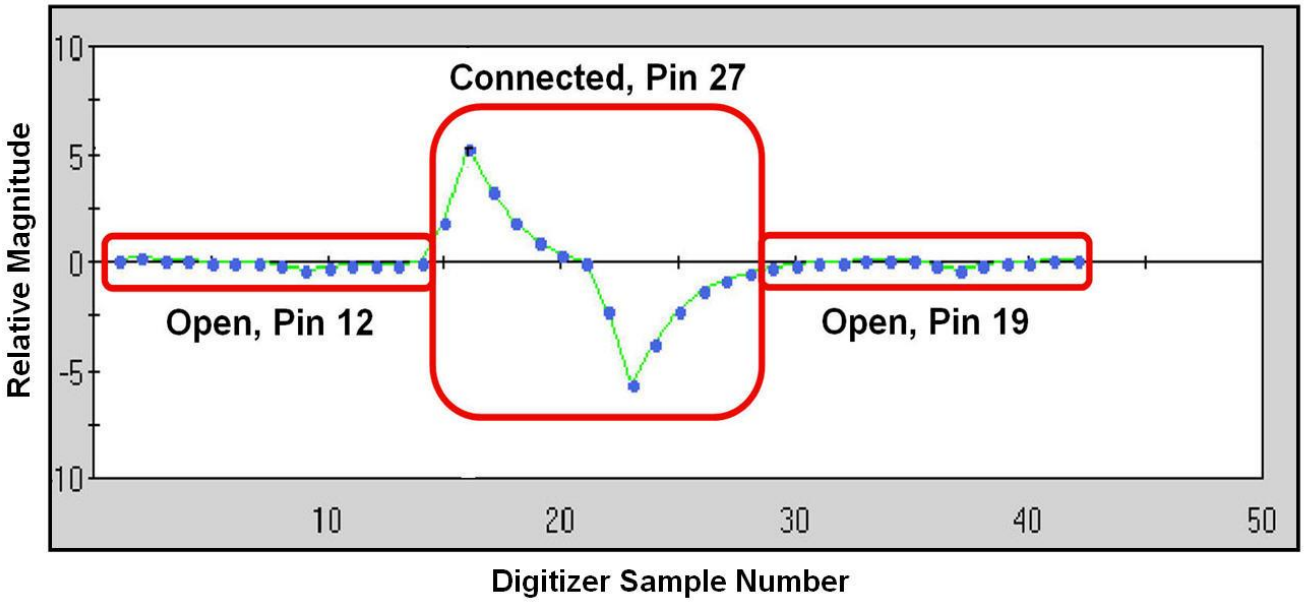


Figure 3.

Signal Analysis

The resultant data for a tested pin is first sorted out from the digitizer's memory and reconstructed into a single long data vector. This vector is created by simply placing the negative edge data samples directly after the last data point of the positive vector. In one portion of the analysis software, the resultant data vector for a pin is cross-correlated to a learned, de-normalized auto-correlation vector that was previously spliced together in a similar manner. This cross-correlation is of a de-normalized type and is shown in equation 1.

In one preferred embodiment of the learn process, several de-normalized auto-correlation values are calculated and averaged to create the reference value for the production cross correlation. This practice also allows one to calculate the mean and standard deviation of a number of auto-correlation values to ensure that there is not excessive variation due to noise. Should there be excessive variation as indicated by a standard deviation value that is large, as compared to the mean value, the pin will be discounted from the test.

$$R(d) = \sum_{i} [\ (x(i) - mx\ ) * (y(i) - my)\ ]$$

Equation 1.

Referring to equation 1, X(i) and Y(i) are the data vectors to be correlated, Mx and My are the mean values of the two vectors. Before a pin is determined good or open, the de-normalized auto-correlation is first performed during the learn process. This will result in a numeric value that will be compared against the de-normalized cross correlation result that is created during production testing. If the de-normalized cross-correlation is either less than or greater than the de-normalized auto-correlation value by a certain percentage, then the pin is then deemed to be defective, otherwise the connection is considered a good one.

The cross-correlation coefficient that is calculated during production test represents the likelihood that the measured signal matches the reference signal in temporal response as well as in magnitude response. It is this correlation result that is then compared against the auto-correlation value. The correlation technique that is described is resistant to random noise in the signal, helping to reduce false calls on the manufacturer's production floor.

Experimental Results

Powered opens utilizing time domain analysis has been applied to a number of different PCB assemblies with good results. One such example involves testing a LGA771 processor socket on a PC mother board. This high density 771 pin socket is shown in figure 4 below.

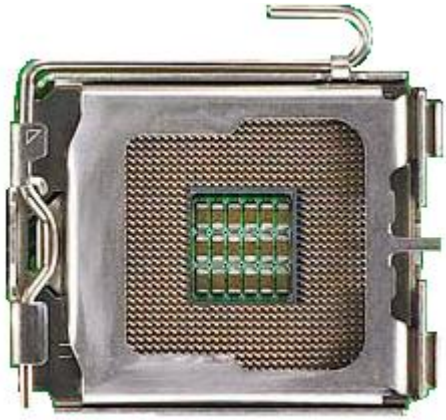


Figure 4. LGA771 processor socket

The socket was stimulated with the boundary scan outputs from a memory controller chip on the same assembly. The results for twelve of the socket pins are shown in figure 5 below. Each positive and negative pulse pair corresponds to a different pin on the socket. The pin numbers are listed at the bottom of the chart. The blue pulses reflect good pins that were toggled, while the pink trace reflects the same pins in a connect state but not toggling. As a result, the pink trace indicates the relative noise in the measurement. Finally, the yellow trace represents an open connection on pin A3 of the LGA771 socket. As can be seen, in figure 5, there is good differentiation between a connected pin and an open pin with the open pin level approaching the noise floor of the measurement.

Another example of powered opens test results is shown in figure 6. In this application, the riser connector of a server class computer board was tested using the time domain technique. Rather than plotting the digitized time domain values as in figure 5, figure 6 shows the results of the cross-correlation algorithm for twelve of the riser pins. The blue trace represents the relative measurements of connected pins that were toggled, the pink trace represents pins that were connected but were not toggling (to simulate the noise floor) and the yellow data points represent three open pins. As can be seen, there is excellent discrimination between open and connected pins with at least a 22 to 1 difference in this test case.

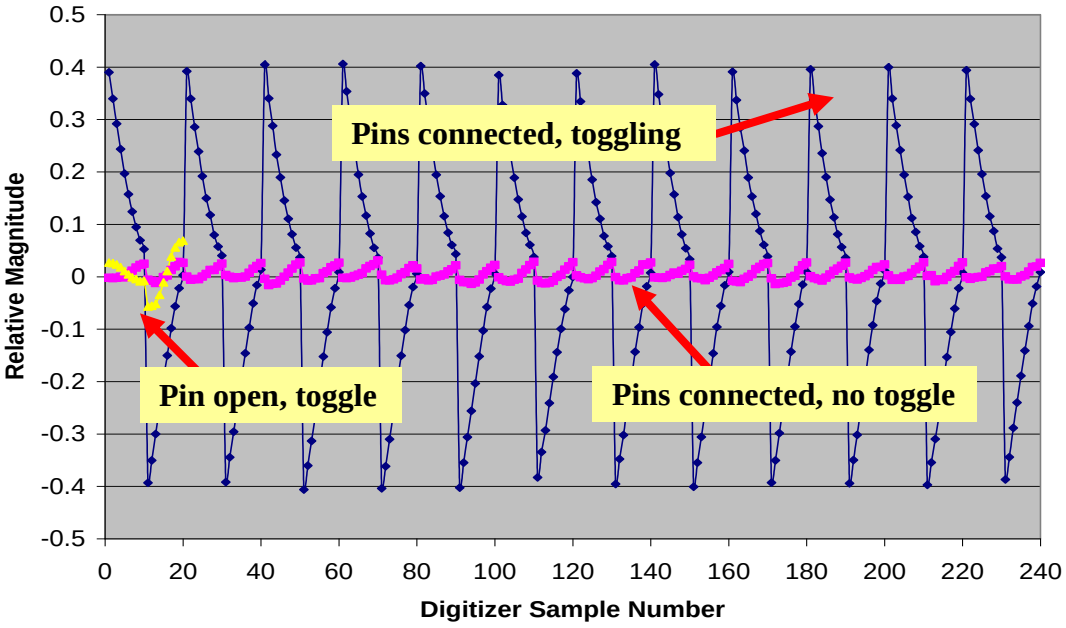


Figure 5.

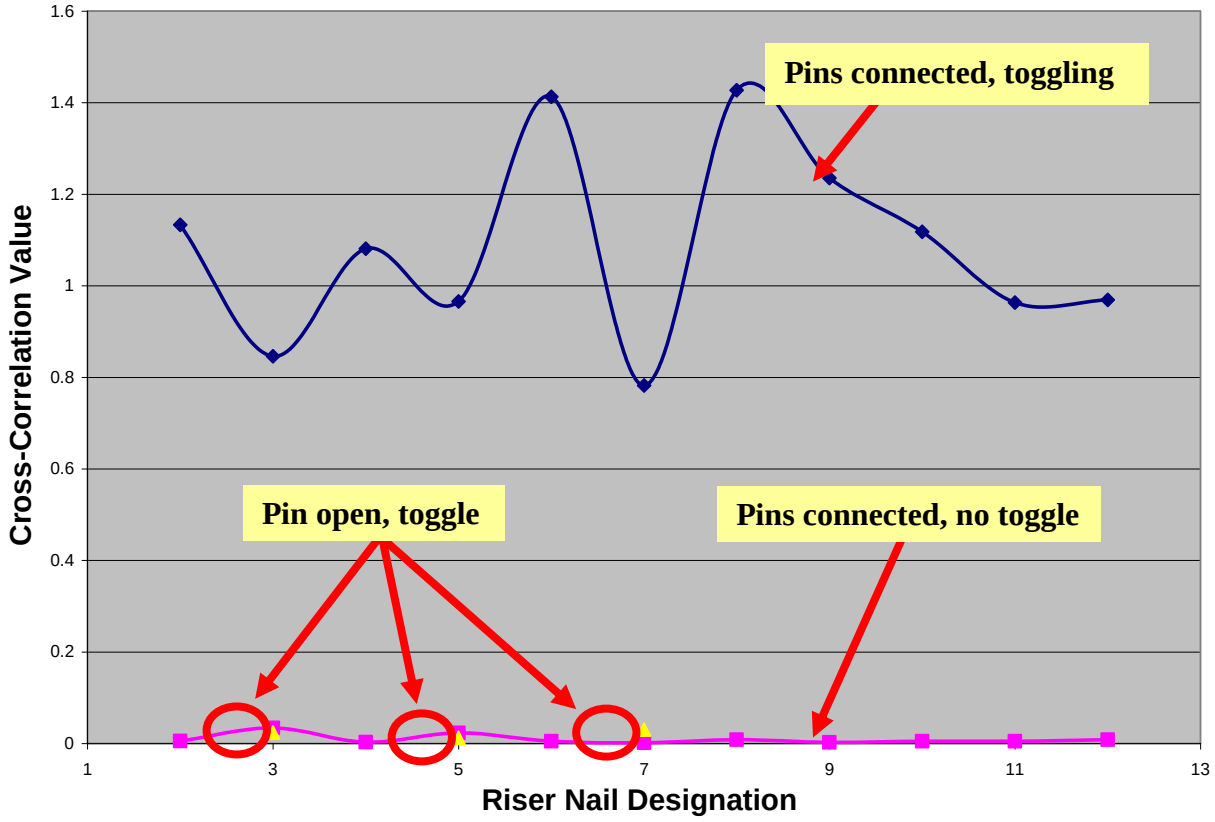


Figure 6.

Signal Interference

There can be situations where other signals can interfere with the intended stimulus signal and possibly result in less reliable results. Some in-circuit testers have sophisticated software algorithms that can largely eliminate any un-wanted on-board activity when testing a target component, so this is normally not a problem with this class of ICT system. However, in order to generate a stimulus signal from a boundary scan part, the test access port's clock, called TCK, must be active.

It is possible to have test cases whereby the boundary scan clock (TCK) is also attached to the same device to be tested for opens. In this case, a pin being toggled for connectivity test and the TCK signal will mix and add or subtract, depending on the transition states of the concurrent edges. An example of this interference is shown in figure 7, where the top signal is the TCK boundary scan clock, the middle signal is the pin being toggled and the bottom signal is the combined output of both signals as viewed from the output of the multiplexer card (see figure 2).

As can be seen in figure 7, there are instances where the edges of TCK and the toggled pin reinforce each other and other instances where they essentially cancel each other.

The time domain technique described in this paper is resistant to this level of correlated signal interference and can still differentiate between a connected pin and an open pin.

Technique Limitations

Although the combination of capacitive opens and boundary scan can increase coverage on boards with either high speed nets or on boards with density issues that cannot afford large test pads, there are several limitations that need to be mentioned.

The first limitation is that the boundary scan component pins can act as a stimulus source only if the pin is either an output pin or a bi-directional pin. As a result, nets that connect to boundary scan inputs are un-testable with this method.

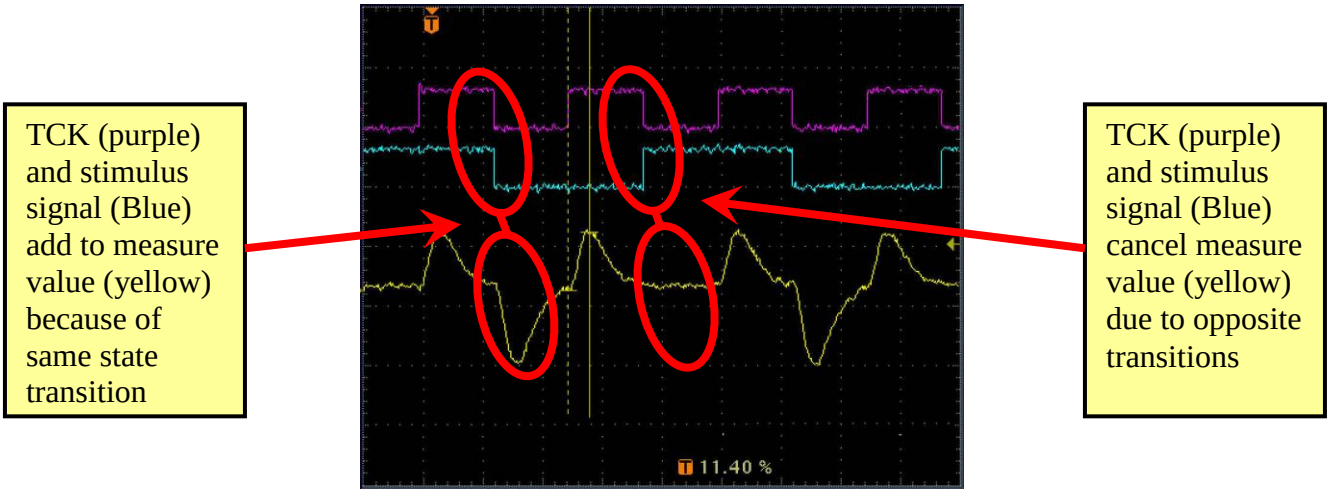


Figure 7.

A second limitation relates to differential signals and fault diagnostics. If one of the two signals that comprise a differential signal are open, there will be a discernable signal change that can be used to diagnose an open pin condition on one of the two nets. If both pins are connected, the signals cancel each other and the capacitive detection scheme measures no signal. The same "no signal" condition is also detected however, if both pins of the signal pair are open. As a result, a fault class of both nets open cannot be distinguished from a both nets properly connected condition.

Work is underway by a committee that proposes the enhancement of IEEE 1149.1-2001 by adding new capabilities at the periphery of the IC, controlled by a new, optional test mode instruction. This same committee is also working to find a solution to the differential signal cancellation issue and to gain stimulus capability on input signal pins [9].

Conclusion

A new test technique is proposed that allows for virtual access on high speed PCB signals that can no longer tolerate the negative effects of electrical test pads. The technique can also be utilized in high density PCB assemblies where there is limited board real-estate for test pad access.

When using time domain edge analysis instead of the more traditional frequency domain analysis, there is no restriction on the number of scan cells in the chain. As a result, the time domain technique can identify common process defects and is compatible with present and future boundary scan compliant silicon devices.

Acknowledgments

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References

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[3] "IEEE Standard Test Access Port and Boundary-Scan Architecture", IEEE Std 1149.1-2001
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[7] Brooks, Leslie, "Testing the Integrity of an Electrical Connection to a Device Using an Onboard Controllable Signal Source", US Patent #6,104,194, Aug. 15, 2000
[8] Brooks, Leslie, "Method and Apparatus for Finding and Locating Manufacturing Defects on a Printed Circuit Board", US Patent #6,144,201, Nov. 7, 2000
[9] "A-Toggle Working Group", see: http//grouper.ieee/groups/1149/atoggle/

Virtual Access Technique Extends Test Coverage on PCB Assemblies

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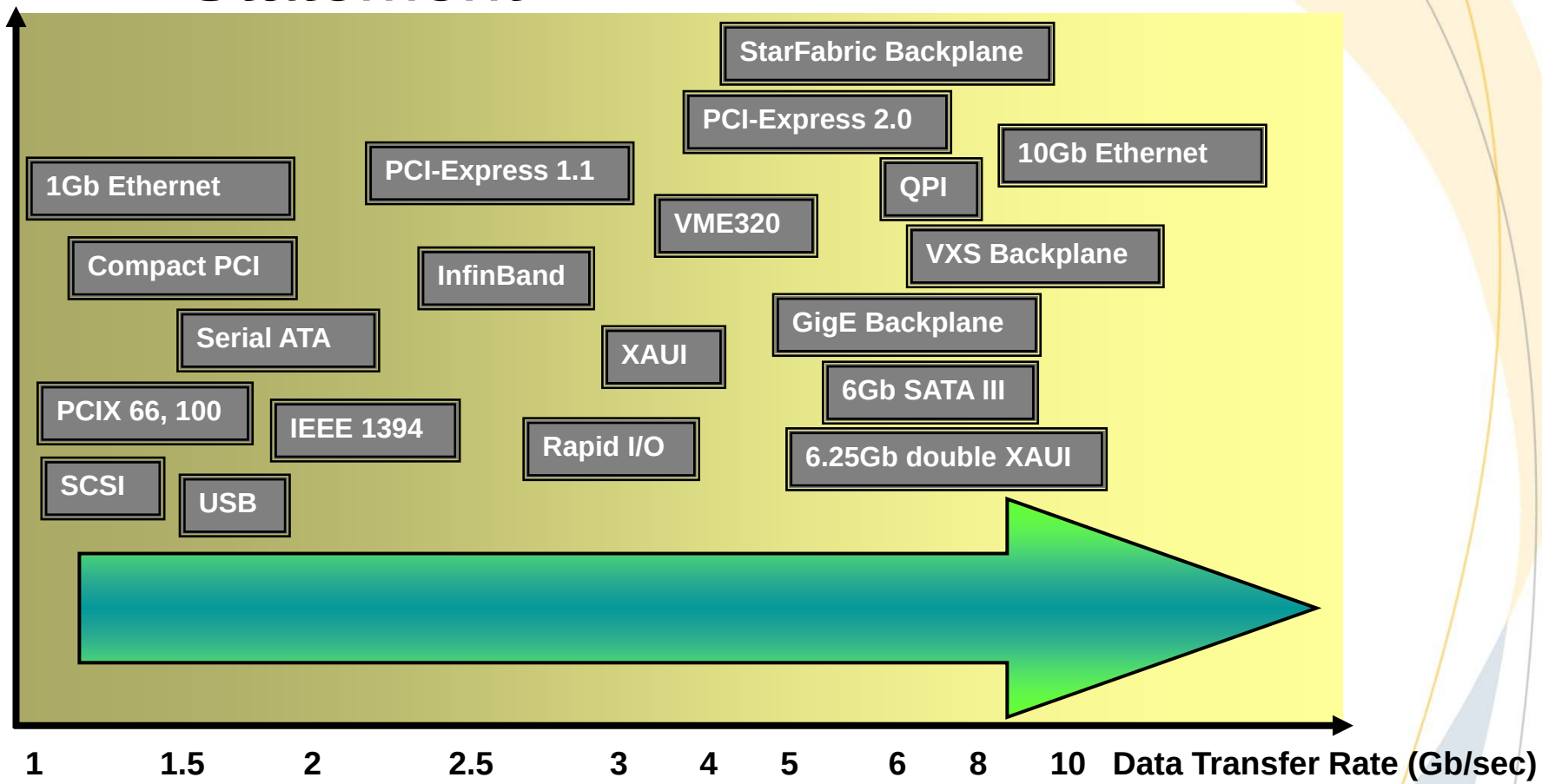
2009 Apex Expo

Outline

- Technology Trends and Associated Problems
- Proposed Solution with Virtual Electrical Access
- Time Domain and Frequency Domain Techniques
- Examples of Test Results
- Technique Limitations
- Summary

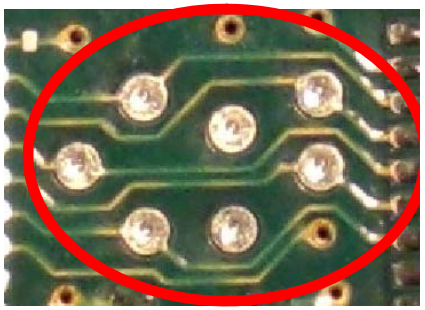
Technology Trends and Problem Statement

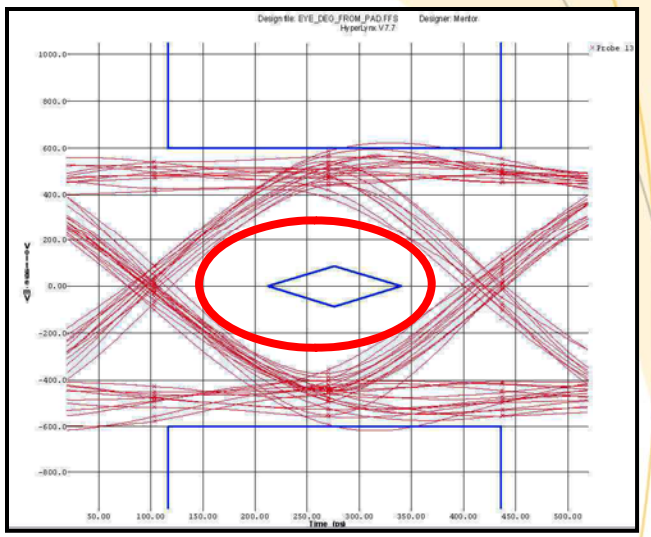


- Signal speeds are continually increasing and many can no longer tolerate conventional test pad access
- Alternative test methods need to be developed to regain test access

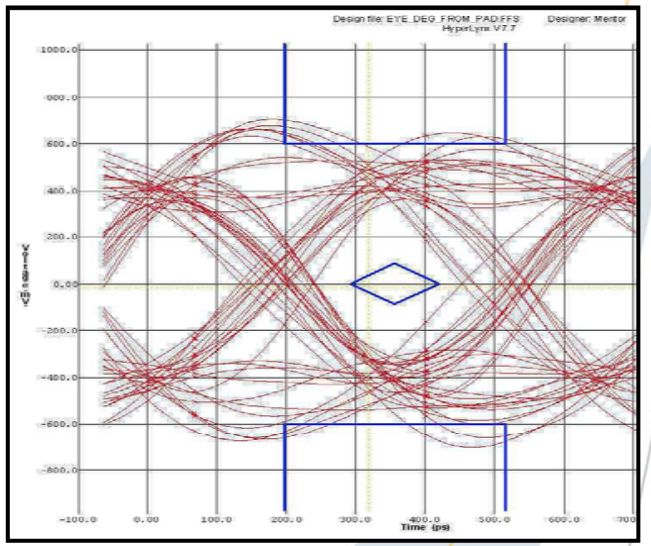
Gigabit Signaling and Test Pads

- Many designers are no longer allowing conventional ICT test pads on high speed signals
- Alternative test access for these signals is still required for manufacturing yields
- Restore defect coverage by supplying ***virtual*** access to these signals via boundary scan structures





Without Test Pads

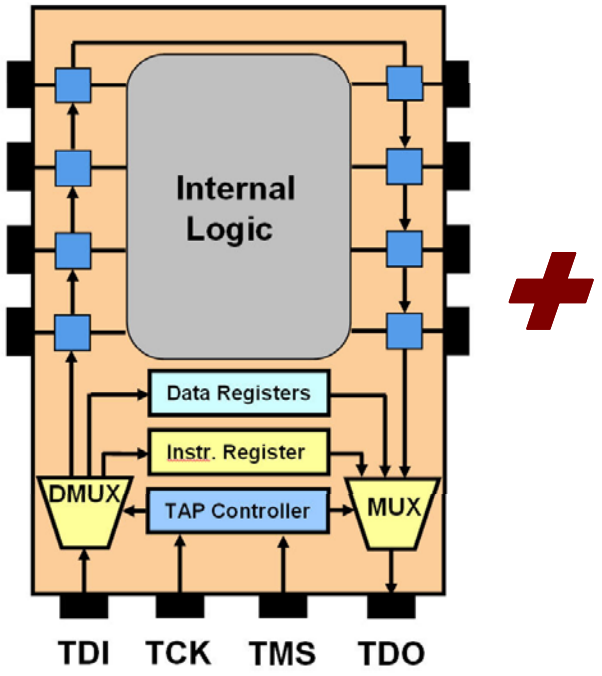


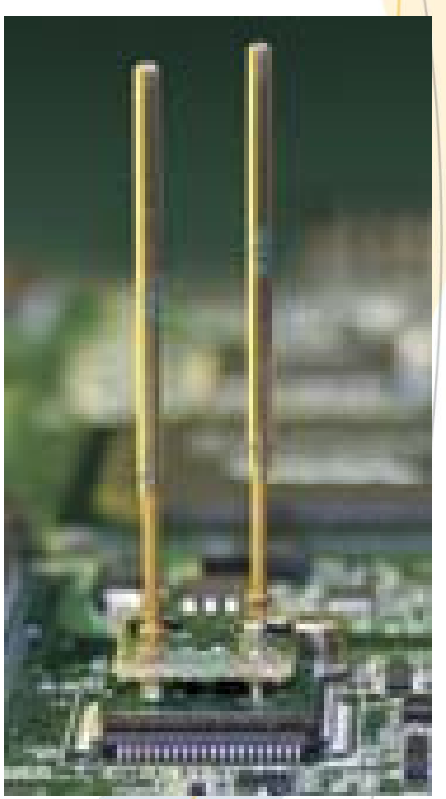
With Test Pads

Eye Diagrams courtesy of Mentor Graphics

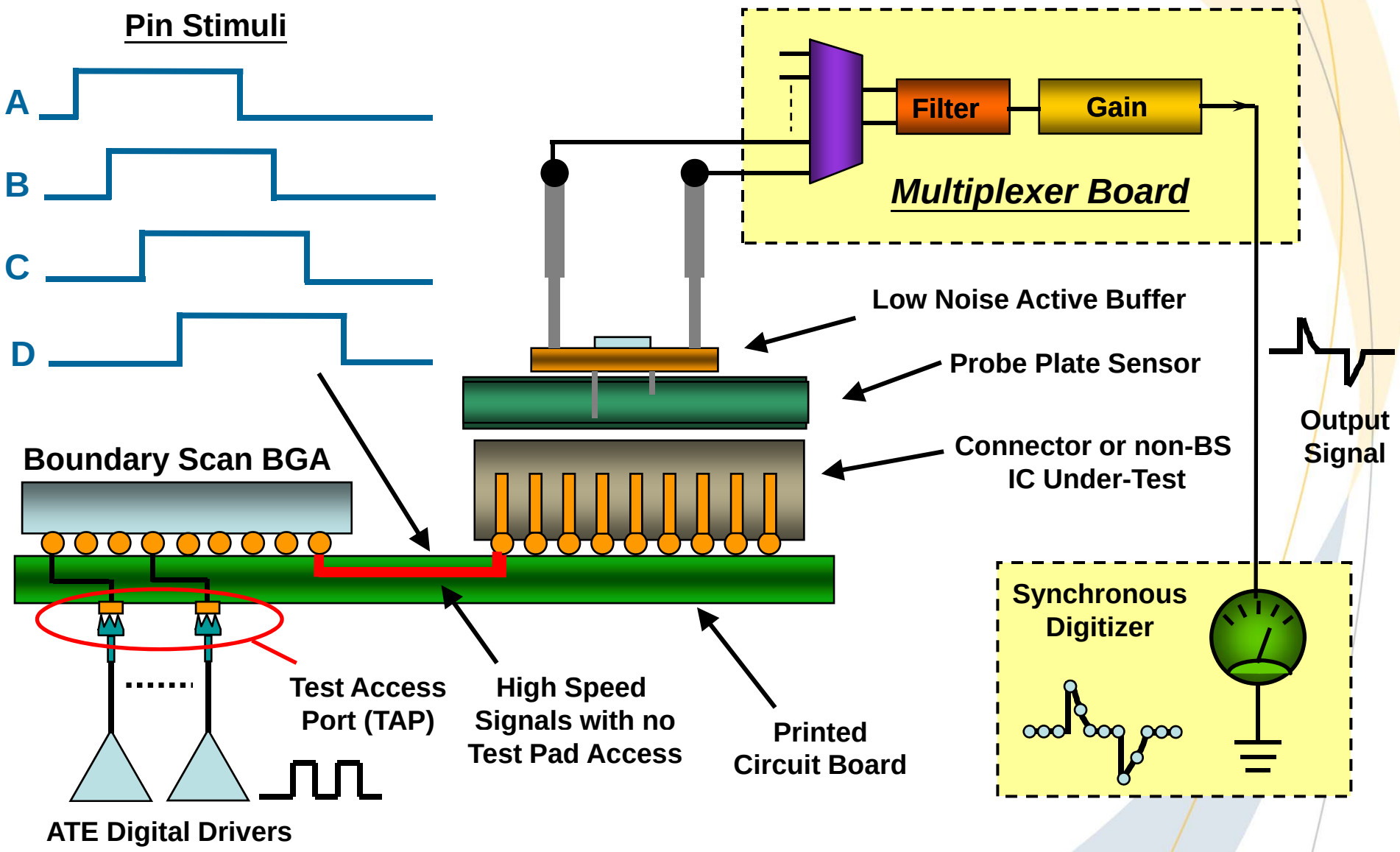
Proposed Solution to Access Issue

- Combines boundary scan and vectorless techniques
- Use Boundary scan devices as digital stimulus
- Signal detection uses capacitive based vectorless technology (FrameScan FX™)
- Identifies opens on connectors, sockets and IC devices
- Retains testability on high speed signals

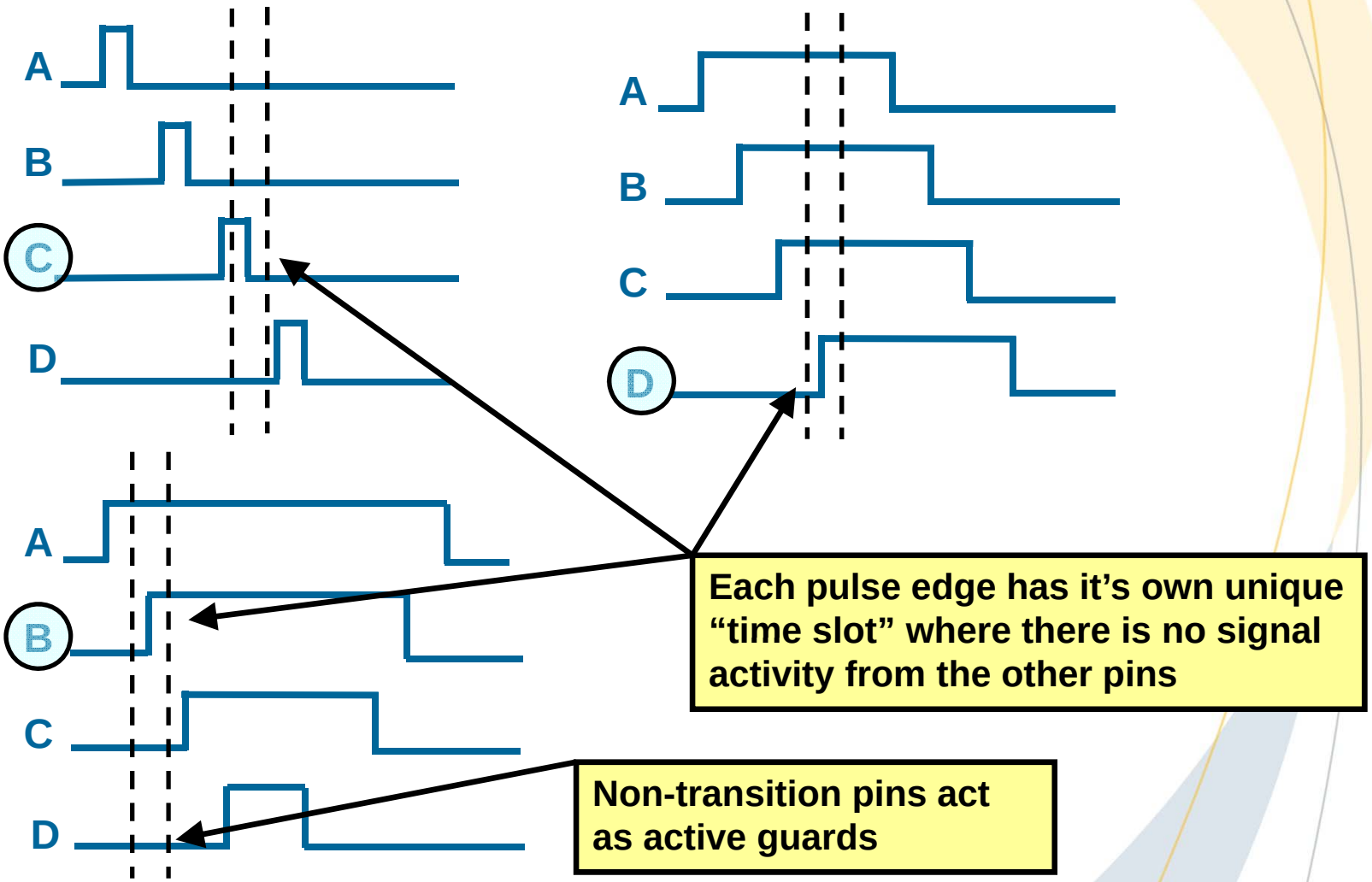




Boundary Scan and Capacitive Opens Techniques (Powered Opens)

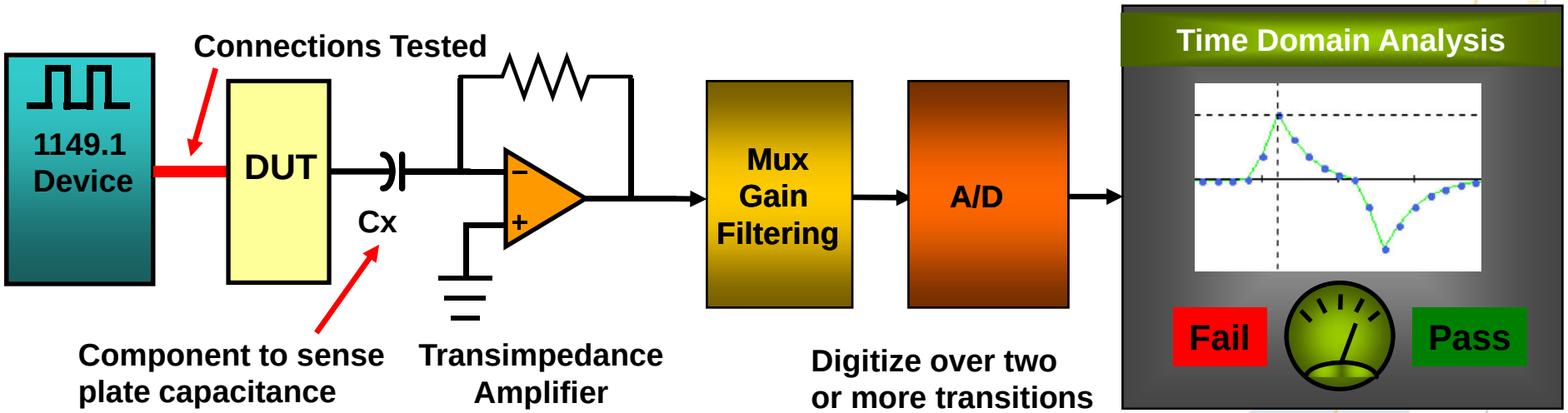


Examples of Pin Signal Patterns



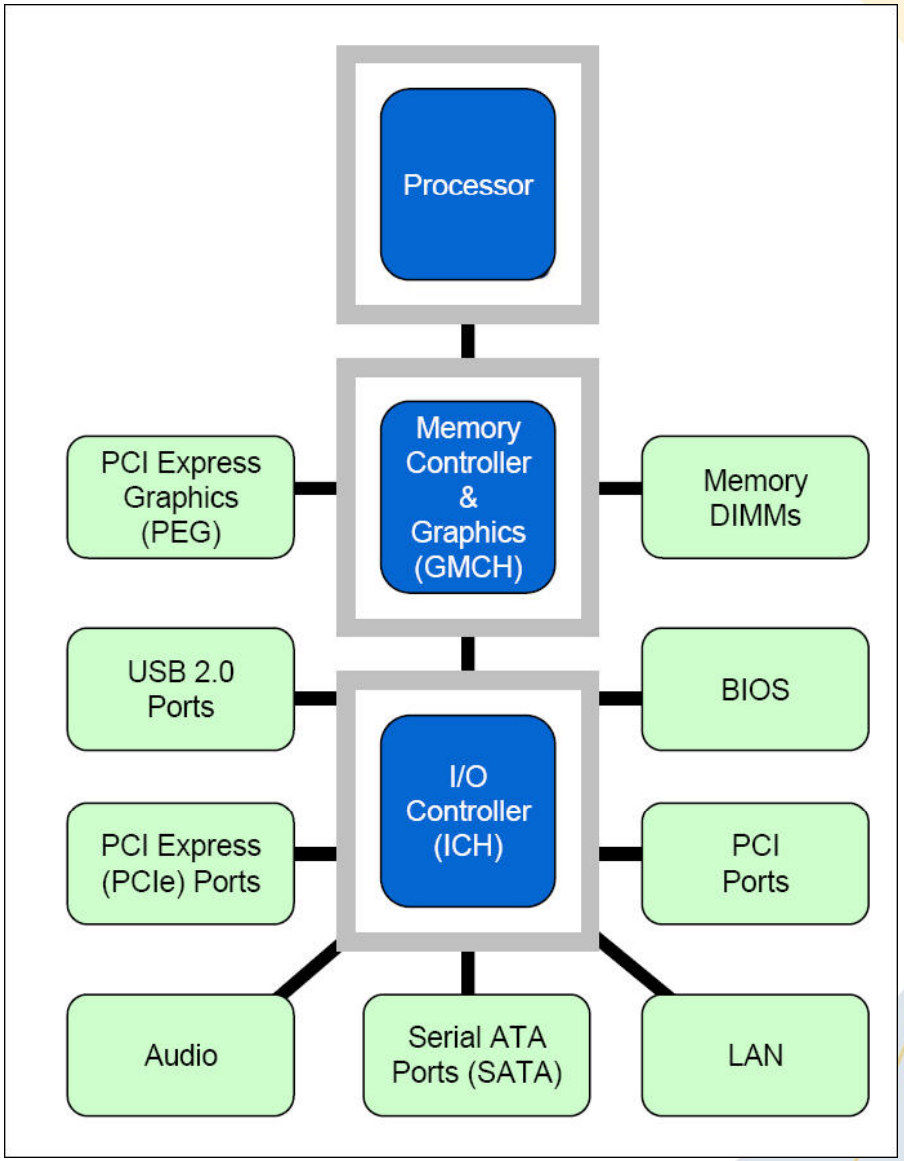
Selected Signal Analysis Method

- Time domain analysis
  - Apply two or more signal edge transitions to device under test
  - Digitize response waveforms from edge transitions
  - Process response signal using correlation techniques to eliminate the effects of both random and synchronous noise on the measurement
  - Compare results against predetermined limits
  - Determine pin connectivity, or open based upon test limits



Powered Opens Advantages

- PC Motherboard example:
- Most boundary scan devices are affixed to empty connectors
- Coverage can be attained by using powered opens technique



Why Time Domain Analysis?

- Conventional opens techniques using frequency domain analysis require a test frequency of about 10KHz
  - Frequencies below this range result in a loss of coverage because of a small measured signal
  - Frequencies above this range can cause board coupling effects and can cause false passes or accepts
- The boundary scan output pin frequency is approximately equal to the (TCK / 2) / (number of scan cells in chain)
- The boundary scan clock (TCK) on in-circuit testers is typically limited to 1-2 MHz
- Many of today's boundary scan devices containing hundreds of scan cells, so cannot generate the desired output clock frequency for test
- Large cell devices may become un-testable with frequency domain technique

Time Domain / Edge Detection Method

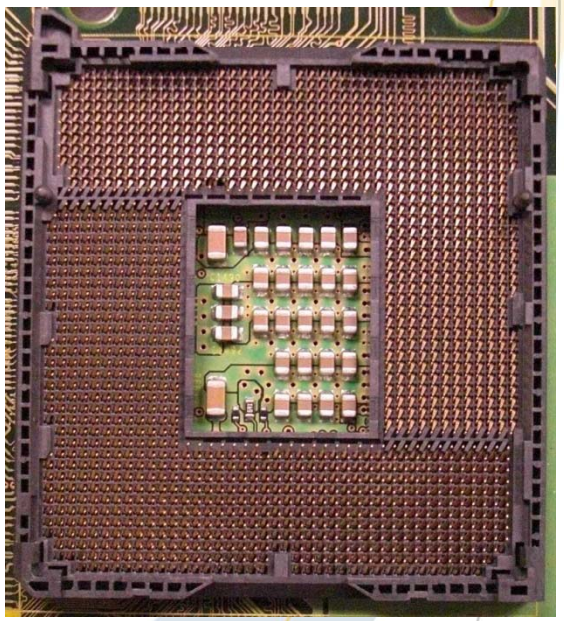
- Benefits
  - No dependence upon output toggle frequency when analyzing edges with autocorrelation and cross-correlation signal processing methods

$$r(d) = \frac{\sum_i [\,(x(i) - mx) * (y(i-d) - my)\,]}{\sqrt{\sum_i (x(i) - mx)^2}\sqrt{\sum_i (y(i-d) - my)^2}}$$

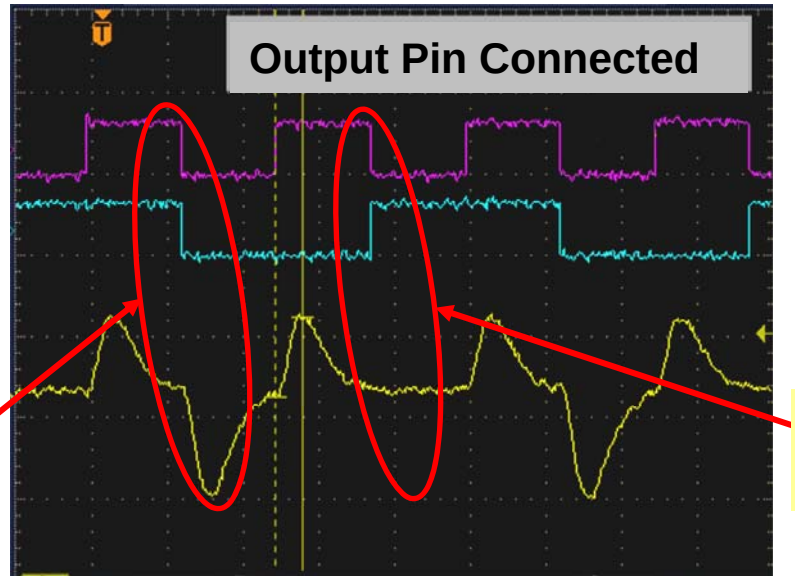
  - No restrictions with the number of scan cells in boundary scan chain
  - Technique operates with today's existing silicon, no need for boundary scan devices to support custom or private instructions
- Challenges
  - Time domain technique with edge recognition is inherently more complex to implement with a much larger software investment
  - Requires tight synchronization between tester's analog and digital subsystems that may not exist on all test platforms
  - On-board activity can generate noise that requires multi-level inhibit and disable software to quiet board

Issues with Boundary Scan Clock Interference

- IC sockets that are tested can contain the boundary scan clock (TCK) that must be active
- The signal seen by the capacitive probe plate will be the sum of the tested pin signal and the TCK
- This interference can be common and must be managed for a robust test solution
- Time domain algorithms using autocorrelation and cross-correlation techniques are robust in rejecting the boundary scan clock signal

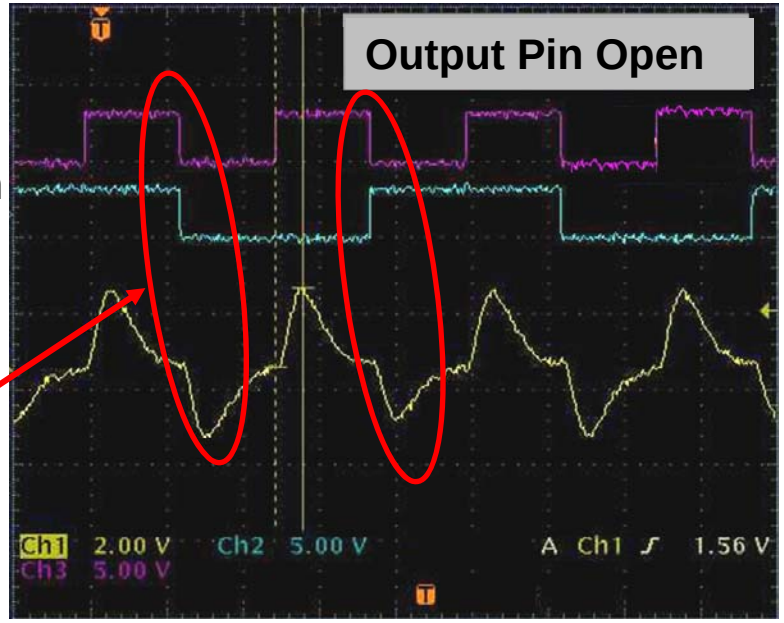


Example of Pin Response with TCK Interference



TCK and pin add in the resultant signal

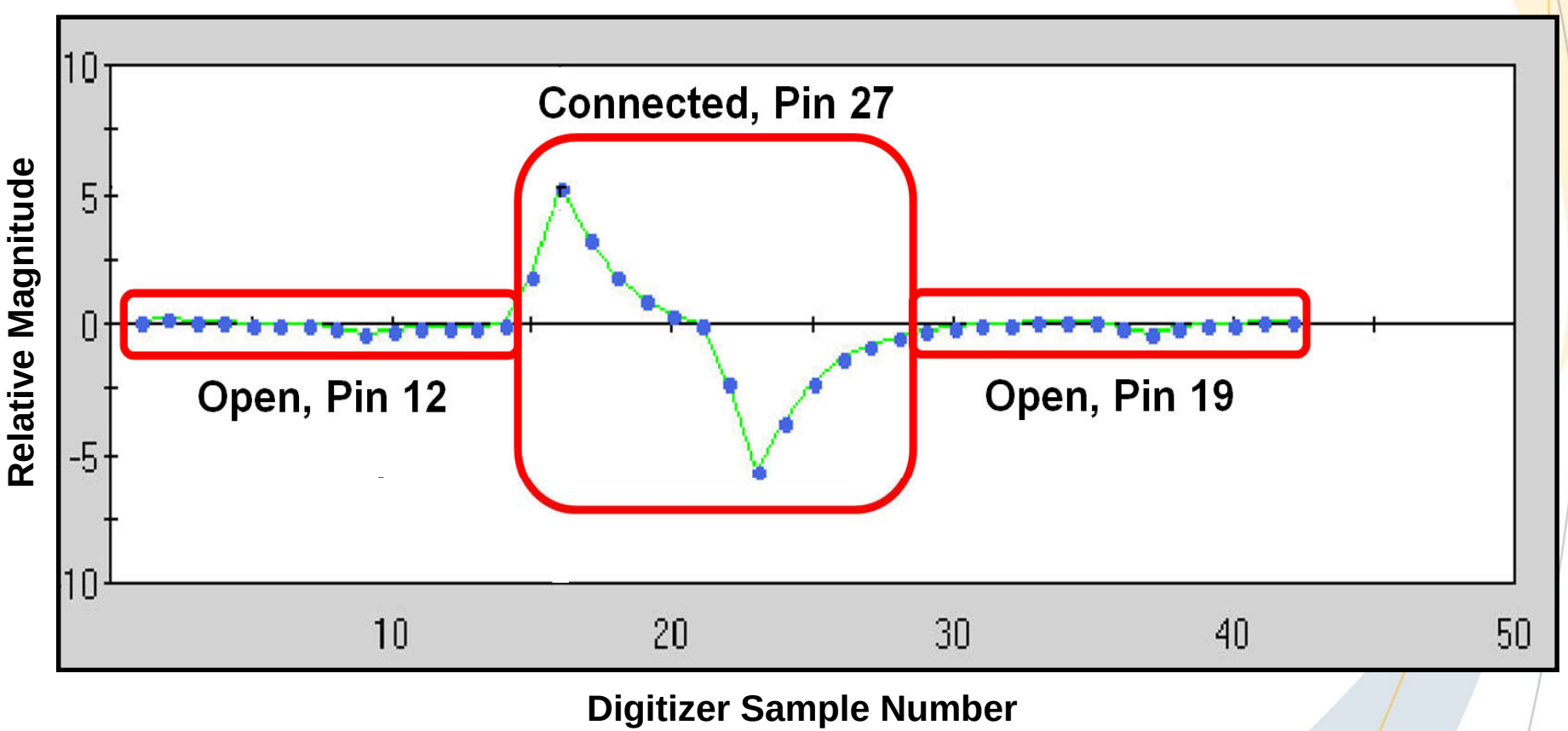
TCK and pin subtract in the resultant signal



TCK dominates the resultant signal but small influence from open pin

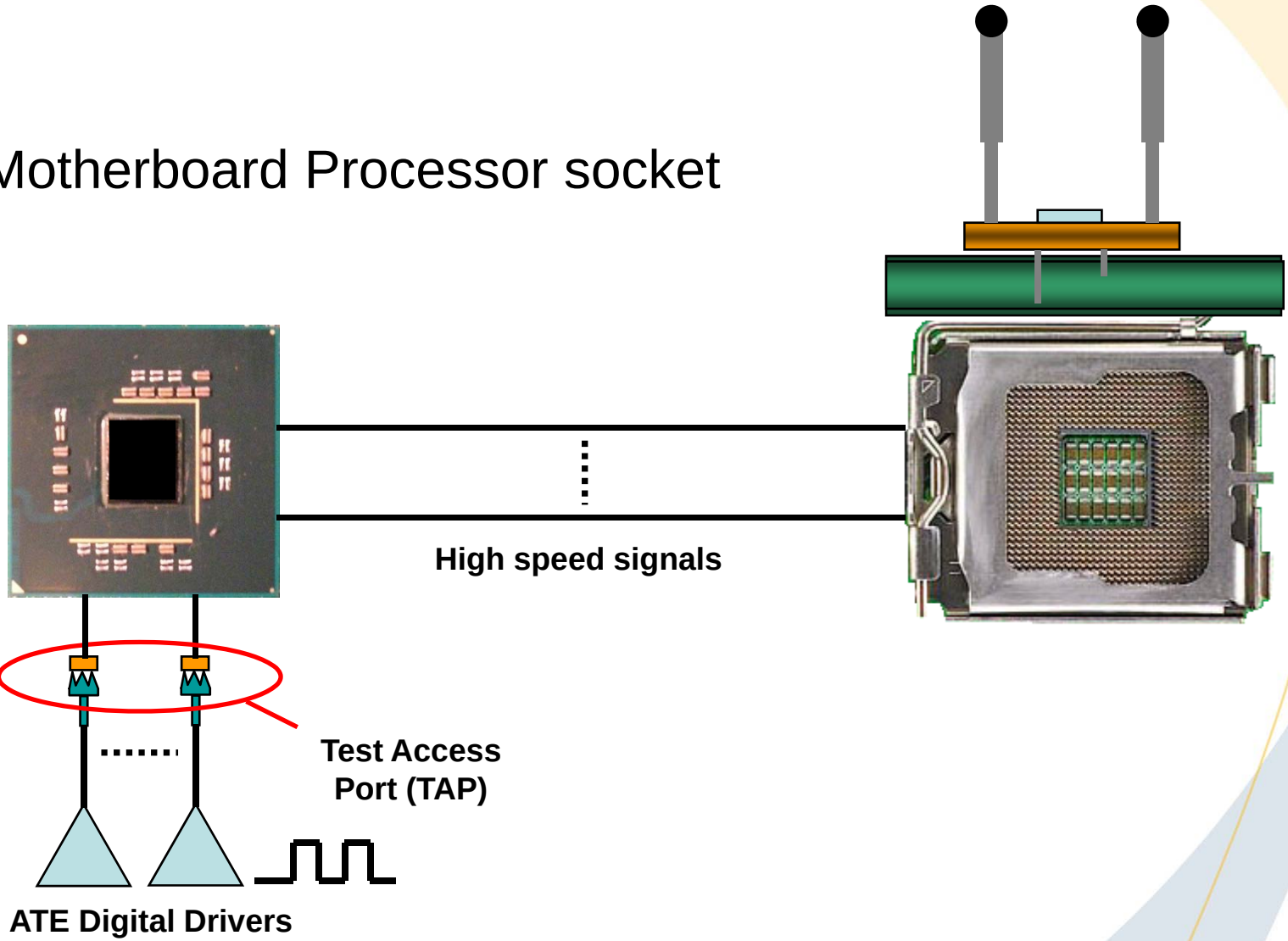
Powered Opens Signals

- Amplitude difference between an open pin and a connected pin on a 20 mil pitch SOIC.



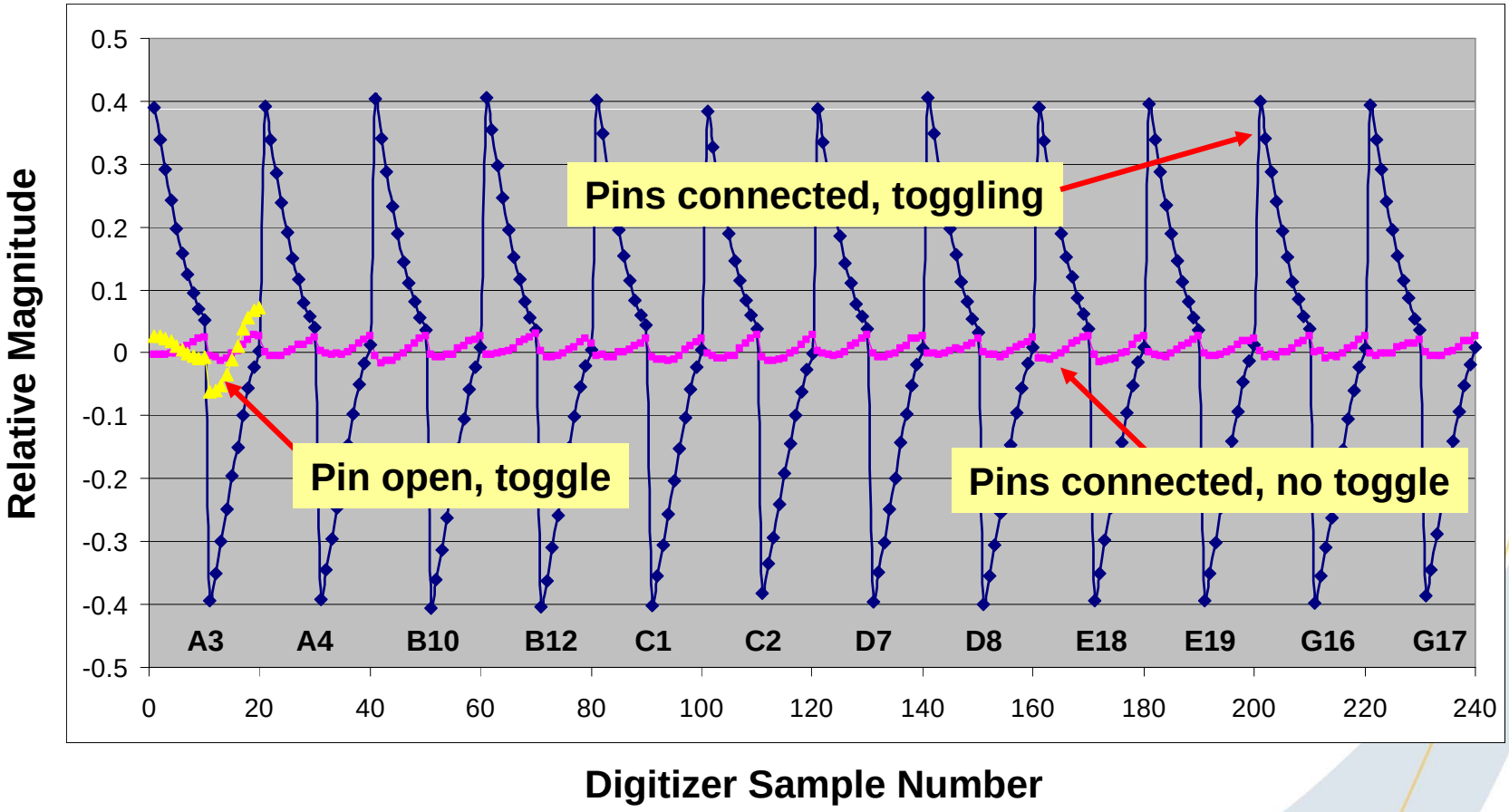
LGA 771 Socket Test Case

- Motherboard Processor socket

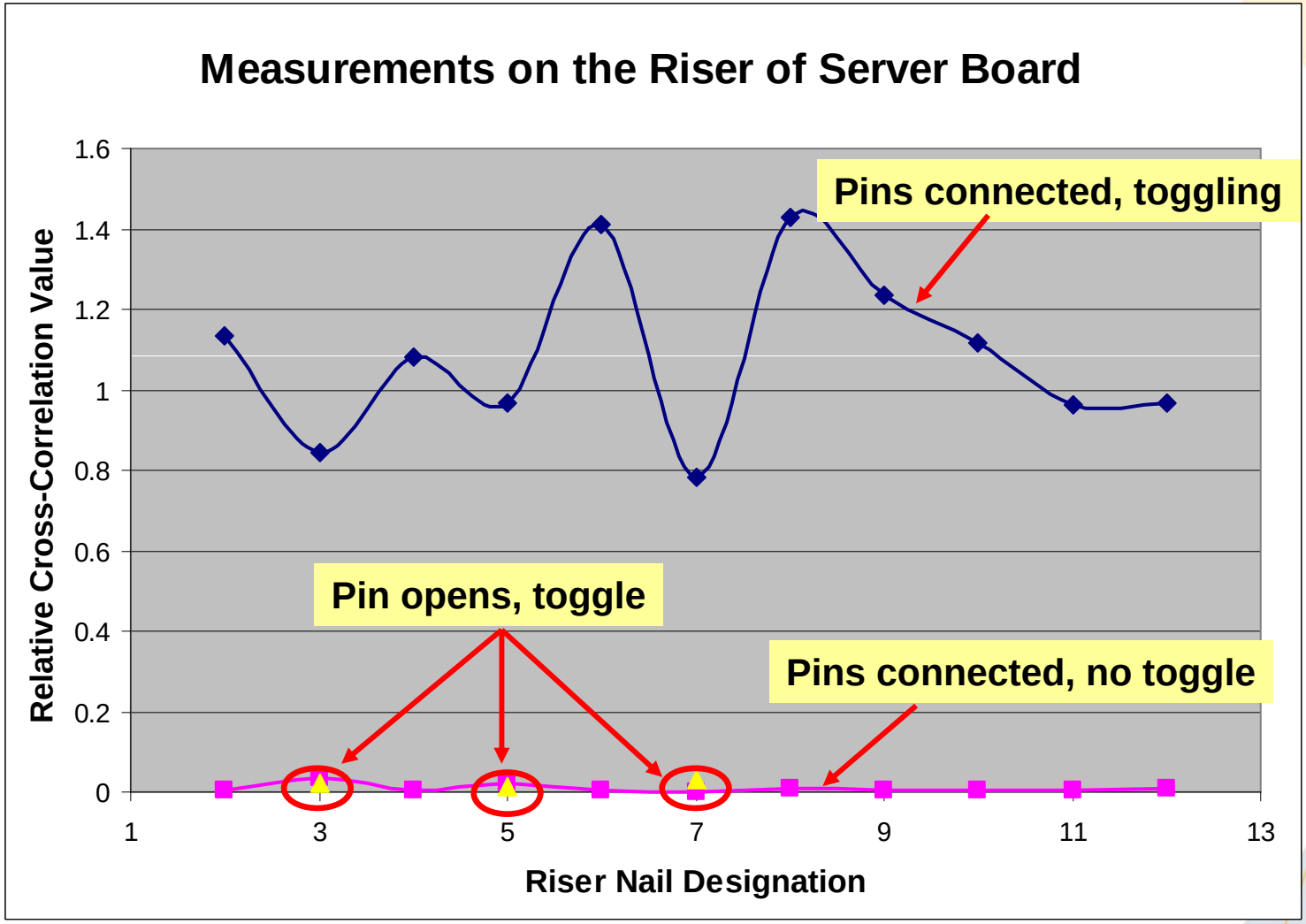


Measurements on LGA 771 Socket

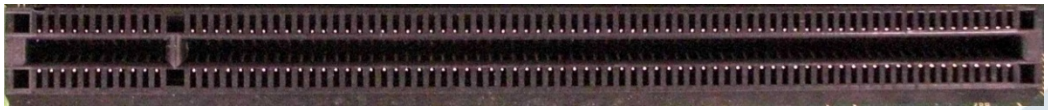
- Each positive and negative pulse pair represents a pin signal. Twelve connected pins are shown



Measurements on Riser Connector

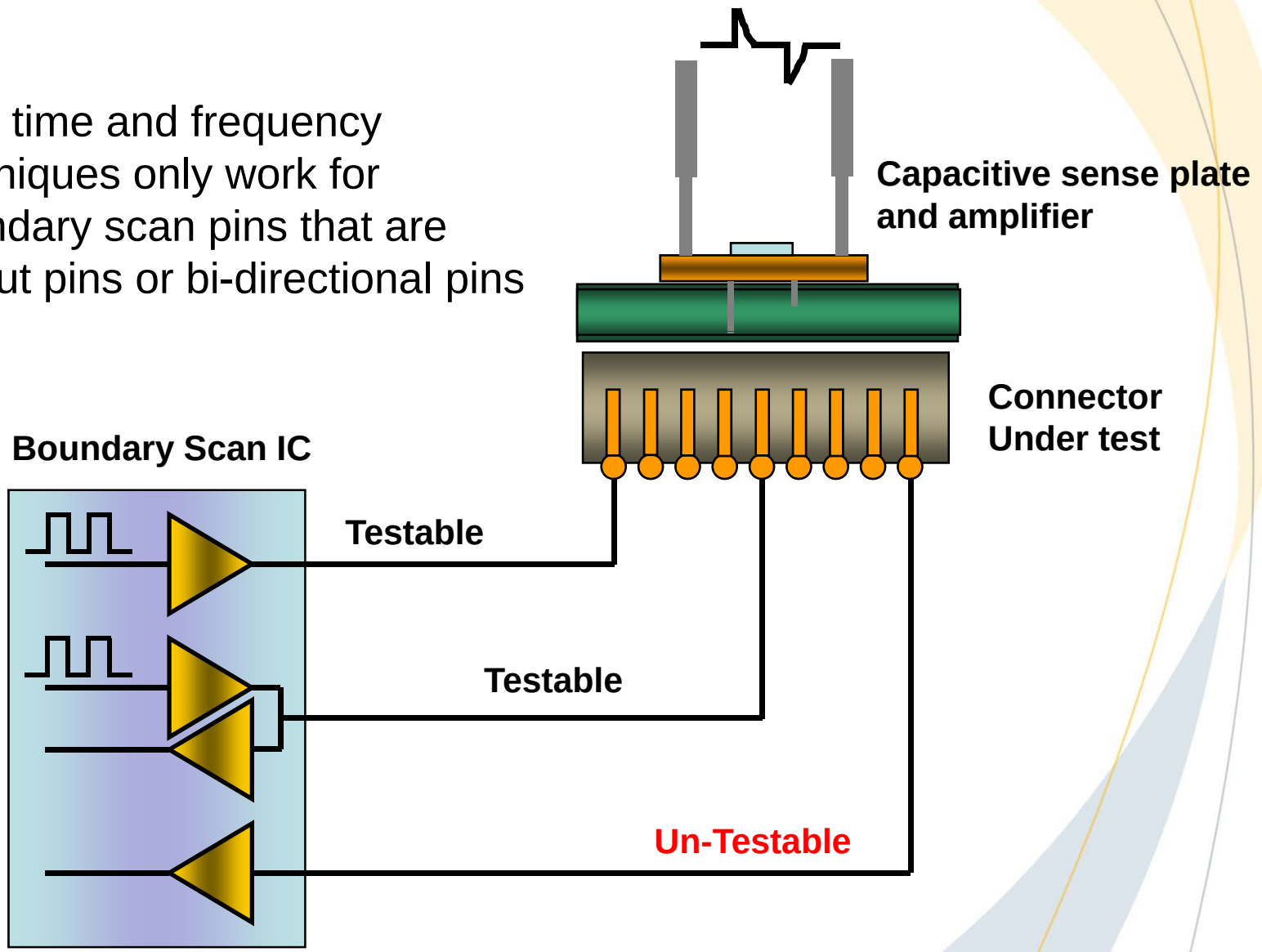


Connector



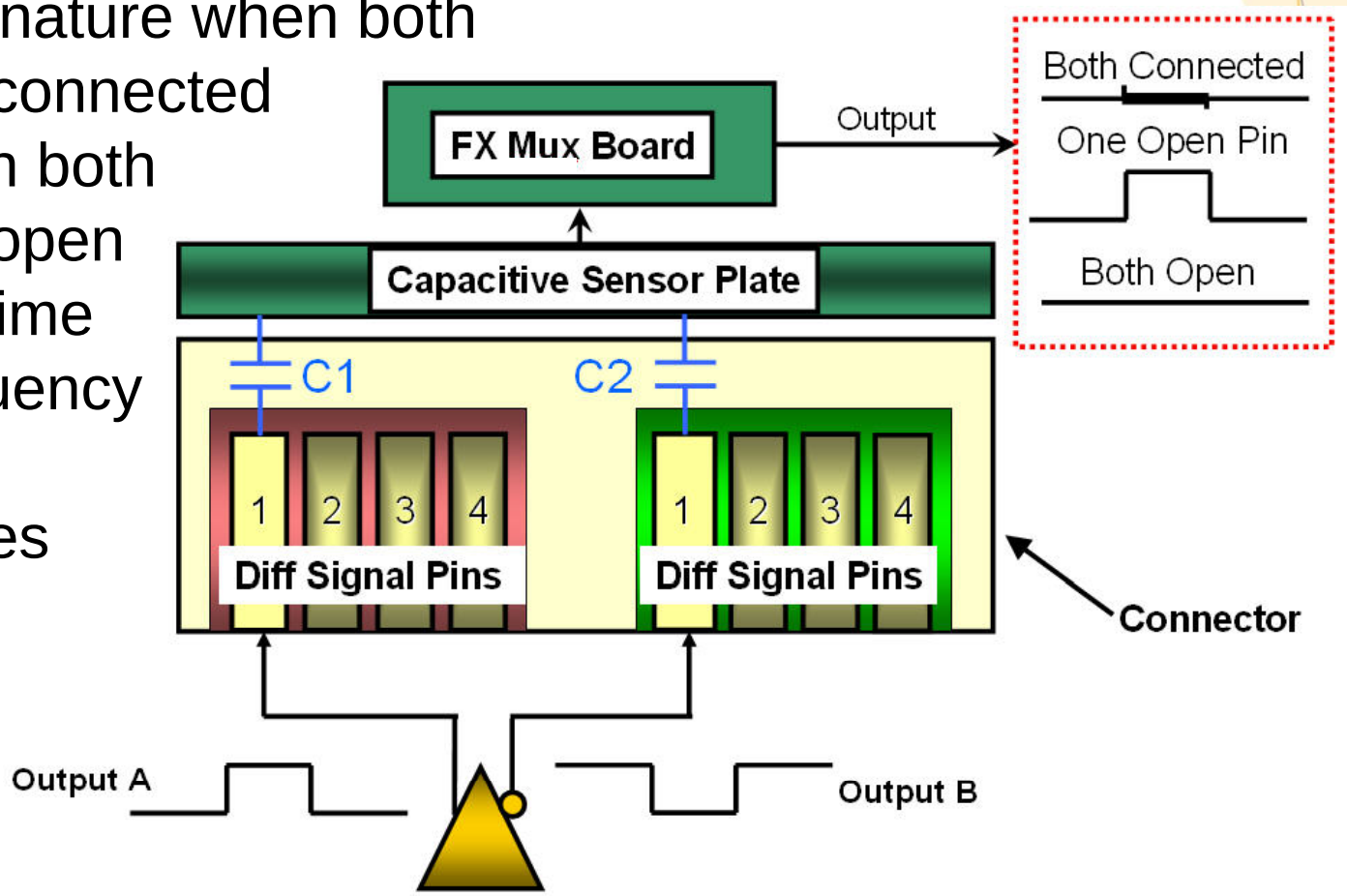
Technique Limitations

- Both time and frequency techniques only work for boundary scan pins that are output pins or bi-directional pins



Technique Limitations

- Differential signals have the same signature when both pins are connected and when both pins are open for both time and frequency domain techniques



Solving Technology Limitations

- Work is underway by a committee that proposes the enhancement of IEEE 1149.1 (IEEE P1149.8.1) by adding new stimulus capability to IC pins at the periphery of the IC, controlled by a new, optional test mode instruction. If adopted by IEEE and IC vendors, this change may then allow for frequency testing of large chains with a low frequency TAP clock
- This committee is working to find a solution to the differential signal cancellation issue
- The committee is also working on solutions to provide stimulus resources to boundary scan input pins
- For more information, visit:

http://grouper.ieee.org/groups/1149/atoggle/

Summary

- Many higher speed signals can no longer tolerate conventional test pad access for in-circuit testing
- A unique combination of boundary scan and capacitive opens techniques (Digital FrameScan™) afford virtual access alternative to high speed PCB nets and on boards with density issues
- Time domain technique is not sensitive to the boundary scan chain length and works with today's IEEE 1149.1 and 1149.6 boundary scan compliant IC devices

Questions

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