#### Understanding the Requirements of a Mass-Imaging Platform with Reference to the Impact of Interconnect Miniaturisation

#### Clive Ashmore Dek Printing Machines Weymouth, UK

#### Abstract

As the frontiers of feature size and interspace between devices become ever challenging, we as an industry have to start revaluating the performance of the toolsets that are used in the SMT arena. The days have gone where a tolerance of tens of microns was acceptable; this has now moved into the sub 10-micron domain. This issue is none more critical than within the print process, it is this pre placement tool-set that is most sensitive to the miniaturisation program running through the industry.

When we take a step back and reflect on what is required from a printing process at this new level of miniaturisation, we can quickly understand that the solder paste volumes required are crossing into semicon territory. Indeed it is clearly possible to count the solder particles that makes up a 0.3mm C.S.P deposit, the scale is so small. It is therefore paramount the composition of this pre placement tool-set is fully realised.

It is the intention of this paper to break down the elements of a print platform into its major mechanical and process subsections. Within the mechanical section, the elements investigated will be co planarity of rail systems and tooling nest; whereas with the process section the elements investigated will be the composition of the squeegee assembly. Each element will be fully explored using analytical methods to comprehend the cause and effects. The separate modules will then be combined to enable an aggregate picture of the process and thus allow a conclusion of which component parts are the most critical and to what level of accuracy is required for the SMT challenges ahead.

#### **Experimental process**

For each experiment the following set-up was conducted; the solder paste used was a type 4 Pb free commercially available material, the solder paste was refrigerated between each run and allowed to stabilise to room temperature before use, the material was replaced after 5 refrigeration cycles.

The stencil used throughout the investigation was a 100-micron stainless steel laser cut mesh mounted foil, the aperture dimensions and metal thickness were measured and it was these values that have been used to calculate the process capability.

The 10 substrates used were pre-numbered and run in order; the board design followed the Dek08 pattern and was fabricated from 1mm FR4. The components to be focused upon during this investigation will be the 0.4mm QFP's and CSP, as can be seen from Figure 1, the 0.4mm QFP appears in opposite corners of the substrate, this feature will be used to understand if the deposition process is symmetrical. The 0.4mm CSP represents the smallest and therefore most challenging device; this will be used to understand the deposition capability.

The solder paste was measured using a Cyber Optics SE300 inspection machine; the machine was calibrated before the investigation and was subject to a satisfactory gage R&R.

The process set-up was reset to the same level before each experiment, the stencil was cleaned using an automatic ultrasonic Sabermax stencil cleaner, the solder paste was loaded on the front of the image and the squeegee pressure mechanism was calibrated.

This investigation was split into two areas of research, transformed process elements and simulated interspace of the print process.

The print platform was checked against the manufactures calibration and build specification after each experiment thus only the forced change was affecting the response.



Figure 1: Image of test substrate

#### Transformed process elements module

The process elements that were adjusted for this investigation were squeegee angle and blade material. The motive for exploring the angle was attributable to the fact that the manufactured attack angle is instantaneity changed with the inclusion of pressure; this phenomenon is illustrated in Figure2



Figure2: Illustration of the effect of attack angle with respect to pressure.

Since the attack angle is a well documented variable within the print process, the approach of this investigation was to fabricate a variable angle squeegee assembly; such that the attack angle could be independently set, Figure 3 shows an illustration of this assembly. The outcome of this work was to understand if a specific angle gave an increase in deposition capability.





Figure3: Drawing of the adjustable squeegee assembly

Under the following conditions; 200-micron thick stainless steel squeegee blade, 15mm overhang, length of 200 mm and 5 Kg of pressure, the average deflection of the squeegee blade was measured to be 8 degs. It was therefore decided that a range between 35 and 60 deg would give ample resolution for this investigation.

The finish of the squeegee blade was also investigated and it was felt that the interface between the solder paste and the metal face of the blade would contribute to the print process. It was decided that the finishes that would be investigated would include the standard stainless steel blade, a stainless steel tetra carbon coated blade and a chromium-coated blade. The purpose of the coating was to introduce a reduction of surface tension and therefore reduce the, "stick-scion" between solder paste and squeegee blade.

#### Simulated interspace module

The simulated interspace elements that were adjusted within this investigation covered the co planarity of the following interfaces; stencil, substrate and tooling.

The motive for including these elements into this investigation were attributed to the fact that within a print process three individual components are interfaced during the print stroke, these been the tooling, board and stencil, if a process is set-up incorrectly it is possible to create interspaces at these interfaces, Figure 4 illustrates this principle.



Figure 4: Diagram showing the possible interspace conditions within a print process. a) correct set-up, b) interspace created between substrate and stencil c) interspace between tooling and substrate

To fully understand the importance of these individual elements and their impact on the print process a set of experiments were set-up to identify the impact.

The first experiment conducted isolated the impact that the co planarity of the substrate to stencil had on the print process. To achieve this objective the following techniques were used; the rail system was systematically deformed using a shimming material, this gave the ability to "dial in" a predetermined amount of deformation and therefore adjust the substrate to stencil co planarity, the overall effect of this would be to produce a varying amount of interspace between the top of the substrate and bottom of the stencil.

The second experiment within this interspace module was to investigate the effect of creating an interspace between the tooling and substrate; figure 5 outlines the test strategy.

#### **Breakdown of Experiments**



Figure 5: Break down of experiments

#### Results

The method of contrasting and comparing the results from the separate experiments was carried out by statistical analysis (Minitab) and surface profiles of individual solder paste deposits. This approach allows for both quantitative and qualitative to be used in the analysis, this was felt important as the market both demands a perfect looking print (sharp definition, flat top etc..) and the statistics to prove that the process is also stable and capable.

The limit sets used to calculate the Cp and Cpk values are shown in Table1, the stencil measurements were used to calculate the theoretical volume; the transfer efficiency and tolerance were derived from previous assembly investigations.

	Table1: Limit sets								
				Theoretical	Transfer		Normalised		
Device	Width/diameter	Length	Thickness	Nominal	Efficiency	Tolerance %	Nominal	USL	LSL
0.4 QFP	230	1524	100	35052000	75%	40	26289000	36804600	15773400
0.4 CSP	230	-	100	4154756	70%	40	2908329	4071661	1744998

The results of this investigation are shown below; each experiment has the statistics and associated charts followed by the surface profiles of the solder paste deposits (for reporting purposes board 5 is only shown)

#### Transformed process elements module

#### **Experiment 1**

-	1					
Experiment			0.4mm QFP 1	0.4mm QFP 1	0.4mm QFP 2	0.4mm QFP 2
Name	0.4mm CSP Cp	0.4mm CSP Cpk	Ср	Cpk	Ср	Cpk
35- 40 deg sqa	0.615	0.499	1.103	0.827	1.262	0.682
45- 50 deg sqa	1.393	1.133	1.03	0.995	1.033	0.98
55 -60 deg sqa	1.45	1.052	1.056	0.956	1.122	1.07

#### Table 2: Statistics data from experiment 1



#### Table 3: Process capability charts from experiment 1



**Experiment** 2

#### Table 5: Statistics data from experiment 2

Experiment			0.4mm QFP 1	0.4mm QFP 1	0.4mm QFP 2	0.4mm QFP 2
Name	0.4mm CSP Cp	0.4mm CSP Cpk	Ср	Cpk	Ср	Cpk
SS-TC	0.894	0.889	0.98	0.848	1.105	0.933
Chrome	1.392	1.288	1.076	0.996	1.114	1.097

#### Table 6: Process capability charts from experiment 2





Chart showing the process capability - Transformed process elements module



Figure 6: Chart showing transformed process elements (experiments 1&2)

#### **Simulated Interspace Module**

**Experiment 3** 

				· •		
Experiment			0.4mm QFP 1	0.4mm QFP 1	0.4mm QFP 2	0.4mm QFP 2
Name	0.4mm CSP Cp	0.4mm CSP Cpk	Ср	Cpk	Ср	Cpk
Substrate to						
stencil						
interspace 300						
microns	0.73	0.054	1.319	1.019	1.165	0.895
Substrate to						
stencil						
interspace 200						
microns	0.65	0.39	2.627	1.356	1.219	0.946
Substrate to						
stencil						
interspace <100						
microns	1.525	1.506	1.318	1.311	1.304	1.296

#### Table 8: Statistics data from experiment 3



#### Table 9: Process capability charts from experiment 3



#### Table 10: Surface profile from experiment 3

#### **Experiment** 4

#### Table 11: Statistics data from experiment 4

Experiment Name	0.4mm CSP Cp			0.4mm QFP 1 Cpk	0.4mm QFP 2 Cp	0.4mm QFP 2 Cpk
Negative tooling			-		F	
gap	0.781	0.163	1.443	0.813	1.148	0.765



#### Table 12: Process capability charts from experiment 4

#### Table 13: Surface profile from experiment 4



#### Chart showing the process capability - Simulated Interspace Module



Figure 7: Chart showing simulated interspace (experiments 3&4)

#### Conclusion

Before comparing and contrasting these results it is worth reflecting on these two general observations: -

- For most process engineers, the print process is the first process to be set-up and the last process to be questioned when thing go wrong.
- Within this industry it is a well-known fact that over 60% of all defects are attributed to the print process.

So why do engineers tend to over look the print process? And why does the print process provide the majority of defects? This paper has been conducted to answer these questions.

The first module focused upon the transformed process elements; within this section the squeegee attack angle and squeegee blade material were chosen as the transformed factors.

It can be observed from Table 1 and 2 that the outcome of changing the squeegee angle affects the process capability, increasing the squeegee angle from 35-40deg to 55-60 deg causes the deposited volumes closer to the nominal volume and increases the process repeatability, where as decreasing the squeegee angle increases the volume deposit and reduces the process repeatability.

To better understand why this occurs we need to consider what is happening at the tip of the squeegee; as the blade traverses over an open aperture the solder paste material, under hydrodynamic pressure is forced into the opening. If the transfer force is too high the solder paste material will start to compress and force itself under the blade and creates a "wake". It is this compression and wake effect that creates the high volume and reduced process capability.

This "wake" effect is most notable when observing the QFP results in table 2, with the blade set at a low angle the charts display a duel peaked curve, after further analysis this bi modal effect represented the split between North-South and East-West deposits.

Analysing the difference between these two aperture orientations it is clear to see that the amount of time that the squeegee blade has to fill the North-South apertures (300 ms) is considerably longer than the East-West (46 ms), it is therefore possible that the high transfer force associated with the longer fill time of the North-South apertures creates a greater opportunity for the "wake" effect to take place and therefore higher volumes and reduced process capability proceeds; where as the East – West apertures have less fill time and therefore are not subject to the "wake" issues.

The surface profiles shown in table 4 also coincide with the observations discussed above; the deposits to deposit consistency increases and the QFP deposits become more "brick" shaped when the squeegee angle is increased from 35-40deg to 55-60 deg.

The second experiment within this transformed process section was to understand the influence of the impact that the squeegee blade material has upon the resultant print process. The two material chosen were Tetra carbon and Chromium, both surface finishes are recognized for their friction reducing properties.

From the results shown in table 5 it is clear to see that the Chromium finished blade is the clear winner from this "bake off", the chromium blade especially performs well when imaging the 0.4mm CSP device. This would indicate that the property of the chromium coating positively influences the interface of solder paste to squeegee blade and consequently improves the filling of small apertures.

The results from the surface profile (Table 7) interestingly show a slightly different picture, the profiles from both tests show very little difference in print quality both look acceptable. It is by analysing this scenario that we can start to understand why a print process could be over looked when fault finding an end of line yield issue. Taking this example into a real life situation, the engineer would look at the profiles from the Tetra carbon results and almost certainly sign off the process as acceptable but the data is otherwise indicating a different story, it is understandable how a print process could be wrongly diagnosed without a full examination.

The results illustrated in Chart 6 overlay all the results from the transformed process module, it is clear to see that a 55-60 deg squeegee coated in chromium gives the best overall results.

The second module focused upon the influence of simulated interspaces within the print process; within this section the effect of interspace relating to the stencil to substrate and tooling to substrate were investigated.

The results from Table 8 and 9 illustrate the relationship between increasing the interspace between the stencil and substrate and print quality. It can be seen that the statistics indicate that as the interspace is reduced the process indices increase thus signifying greater process control, the surface profiles shown in table 10 also confirms this theory.

Investigating further into the charts shown in Table 9 provides a clear understanding as to why this phenomenon occurs. It can be seen from the 0.4mm CSP (300 microns and 200 microns) distribution chart two distinctive peaks are visible; unlike the QFP device, the CSP is not asymmetric, therefore this twin peaks effect is not related to the fill process but more likely associated with the release process.

To better understand how this effect could cause poor print quality we need to consider that during the moment of aperture fill the squeegee is pushing (gasketing) the stencil onto the substrate, as the squeegee moves away from the aperture the stencil will start to peal away from the substrate thus causing a "false separation" step. It is during this "false separation" step that the material inside the filled apertures will be subjected to interference and depending upon the amount of stencil peel and friction of solder paste to its interfaces, will depend how "fractured" the solder paste will become inside each independent aperture. This effect is most striking when evaluating the surface profiles from Table 10, it can be seen that the print deposits of the 0.4mm CSP exhibit a "fractured" structure in which the deposits are varying in shape and volumetric quantities.

The reason why the <100 micron interspace results showed no detrimental effect can be explained by the principle that if the "stencil peel" does not exceed the solder paste deposit height then the solder paste within the aperture will not have been completely fractured and therefore will still follow the standard release method.

The results from this experiment conclude that if the interspace is greater then the stencil mask thickness the influence of the "false separation "will cause a detrimental print quality.

The second experiment in this module investigated the influence of including an interspace between the substrate and tooling assembly. The results from this experiment are shown in Tables 12 and 13. As can be seen from the statistical data, the addition of the interspace has decreased the print quality in both accuracy (Cp) and repeatability (Cpk). Analysing the surface profiles reveals a similar image as those of the stencil to board interspace results; thus it can concluded that this tooling to substrate interspace has also caused a "false separation" step within the print process.

The results illustrated in Chart 7 overlay all the results from the simulated interspace module, it is clear to see that any interspace reduces the process capability, this is especially apparent on the fine pitch CSP devices.

Throughout this investigation the following discoveries have been made:

- Squeegee angle significantly influences the print quality
- The squeegee material significantly influences the print quality
- Interspaces between the substrate and stencil greater then the print thickness significantly influences the print quality
- Interspaces between the tooling assembly and substrate greater then the print thickness significantly influences the print quality
- Quantitative and qualitative does not always concur

The final step of this paper is to address the questions posed at the start of this section: -

It has been seen that merely observing the print quality does not tell the whole story, the print could look acceptable but the capability of that process is questionable. This situation would lead an engineer to wrongly accept the process capability and thus overlook the print process.

We have also seen that very small changes have large impacts; the inclusion of an interspace within the print set-up has been highlighted as a major cause of variation. Within the real world of solder paste printing these interspaces can be introduced through incorrect substrate solder mask thickness and incorrectly manufactured tooling assemblies, etc. It is due to these influences that can cause the reported headline rate of 60% defect associated with the print process. It is therefore important that the engineer fully appreciates the sensitivity that these small "environmental" influences can have on the solder paste print process.

Understanding the requirements of a mass-imaging platform with reference to the impact of interconnect miniaturisation

**Clive Ashmore** 

Dek Printing Machines Weymouth, UK



### Abstract

- As the frontiers of feature size and interspace between devices become ever challenging, we as an industry have to start revaluating the performance of the toolsets that are used in the SMT arena
- When we take a step back and reflect on what is required from a printing process at this new level of miniaturisation, we can quickly understand that the solder paste volumes required are crossing into semicon territory.



### Abstract

 It is the intention of this presentation to understand what are the critical areas of a print platform set-up.



### **Experimental Conditions**

Parameter	Value & Unit
Print Speed	50mm/s
Print Pressure*	5Kg
Separation Speed	10mm
Separation Distance	3mm/s
Squeegee Angle	35 – 60 Deg
Tooling	Vacuum tooling block
Temp & Humidity	21 Deg C & 40% R.H

\* 35-45 deg blades required higher pressure 8Kg



## Equipment Set

- Dek Galaxy Printer
- Commercially available Type 4 Pb free solder paste
- 100 micron laser cut stainless steel stencil
- Cyberoptics SE300
- Stereo Micropsope

All machines calibrated prior to experiments

### **Experimental Conditions**

- 3 "dummy" prints performed before each experiment.
- 10 pre numbered boards run in sequence for each set-up.
- DEK 08 Test board used.
- 0.4mm QFP and 0.4mm CSP used for investigation.

### Image of DEK 08





### **Breakdown of Experiments**

- Transformed Process Elements
  - Squeegee angle
  - Squeegee coating
- Simulated Interspace
  - Stencil to board interspace
  - Board to tooling interspace



### **Breakdown of Experiments**



IPC Printed Circuits Expo<sup>®</sup>, APEX<sup>®</sup> and the Designers Summit 2008

IPC

and the DESIGNERS SUMMIT

PEX

• Why squeegee angle ?



#### Objective – To understand which angle produces the most stable process



 Adjustable squeegee assembly





- Blade thickness 200 microns
- Blade overhang 15mm

- Blade length 200mm
- Tested angles 35 –60 deg

• Why squeegee coating ?



Objective – To understand the impact of squeegee coating on the process



- Squeegee coating
  - Tetra carbon
  - Chromium (Trivalent not Hexavalent)



### Simulated Interspace



a) On contact.

IPC

- b) Interspace created between substrate and stencil.
- c) Interspace between tooling and substrate.



### Results

#### • Limit Sets

				Theoretical	Transfer	Normalised		
Device	Width/diameter	Length	Thickness	Nominal	Efficiency	Nominal	USL	LSL
0.4 QFP	230	1524	100	35052000	75%	26289000	36804600	15773400
0.4 CSP	230	-	100	4154756	70%	2908329	4071661	1744998

Derived from previous work

#### • What will be reported

- Quantitative data Statistics
  - Cp (spread) and Cpk (accuracy)
- Qualitative data Observations
  - Surface profiles

### Results - squeegee angle

Large spread High volumes

Tight spread & accuracy

Tight spread & accuracy



Large spread Dual peaks (N-S/E-W)

Dual Peaks (N-S/E-W)

Tight spread & accuracy



### Results - squeegee angle



Reducing "dog ears"



Increasing consistency

### Results - squeegee coating @ 55 -60°



IPC Printed Circuits Expo<sup>®</sup>, APEX<sup>®</sup> and the Designers Summit 2008

APEX

and the DESIGNERS SUMMIT

### Results - squeegee coating @ 55 -60°





#### Results - squeegee summary

Chart showing the process capability - Transformed process elements module



IPC

### Results – forced interspace

Large spread Dual peaks

Large spread Dual peaks

Tight spread & accuracy



Large spread

Large spread

Tight spread & accuracy



### Results – forced interspace



Increasing consistency

IPC

and the DESIGNERS SUMMIT

APEX

IPC Printed Circuits Expo<sup>®</sup>, APEX<sup>®</sup> and the Designers Summit 2008

Reducing "dog ears"

# Results – Negative tooling interspace





# Results – Negative tooling interspace



PRINTED APEX CIRCUITS APEX and the DESIGNERS SUMMIT PC Printed Circuits Expo<sup>®</sup>, APEX<sup>®</sup> and the Designers Summit 2008

#### Results – interspace summary

Chart showing the process capability - Simulated Interspace Module





- Increasing the angle from 40-45° to 55-60° significantly increases the process capability
- 40-45° squeegee gives higher volumes but lower process capability



 The increased attack angle produces a "wake" effect







N/S 0.4mm QFP aperture Print speed @ 50mm/s Fill time = 300mS

E/W 0.4mm QFP aperture Print speed @ 50mm/s Fill time = 46mS

 At high attack angles N/S apertures tend to over fill w.r.t E/W = unbalanced process.

- So how does this effect my process ?
- An operator can adjust to attack angle with pressure
- Increasing the squeegee pressure (to mask set-up issues) will increase attack angle.



- The squeegee material significantly influences the print quality
  - Increased process capability observed from chromium coating



### **Conclusion - Interspace**

 Any interspace between stencil, substrate and tooling will cause poor process capability.



### **Conclusion - Interspace**

- So how does this effect my process ?
  - Debris on stencil, board or tooling will produce an interspace.
  - Poorly maintained machines can cause critical settings to drift
  - Poorly fabricated tooling and boards can cause interspaces.



### Thank you for your attention

#### Clive Ashmore cashmore@dek.com

