Results from 2007 Industry Defect Level and Test Effectiveness Studies

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Abstract
To select an optimal test strategy, good knowledge of defect levels and test effectiveness are two very important factors to include. In 1999 an industry defect level study was completed and was often referred to as the "One Billion Solder Joint Study". The content of this study was presented in several papers and articles [1],[2]. Other industry defect studies have also been done [3],[4] A study was performed in 2007 with data from 14 different companies from Asia, Europe, and Americas and with data from around 3.7 Billion solder joints inspected. This paper will present result from this updated study.

Test Effectiveness has also been presented in several papers [5],[6]. A test effectiveness study is a way to evaluate a test method's effectiveness to detect defects and is probably the most objective way to measure these very important characteristics. This paper contains updated data from this type of study. Effectiveness from ICT (In-circuit Test), AXI (Automatic X-ray Inspection) and combined results from AOI (Automatic Optical Inspection), FT (Functional Test) and MVI (Manual Visual Inspection) will be presented.

Keywords: Defects Per Million Opportunities (DPMO), Defect levels, Test Effectiveness, 3D AXI, ICT, AOI, Functional Test, Manual Visual Inspection

Introduction
Test engineers today have significantly more challenges than ten years ago. The board complexity is increasing with more components, more joints, higher densities, and new package technologies. The higher component and joint counts create more defect opportunities which lead to lower yields for a given defect level. At the same time, there are more test and inspection alternatives today with advanced technologies such as Solder Paste Inspection (SPI), Automatic X-ray Inspection (AXI), and Automatic Optical Inspection (AOI). These inspection technologies are today well established and provide real choices. Boundary-Scan test technology has also emerged as a popular electrical technique to complement In-Circuit Test (ICT) and Functional Test (FT). While these tools offer more choices, they also pose a dilemma. Which is the right test / inspection strategy? What is the test effectiveness of different test / inspection solutions? What are defect levels in the industry today?

This paper will focus on those questions. Agilent Technologies has performed many studies trying to find out industry defect levels [1][2]. Since those studies were done with data from 1999, Agilent thought it would be good to do a similar study today and asked me to do it. Agilent has also done test effectiveness studies [5], [6] with the purpose of finding out different test / inspection methods' effectiveness of finding different defects. Again updated test effectiveness studies have been done and the results have been included in the results that will be presented in this paper. Two main themes in test strategy selection are defect prevention (or process control) versus defect containment (or more traditional test and inspection). Should one of these two strategies be dominant or should both be used? To answer that question the number of random defects and the number of systematic defects needs to be known. A rough estimate of those numbers is also included in the studies presented.

The paper will discuss the key findings in the studies that have been done. It will also present the insights and conclusions from that work.

Methodology Defect Study
For the industry defect level study the following method was used to collect and analyze the data. All Agilent 5DX AXI users with a data collection system where data could easily be extracted were invited. 14 users from around the world accepted and provided data. Since this is very sensitive information only one person, the author of this paper, knows which users submitted data. For the purpose of this paper and to maintain anonymity, these companies will be referred to as company A, B, C, etc. up to N. All defects are detected by 3D AXI, and the data is after the repair station, where it has been classified as a true defect, a process indicator, or a false call. It is important to realize a couple of facts about this collection method. First, only data from 3D AXI is included in the data, therefore defects detected prior to this point by mainly MVI and AOI are not included and can significantly impact the resulting Defects Per Million Opportunities (DPMO). Also data

from electrical test, such as ICT, Boundary-Scan, Functional, and System test is not included. Defects detected as electrical test are not included in the DPMO values presented, but are expected to have less impact on the numbers than the inspection steps prior to 3D AXI. In Table 1 you can see key facts about the DPMO study.

Table 1 – Key data about data gathering for DPMO study

Boards inspected	726,091
Joints inspected	3,675,298,930
Board types	1,138
Total users providing data	14
Users in Europe providing data	4
Users in Americas providing data	2
Users in Asia providing data	8

After the data was received some cleanup was done. For example, data from boards that were inspected during program development were removed. Also, data from boards that were inspected more than 1 time was removed. If you include that information, the number of defect opportunities and number of defects are tricky to get right. Only a few percent of the boards were inspected more than 1 time. A few companies also provided a lot of data, so to make it more manageable the data was limited for each user to slightly over 500 million solder joints. Table 2 shows how much data was provided and used for each of the 14 companies.

Table 2 - Data provided and used by companies

Company	Joints inspected
A	240,328,802
B	415,898,135
C	400,063,071
D	531,501,641
E	57,594,032
F	30,432,110
G	54,878,817
H	113,359,833
I	529,211,454
J	314,924,245
K	384,748,491
L	9,937,099
M	532,827,413
N	59,593,787
Total	**3,675,298,930**

The data was then analyzed for number of defect opportunities and number of defects. What the repair operator had marked as repaired or repair later was included as defects. Process indicators, which are borderline defects, were also noted but will be reported separately. Please note that DPMO numbers are presented on a joint basis. Every inspected solder joint is one defect opportunity, and every defective solder joint is counted as one defect. Maximum one defect is counted per solder joint. Analysis of defect spectrum was also done on the data. On a randomly selected subset of the data an analysis of random defects and systematic defects was also done.

Data Results DPMO Study

The DPMO result for each company can be seen in Figure 1. The companies are called A, B, C, up to N. The defects are the solid lower part of each bar. A few companies have below 50 DPMO measured at the 3D AXI system and one company, N has over 2,000 DPMO. The average for all 14 companies is 327 DPMO of repaired defects.

The hatch-mark of the top parts of some bars represents process indicators. Process Indicators are a deviation from the norm, but not significant enough to render a repair action. However, process indicators are very close to being defects so it is a good idea to keep track of them. A good process engineer is always trying to tweak the process in an effort to minimize process indicators, because minimizing process indicators also help minimize defects. The average rate of process indicators is 245 DPMO, or more correctly called PIPMO (Process Indicators Per Million Opportunity) of all 14 companies. If the defects and process indicators are added together the result is 572 “DPMO”. The result of the “One Billion Solder Joint

Study" from 1999 was 1,083 "DPMO" that should be compared with the 572 in this study. At first glance it looks like defect levels have been cut in half over the last eight years; however that is probably not the case. As was stated earlier the defect numbers are only from 3D AXI so prior inspection by AOI and manual visual inspections is not included. Checking with the companies today almost all of them have AOI, MVI, or both prior to the AXI inspections and to a larger extent then in the 1999 study. Therefore, part of the improvements shown in this study can be explained by that, however an improvement in defect levels is also likely the explanation.

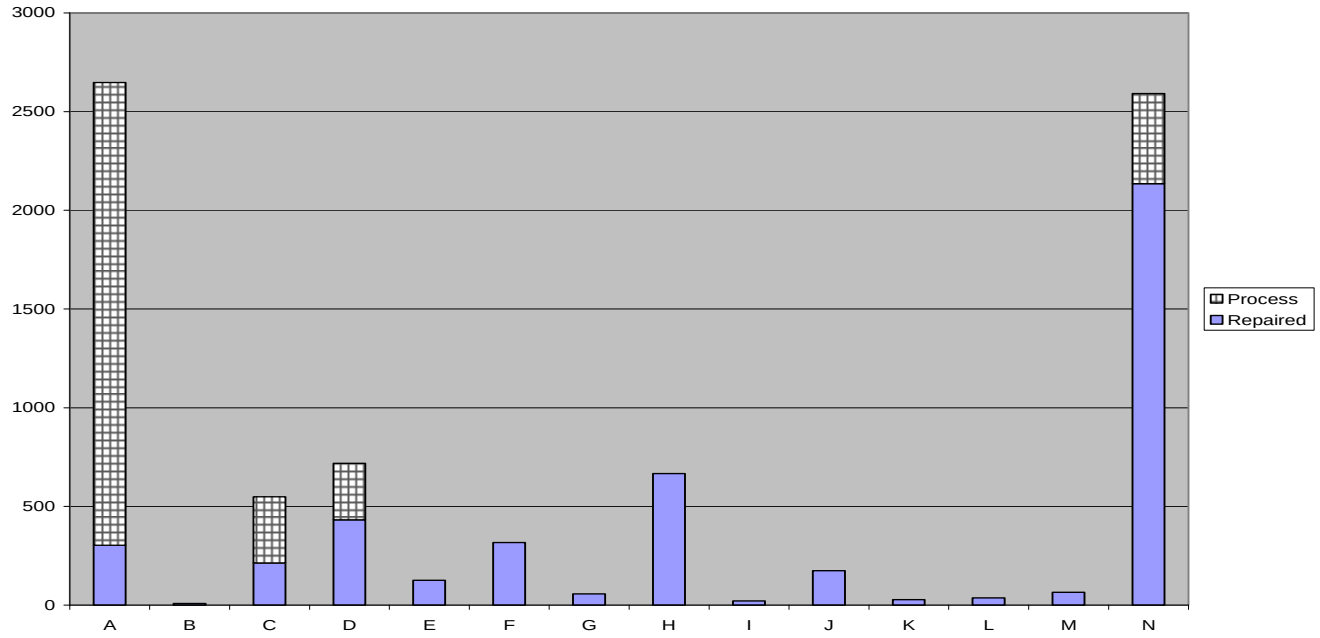

Figure 1 – DPMO per company. Repaired and Process Indicators

The defect spectrum can be seen in Table 3 and also in Figure 2. The most dominant defect type is insufficient solder, followed by misaligned component. Note that those two defect types have an X to the left on them as well as the defect type raised component. These defect types are very likely to pass electrical test such as ICT, functional test, as well as system test and are likely to be shipped to the end customer, where some of these defects may be warranty failures or field failures. In Figure 2 these defect types have been noted with a reddish color. Some of the other defects such as missing component, open, shorts, or damaged component will also be detected by electrical test, but typically not all of them.

Table 3 – Defect spectrum

	DEFECT TYPE	# DEFECTS	PERCENT
X	INSUFFICIENT	373,710	31.1%
X	MISALIGNED C.	281,683	23.4%
	MISSING C.	171,246	14.2%
	OPEN	156,041	13.0%
	SHORT	115,082	9.6%
X	RAISED C.	75,143	6.3%
	DAMAGED C.	16,201	1.3%
	OTHER	12,716	1.1%
	TOTAL	**1,201,822**	**100.0%**

Another key question for test strategy selection is how many of the defects are random and how many are systematic? To try to answer that question some analysis on the data was done. Specifically, in the data set there were 1,138 board types, but one criterion was to limit that data so it did not include prototype boards so it needed to be more than 100 boards manufactured. Also another criterion was that there were at least 1,000 inspected solder joints per board type. The final criteria was to exclude boards that had just a few components inspected, so to be included it needed more than 20 components inspected. 430 board types met those criteria's. Out of those 430, 10 board types were randomly selected.

What was considered a systematic defect in this analysis? In this study it was declared a systematic defect if a reference designator showed up on 3% of the board or more. The possibility was not considered that the same systematic defect on several similar components, for example a wrong size pad on a set of chip components. If those were included, the number of systematic defects would increase, in the number calculated.

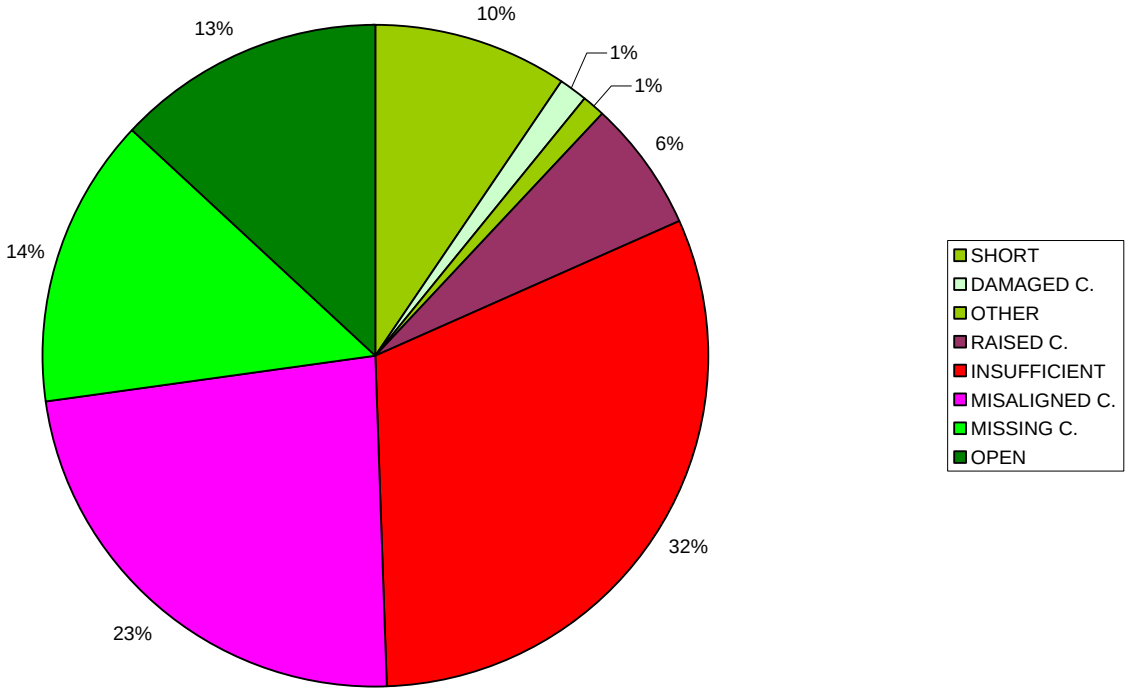

Figure 2 - Defect spectrum of new study

On the other hand, the types of defects on that component were not considered either, for instance if U1 was misaligned, another was missing, and the third had an open, in that case it was counted as a systematic defect. This is an example of a factor that would decrease the number of systematic defects in this study. Therefore there are factors that both decrease and increase the number of defects in both categories. To some extent, this will even out. Keep in mind that the objective with the analysis is only to indicate ball park numbers. For a very accurate analysis real boards with defects are needed. The 3% same reference designator number is based on engineering judgment and is believed to be rather conservative.

So what was the result of this study? Systematic defects were 27% of all defects, 73% of all defects were random. Again just think of this as ballpark numbers. In Figure 3 the results from all 10 randomly selected boards can be seen. As one would expect there are different situations. Board #6 has around 70% systematic defects, and board #3, #4, #5, and #8 have no systematic defects. Again the average was 27% systematic defects, and 73% random defects. In this study, around 75% of defects are random, so the question is - should defect prevention strategies be implemented if only around 25% of defects are systematic? And the answer is ABSOLUTELY! 25% is a very significant amount and preventing defects are always the best way to handle them. However, since a majority of defects are random in nature, an effective defect containment strategy is also needed, especially for medium and high complexity boards with many defect opportunities.

Methodology Test Effectiveness Studies

A test effectiveness study is a study on the production floor with real boards and with real naturally occurring defects. A typical test effectiveness study takes around a week to perform. A number of boards are manufactured; no test, no inspection or no repairs are done on the boards. Then the boards are inspected by the first system in the study, maybe an AOI system. All calls by the AOI system are classified as true calls or falls call. This is important, no repairs are done. Then the boards may go to a 3D AXI system, again all calls are classified but no repairs are done. Then the boards may go to an ICT system and after that to Functional test. If it is done this way, then all test and inspection systems have the same chance of finding

all defects. In all cases it is the user of the test / inspection system that decides what a defect is and what is not. Agilent has done many test effectiveness studies around the world and in this paper will show the combined data from 9 studies that have complete data in order to construct a Venn diagram. Those studies have been performed at 9 different sites, on a total of 421 boards. No repairs were done between test steps, except for shorts were repaired at ICT. To be able to compare systems only one defect per component maximum is counted. In all of these 9 studies ICT and 3D AXI were present all the time. There was also always a third test / inspection method in the result and it was AOI, manual visual inspection, or Functional test. The 3D AXI system was always the Agilent 5DX, for ICT and AOI there were different vendors system in these studies.

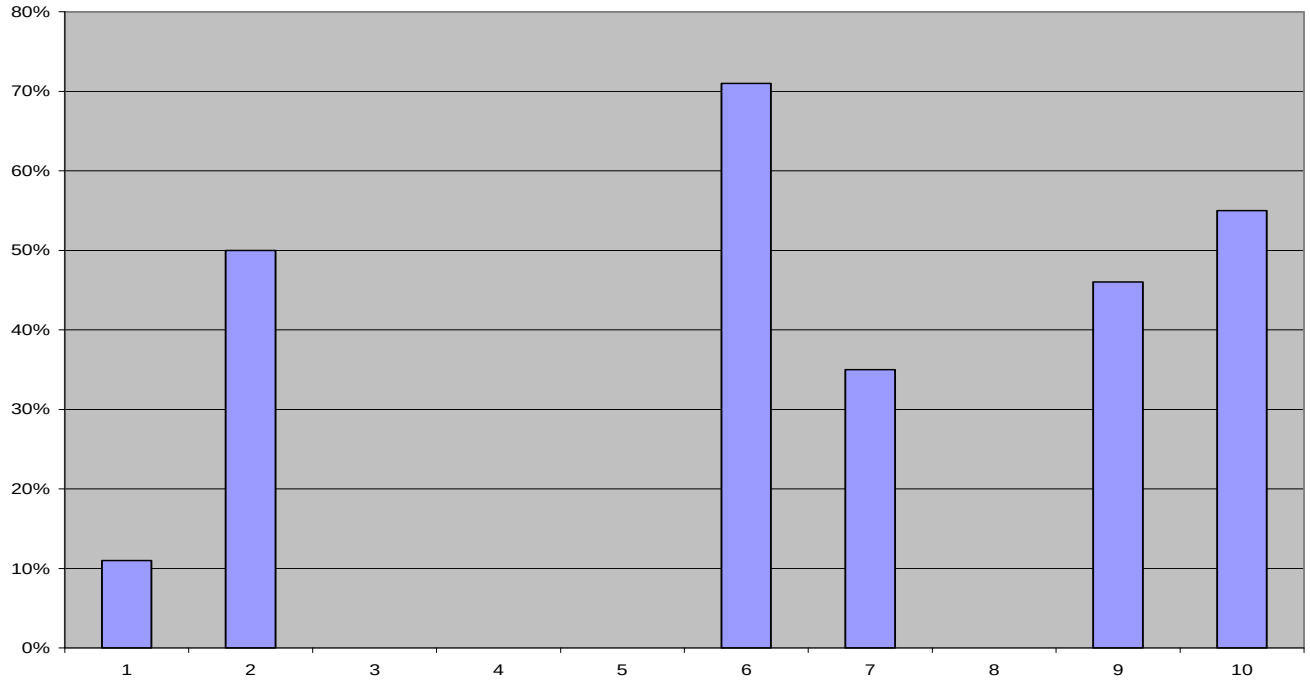

Figure 3 – Systematic defects per 10 randomly selected board types

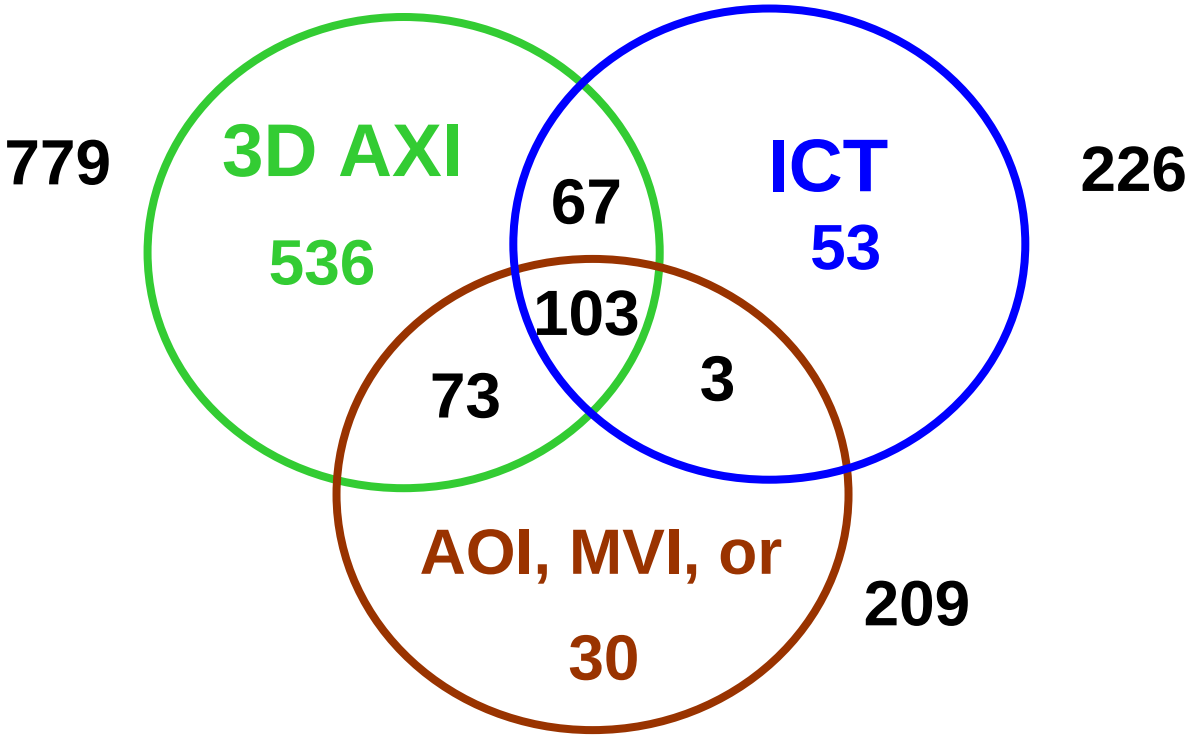

Figure 4 – Defects found by different test methods in 9 studies

Data Results Test Effectiveness Studies
The test effectiveness for one test or inspection system is the number of defects found by that system divided by number of all defects in the test set, expressed as a percentage. Finding all defects may be difficult to do. In the test effectiveness studies that has been done the number of all defects found is used and should be close to the real number since a well diverse test set has been used.

The combined result of the 9 test effectiveness studies can be seen in Figure 4. There were a total of 865 defects found. ICT found 226 defects and 53 of these defects no other system found. AOI or Manual Visual Inspection or Functional Test found 209 of the 865 defects. The 3D AXI found a total of 779 out of the 865 defects and 536 of those defect no other test method found.

In Figure 5 the test effectiveness in these studies can be seen. 3D AXI found 90% of all defects, ICT 26% and the third method found 24%. The size of the circles now better indicates the test effectiveness or defect coverage.

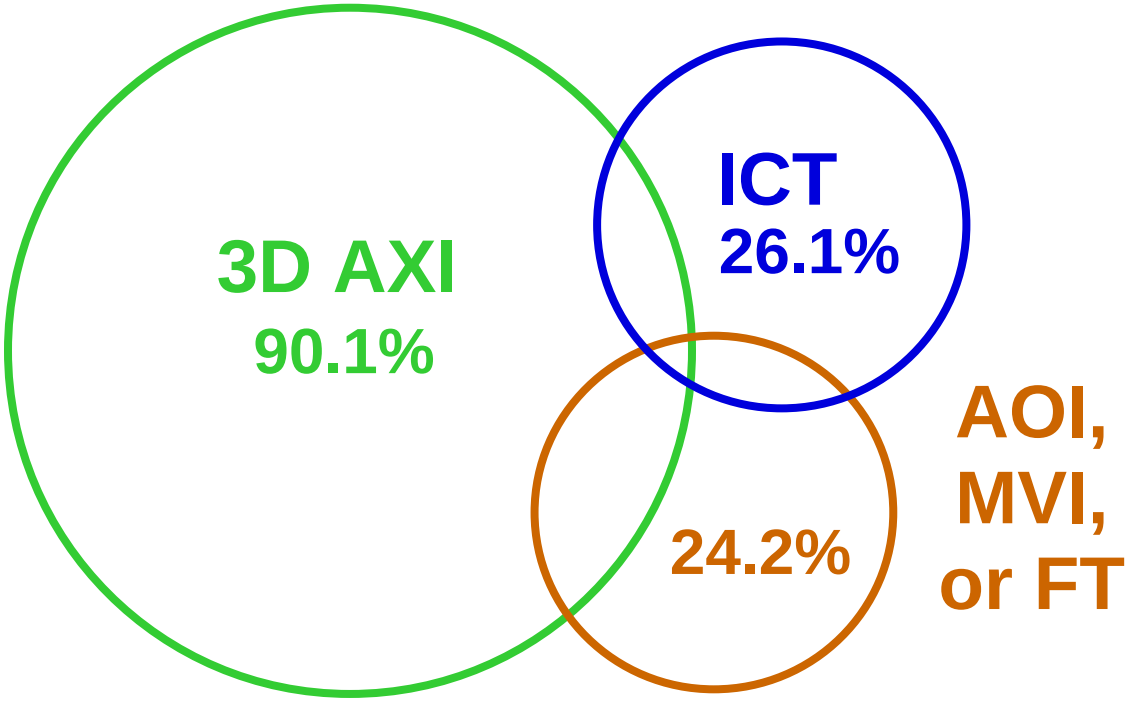

Figure 5 – Test Effectiveness in 9 studies

If data from all the test effectiveness studies that have been done is included and, not only the ones used to do an accurate Venn diagram, the test effectiveness for the system has been, 3D AXI 85-95% effective. Post-reflow AOI is 25-75% effective. The higher number that has been seen was in a case with no wave solder or selective wave. The lower number was in a case with wave solder. On average AOI finds around 40-50% of the defects. Note that AOI systems from various vendors have been included in these studies. The ICT result has been from 20% to 60%. Again different vendors ICT system have been included. Functional test effectiveness has been between 5 – 20%. It has been interesting to see that Functional Test is not that effective on finding many of the manufacturing defects.

Conclusion
In the industry defect study that has been done during 2007, the defect levels are still high, over 300 DPMO and if process indicators are included the number is over 500. The number is half what it was in the 1999 study and the most likely explanation is a significant higher use of MVI and AOI for the companies providing data in this study. In the 1999 study no Asian companies provided data. It is also likely that some improvements in defects levels also have happened during the last eight years. A significant number of defects found by 3D AXI, more than 50%, are defects very unlikely to be detected by electrical test. These defects should be thought as “walking wounded” and some of these defects are likely to end up as end customer field failures with warranty implications.

A rough attempt to analyze the number of random defects and systematic defects was done on the data set. Around a quarter of all defects seem to be systematic and indicate that a good defect prevention strategy in solder paste inspection and pre-reflow AOI or MVI should be implemented. This data also shows that around three quarters of defects are random and good defect containment strategies should be implemented by post reflow test and inspection.

The test effectiveness study, which is probably the most objective way to measure defect coverage, shows that 3D AXI had the highest test effectiveness. However, it also shows that a good test strategy is a combination of inspection and electrical test since some defects can only be detected by inspection AXI, AOI and/or MVI, while other defects can only be detected by electrical test. Which combination of these test and inspection solutions that should be used is a matter of the complexity of the board [7] and should be done on an economic basis.

References

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[2] Stig Oresjo, "Defect levels for different component types at the PCBA manufacturing process", Proceedings of SMTA International 2001.

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[5] Tracy Ragland, "Test Effectiveness: A Metric for Comparing Apples to Oranges in Electronics Test", Proceedings of APEX 2002.

[6] Tom Molamphy, "Six case studies show more defects shipped than expected: What to do about it", Proceedings of APEX 2002.

[7] www.agilent.com/see/complexityindex

Results from 2007 industry defect level and test effectiveness studies

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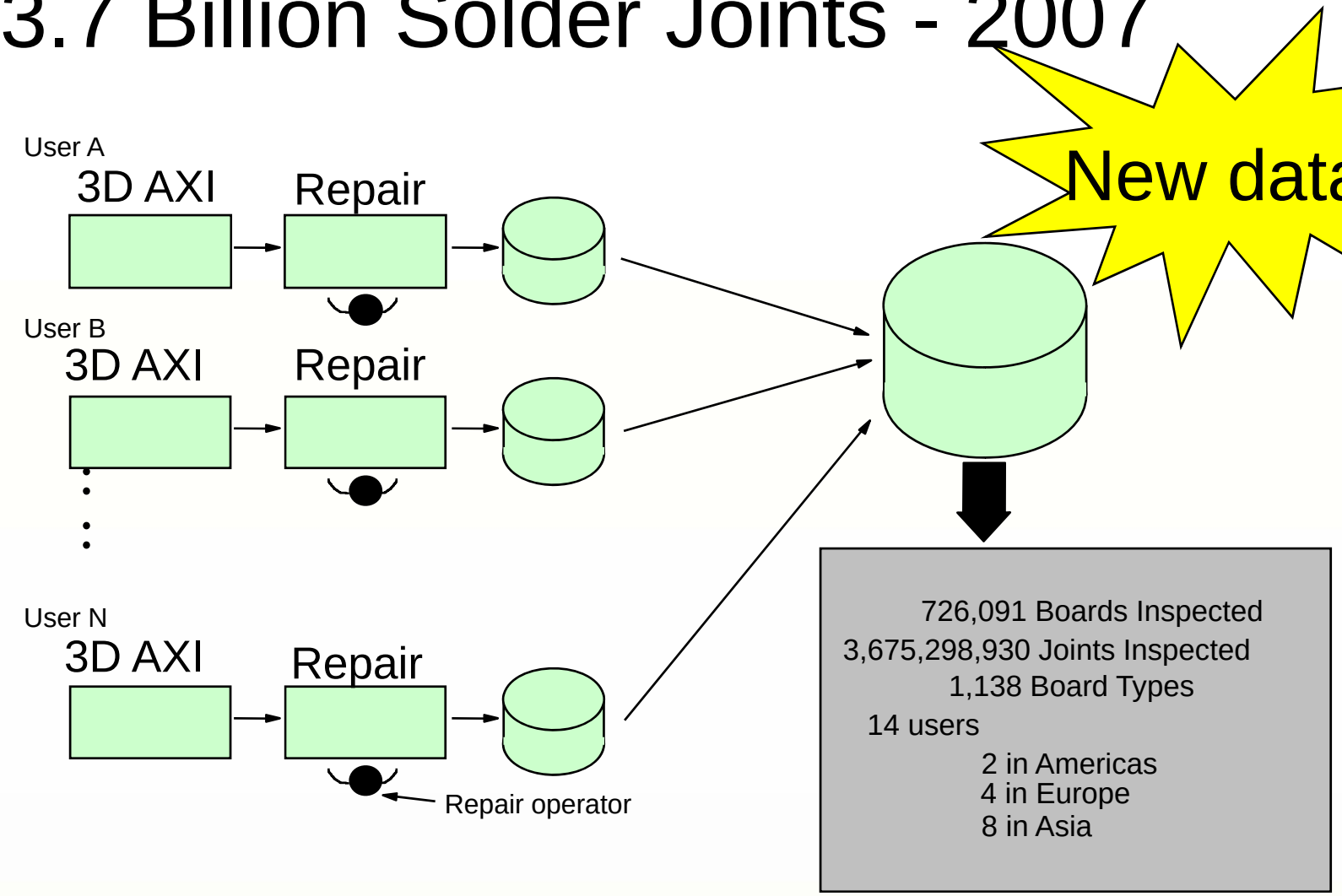
Topics

- New DPMO study
  - Systematic and random defects
  - New test effectiveness studies
  - Summary

3.7 Billion Solder Joints - 2007



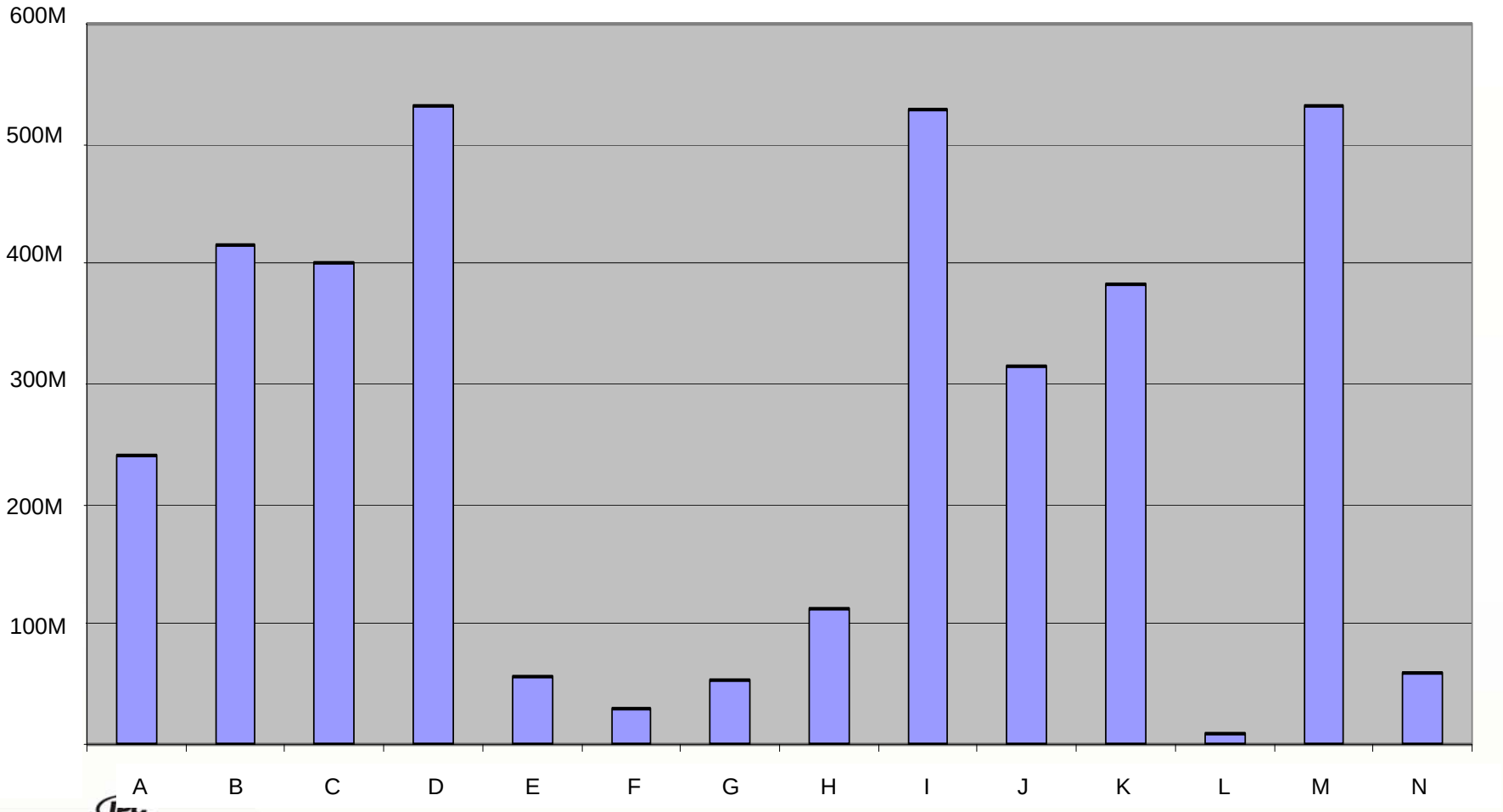
Most of the data is from early 2007

Data “clean up”

- Removed debug boards
  - Serial Number = “Family”, “Component”
  - Serial Number obvious debug
- Boards inspected > 1 time
- Data over around 500 million joints inspected

Solder Joints inspected by company

- 14 companies/sites, total = 3.7 billion



DPMO Repaired and process indicators

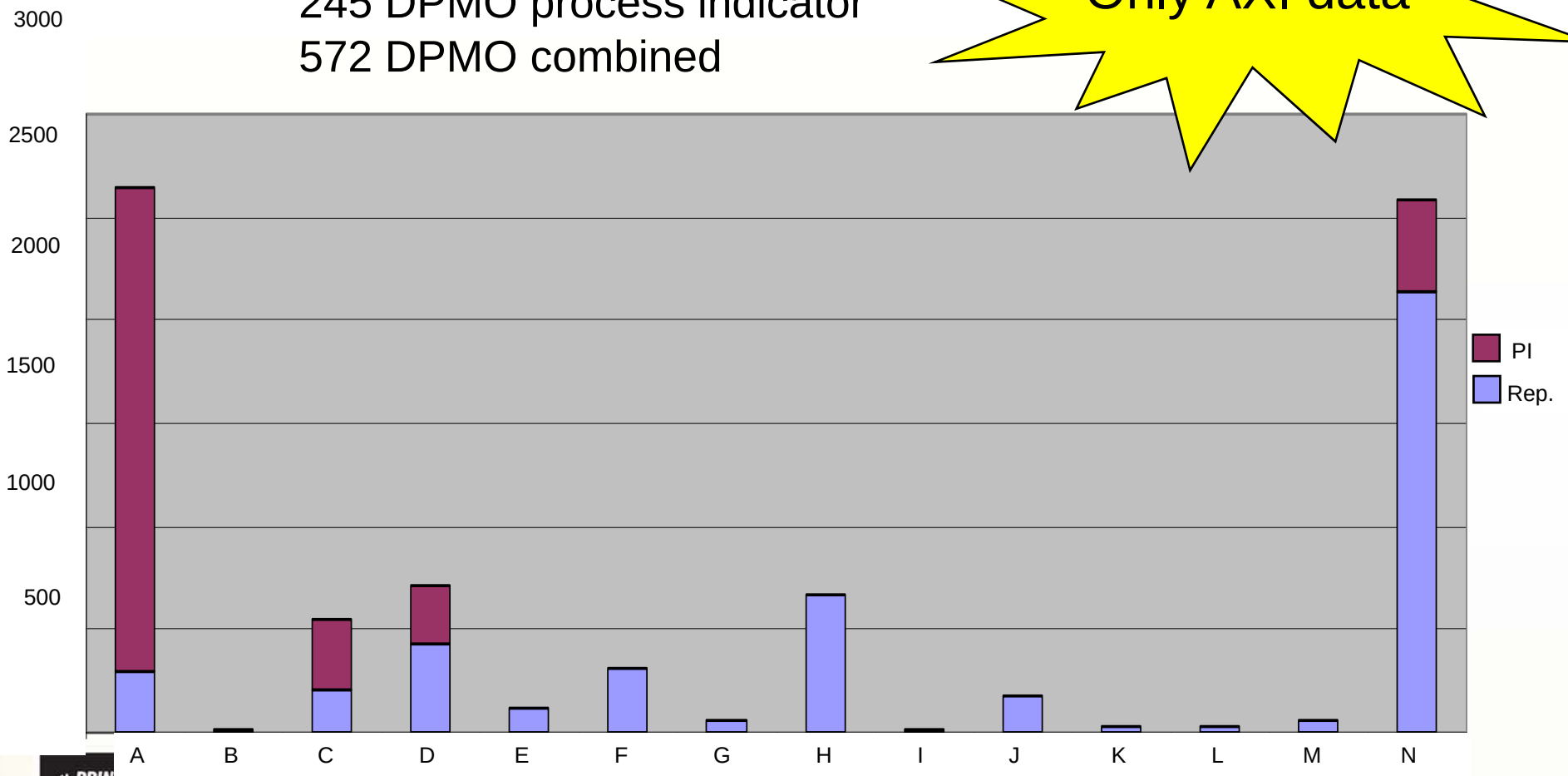
Average numbers

327 DPMO repaired

245 DPMO process indicator

572 DPMO combined

Only AXI data



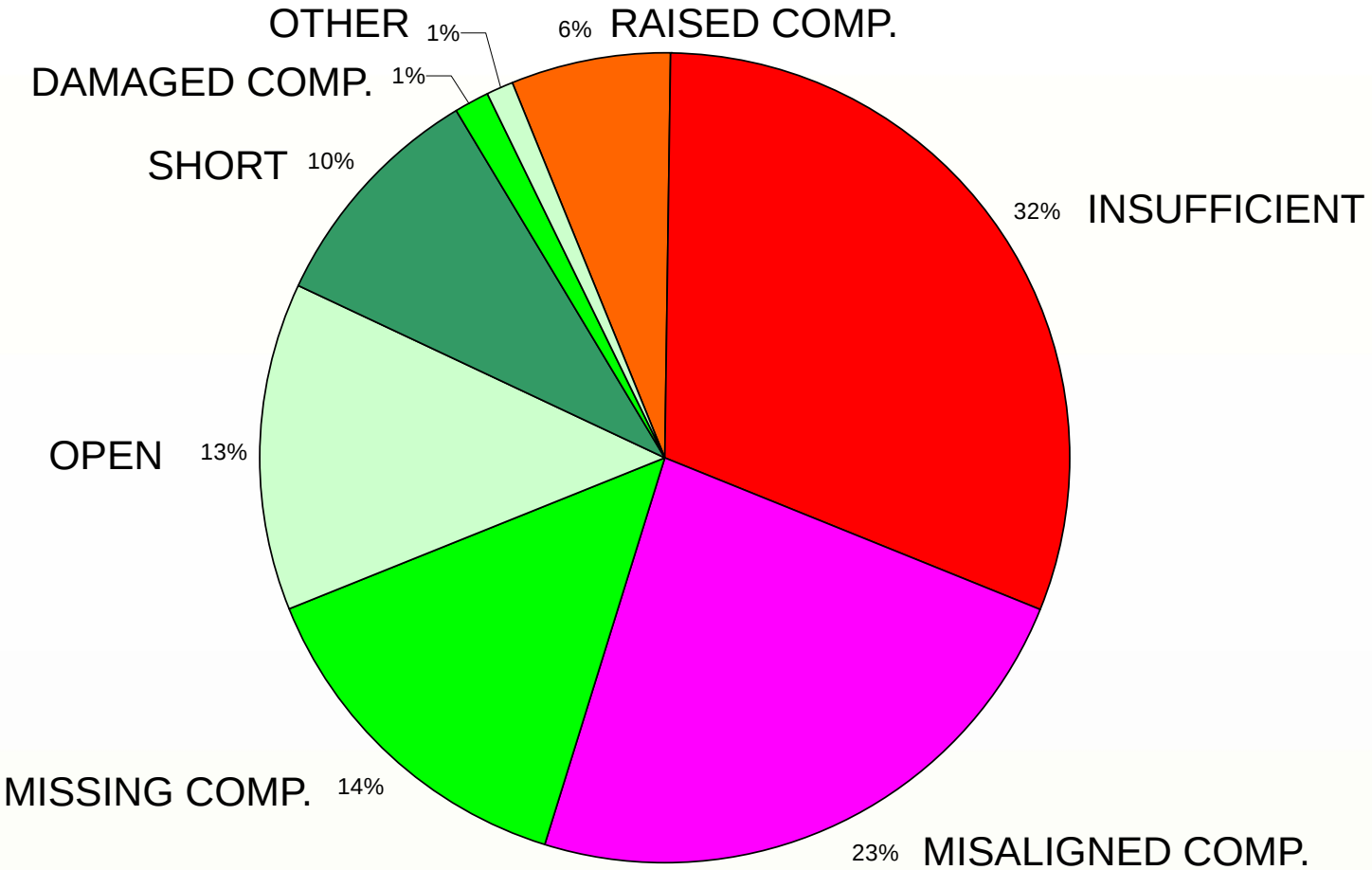
Keep in mind

- Only data from 3D AXI
- Defects found at MVI, AOI, ICT and FT not included
- In most cases MVI and / or AOI prior to 3D AXI

- MVI = Manual Visual Inspection
- AOI = Automatic Optical Inspection, including Solder Paste Inspection
- ICT = In-circuit test
- FT = Functional Test

Defect spectrum

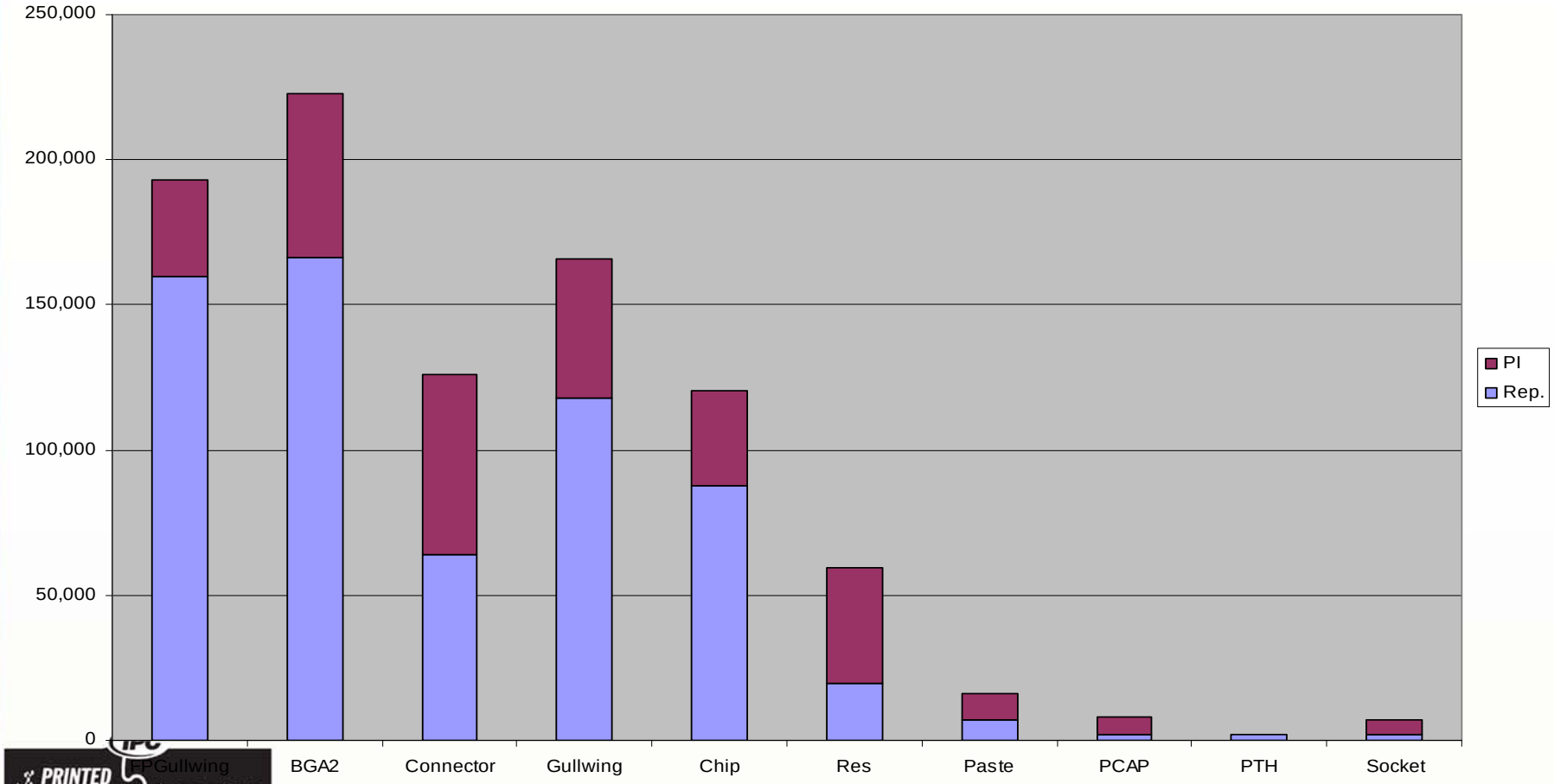
1,201,822 defects



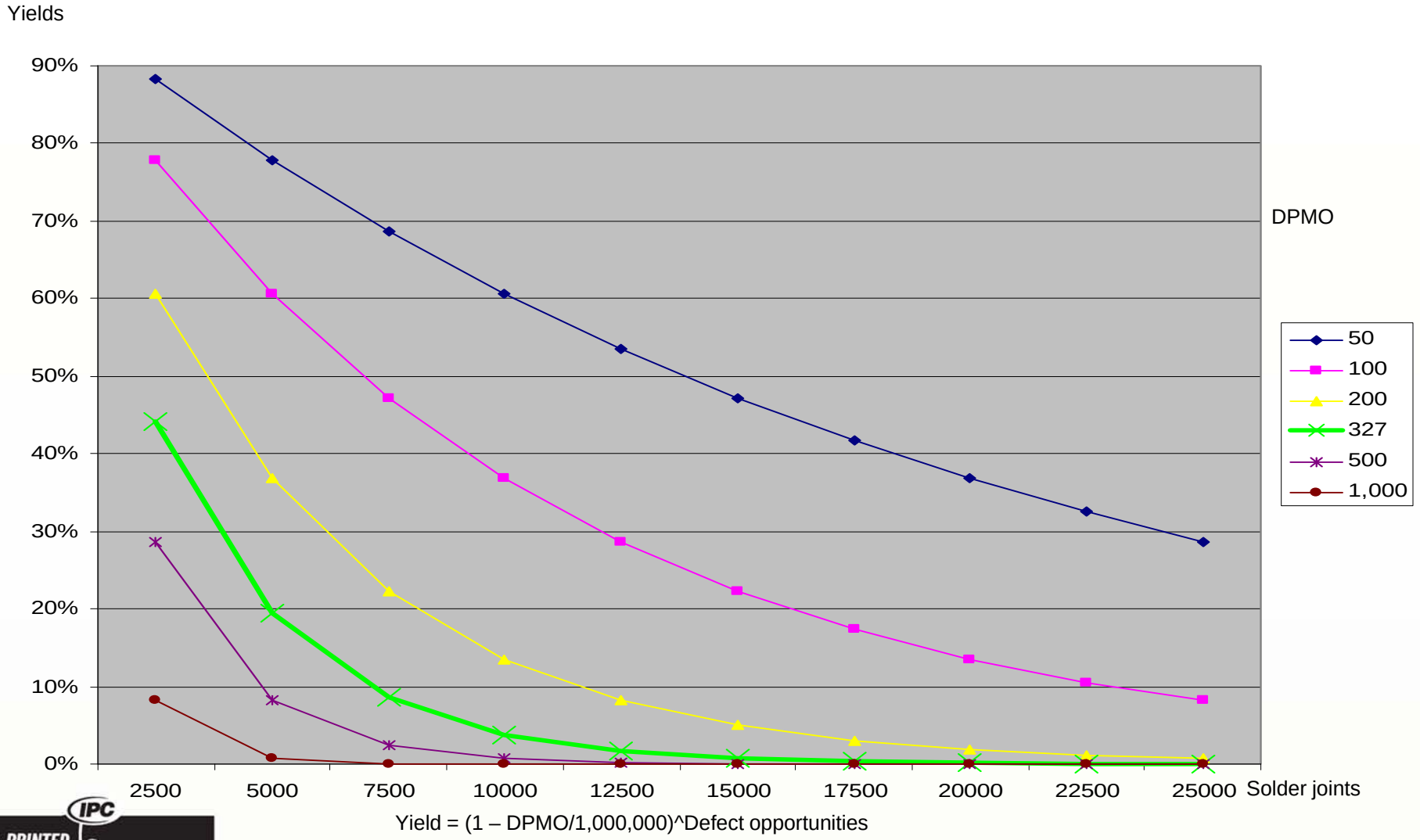
Calls per 10 topped called algorithms

This is showing calls after repair operation, only for the top 10 algorithms based on # of calls.

(Number of opportunities per algorithm is not recorded, therefore DPMO values can not be calculated)



Estimated yields



Yield = (1 – DPMO/1,000,000)^Defect opportunities

Topics

- New DPMO study
- Systematic and random defects
- New test effectiveness studies
- Summary

Question

Are defects systematic?
And if so what percent are systematic?

Boards available for analysis

1,138 board types in data base

Selection criteria:
>= 100 boards manufactured
>= 1000 joints inspected
>= 20 components inspected

430 board types meet criteria
Production volume from 100 to 72,834

10 boards were selected randomly

What is a systematic defect?

In this analysis the following was used:

Same reference designator called* on >= 3% of the boards

*Called with repair, repair later, or process indicator actions.

Factor that could under-report** # of systematic defects
Several RefDes same basic problem (DFM issue)

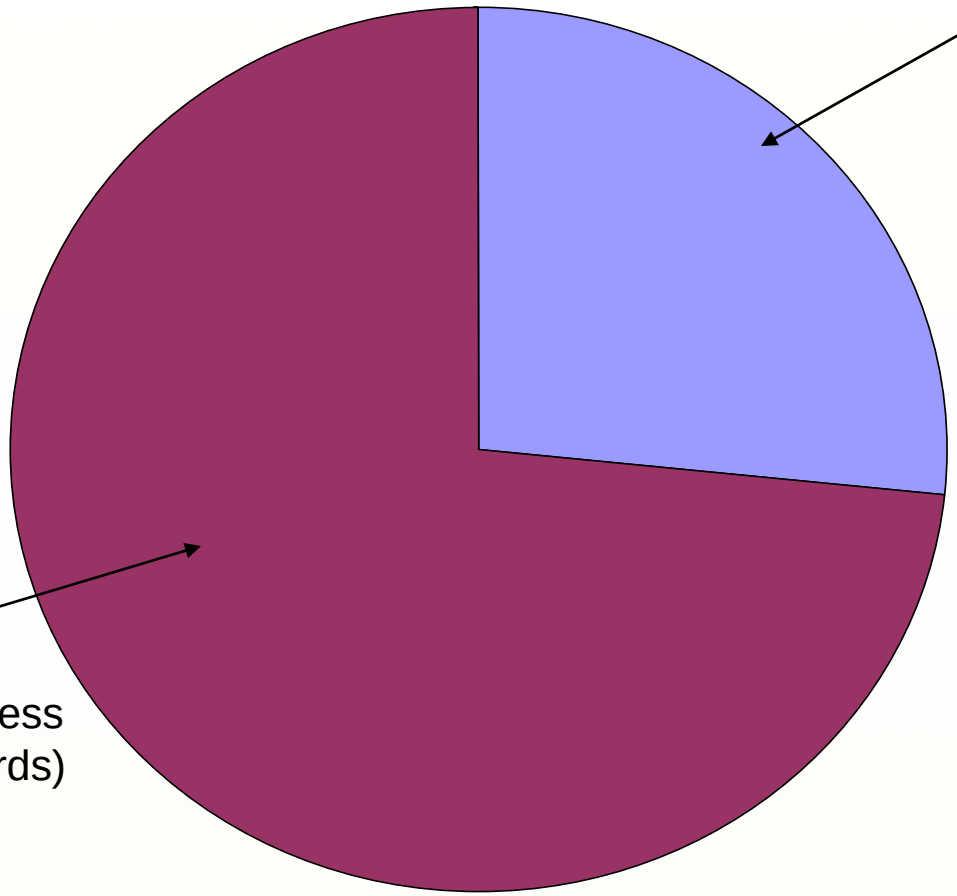
Factor that could over-report*** # of systematic defects
All defect types for one RefDes considered systematic

** Increase # defects in real sample compared to result in analysis
*** Decrease # defects in real sample compared to result in analysis

Objective with study is only to indicate ball park numbers.
For precise analysis availability to boards with defects are needed.
3% was selected on engineering judgment basis.

Result

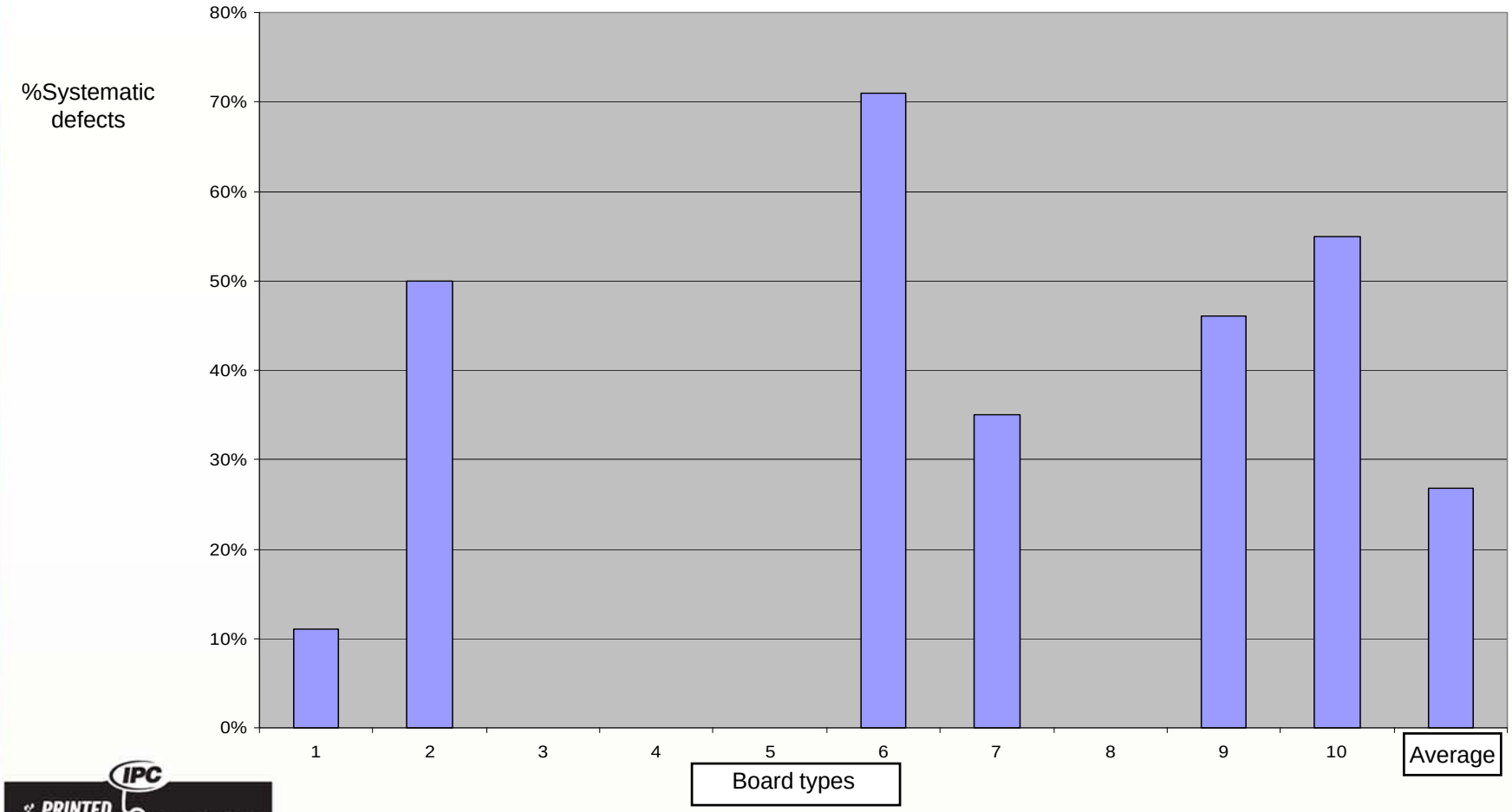
For 10 boards types randomly selected.
Number of random defects 73%



("Same" defect on less than 3% of the boards)

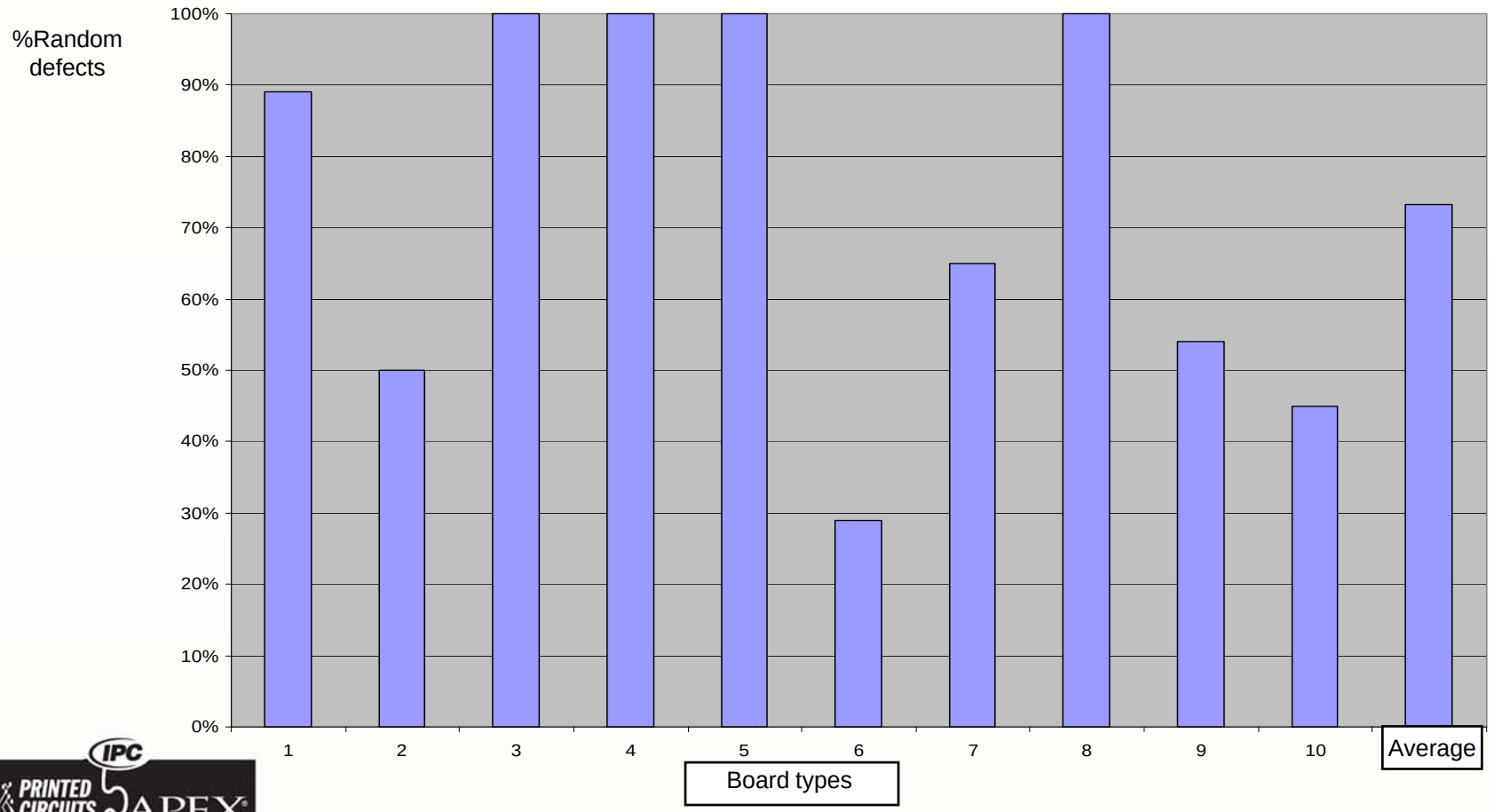
Result

For 10 board types randomly selected.
Number of systematic defects



Result

For 10 board types randomly selected.
Number of random defects



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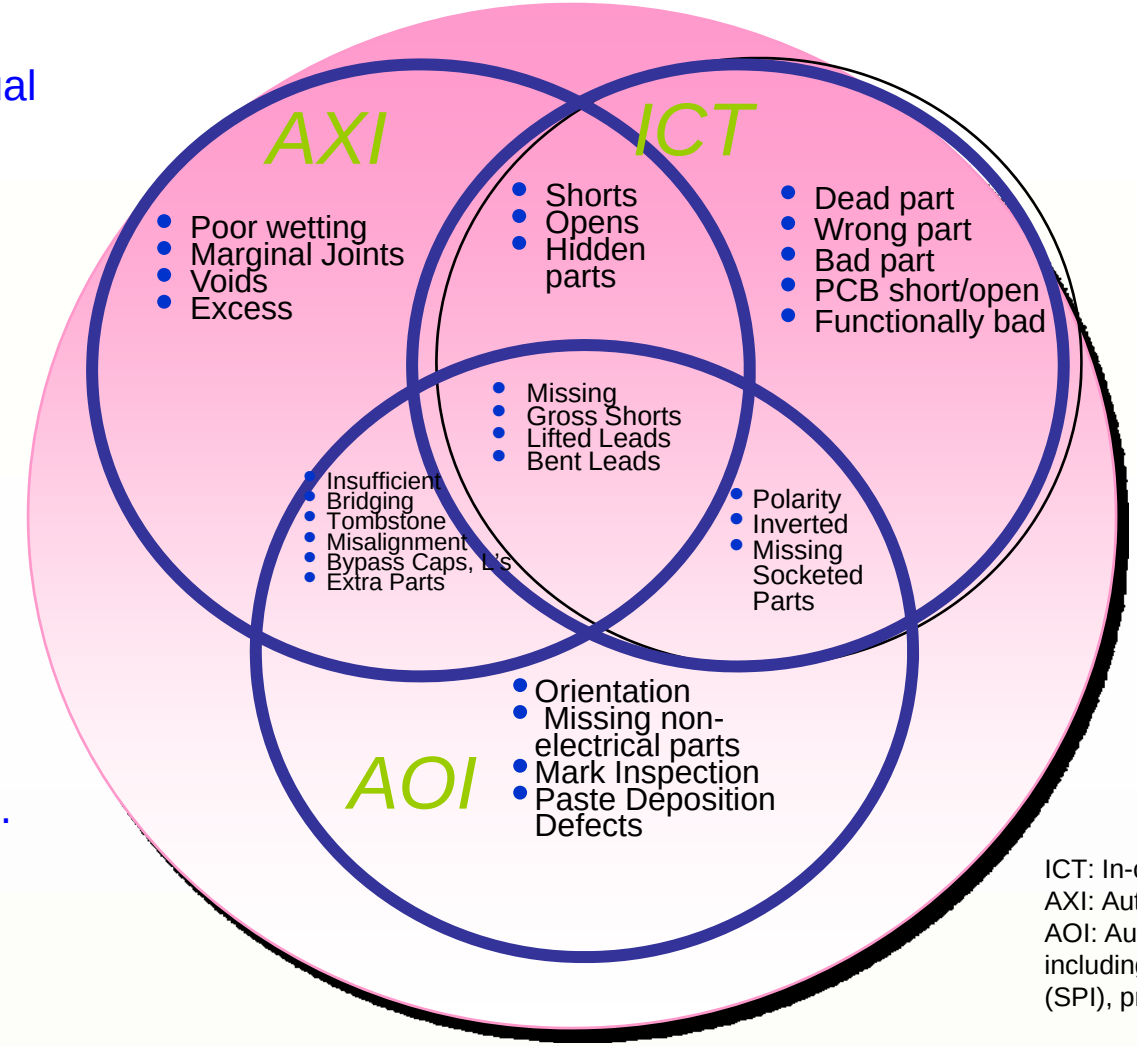
Defect coverage

This is a conceptual diagram!



How do you get accurate data? ….

ICT: In-circuit Test
AXI: Automated X-ray Inspection
AOI: Automated Optical Inspection – including solder paste inspection (SPI), pre-reflow and post-reflow.

Two major methods

Both methods are valid and have their advantages disadvantages

- PCOLA-SOQ

A theoretical calculation of one or several test methods and programs coverage against “all” possible defects.

Device properties

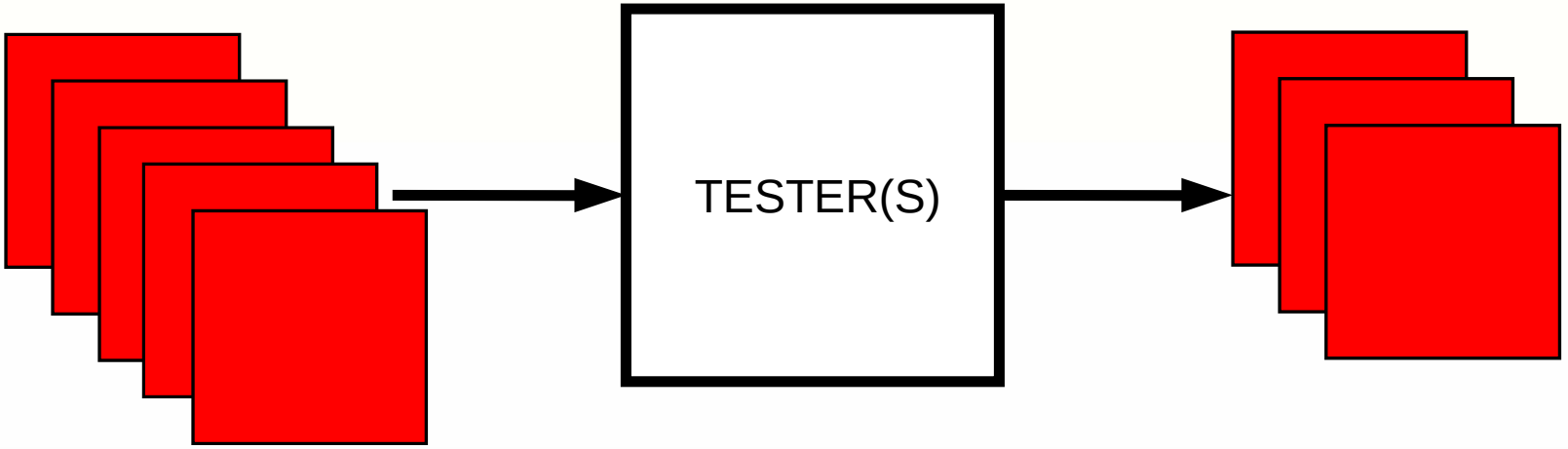
- P - Presence
- C - Correct component
- O - Orientation (90,180, 270 degrees off)
- L - Live (basic function)
- A - Alignment
- Test Effectiveness Studies . . . .

Joint properties

- S - Short
- O - Open
- Q - Quality

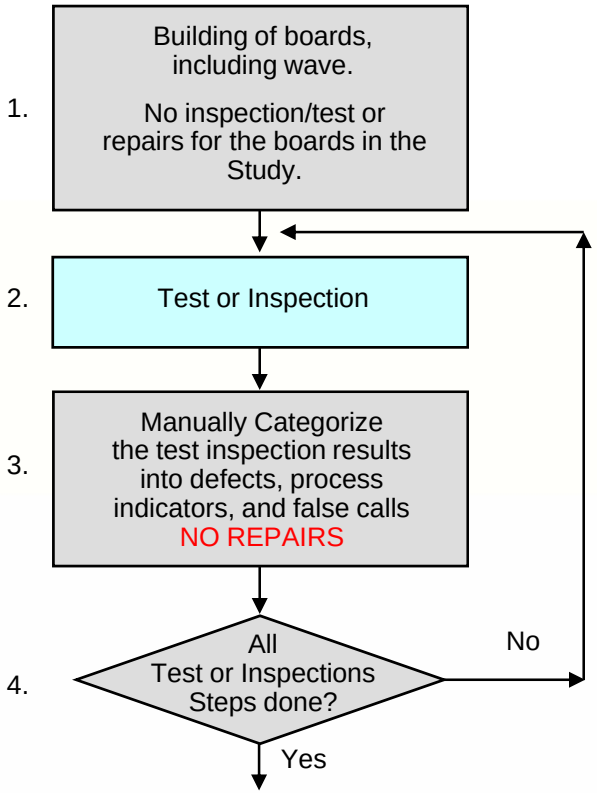
What is Test Effectiveness?

- Test Effectiveness is a measure of the “goodness” of your test and your test /inspection equipment and programs using real data in production.



Test Effectiveness = (10-3)/(10) = 70%

Test Effectiveness Evaluation Flowchart



Customer has final say on what is a defect, process indicator, or false call.

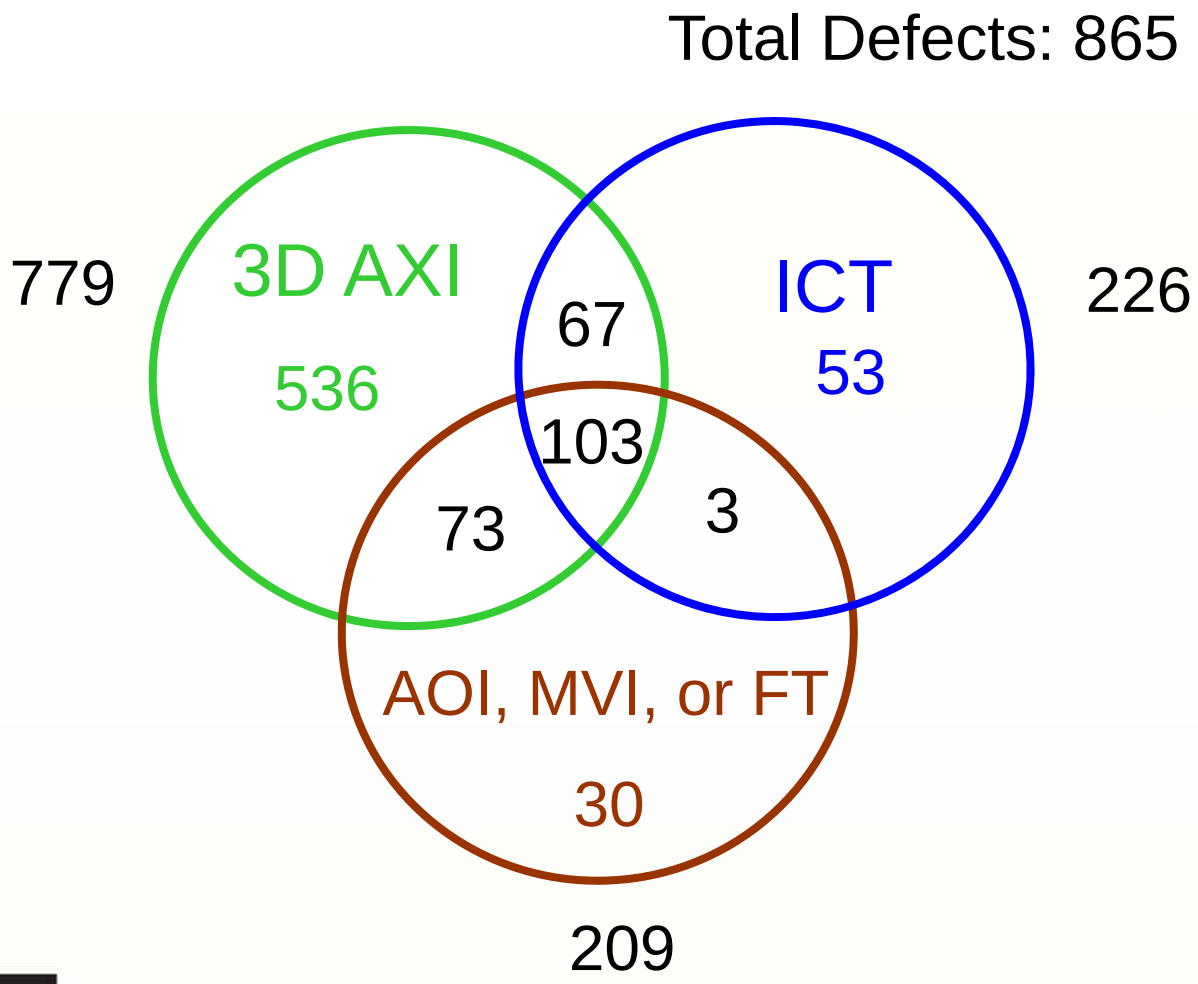
Only defects are included in Test Effectiveness data.

Case Study

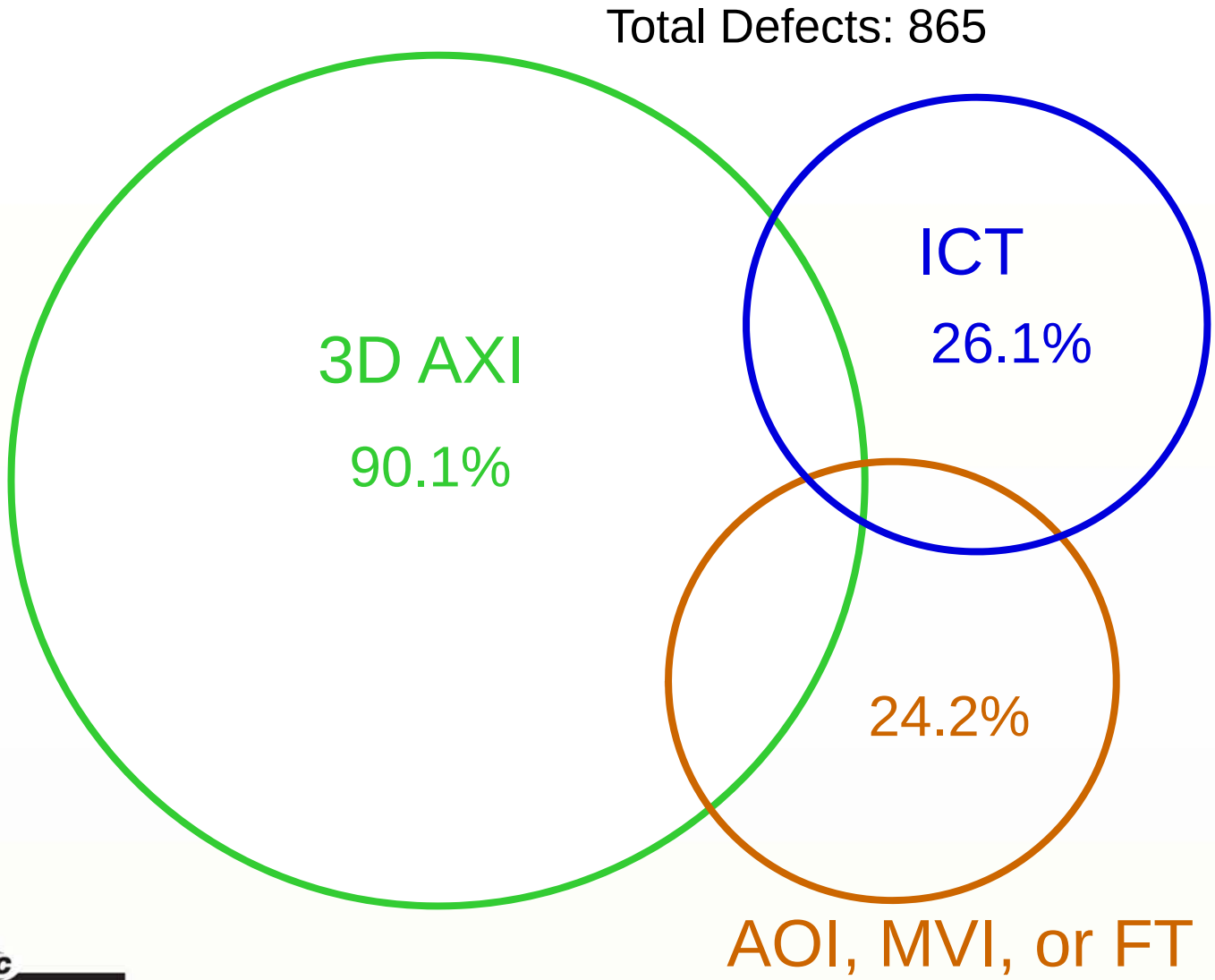
- **Compilation of nine similar studies performed in nine separate manufacturing facilities**
- **421 assemblies tested**
- **No defects repaired between test/inspection steps (except shorts at ICT)**
- **Only one defect per component**
- **3D AXI and ICT always present in study**
- **One of AOI, Functional Test, and Manual Visual also present**

Most of these studies have been done on medium to high complexity boards with medium to low manufacturing volumes.

Summary TE Studies – 421 boards



Summary TE Studies – Defect Coverage



Test Effectiveness studies - Summary

Key learnings:

- 3D AXI Test Effectiveness		85% - 95%
- AOI	" "	25% - 75%
- ICT	" "	20% - 60%
- FT	" "	5% - 20%

These numbers includes both Agilent and non-Agilent systems (3D AXI is Agilent 5DX only)

All systems are not equal!!

Topics

- New DPMO study
- Systematic and random defects
- New test effectiveness studies
- Summary

Summary

- Defect levels are still high > 300 DPMO
- An effective defect prevention strategy is recommended
- A majority of defects are random
- 3D AXI is found to be the most effective test / inspection method.
- To achieve high yields at ICT and FT and to minimize warranty and field failures, use of an effective inspection solution should be considered, especially for boards with many defect opportunities.