Processing High Density Interconnects: Selecting the Best Option for Via Fill Applications

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Abstract
With the increased use of High Density Interconnects in printed wiring boards (PWB) there is a critical need for reliable methods to completely fill through hole and blind vias. Complete filling of the vias is often necessary to prevent solution entrapment or failures during thermal cycling. For double sided and multilayer printed wiring boards, complete filling of through holes and blind vias include the use of conductive and non-conductive polymeric ceramic filled paste materials, and the occasional use of liquid photoimageable soldermasks (for partial via filling) For blind vias at n-1, superfilling of the via with copper plating is also gaining acceptance in the market place. In addition, methods to fill buried vias include the use of filling with resin during lamination or the use of the polymeric pastes described above. Blind vias within a sublam can be filled via copper plating as well. The best option depends upon via diameter, via depth, productivity and reliability requirements. In recent years plating of microvias and using ceramic-filled plugging paste for buried vias has gained popularity. The purpose of this paper is to discuss the applications, advantages and disadvantages of each option and offer guidelines for selection of the process that will best suit the needs of the board manufacturer. Applications involving copper electroplating and ceramic plugging pastes will be discussed in detail. We will evaluate thermal stability of the vias using Interconnect Stress Testing (IST).

Introduction
Filling of plated through holes is not new to the PWB fabrication industry. For many years, end users required some or all via holes to be partially plugged with solder mask. This task was required in order to prevent solder from wicking through the holes (to the component side) during the assembly process and to create a vacuum for electrical test. Minimizing flux residues in the holes is another valid reason to undertake this operation.

Basically, the key reasons for via filling are:

- To increase the density and frequency for PWB's
- To minimize signal delays and avoid effects of electron migration.
- To make a smooth surface layer and avoid indentations.
- To enhance the I/O number of package substrates.
- To avoid incomplete fill of micro via holes filled by dielectric or conductive materials.
- To solve the differences in coefficient of expansion of metal and resin.
- To improve fine line design, via on via (Fig.1) and interconnect reliability.

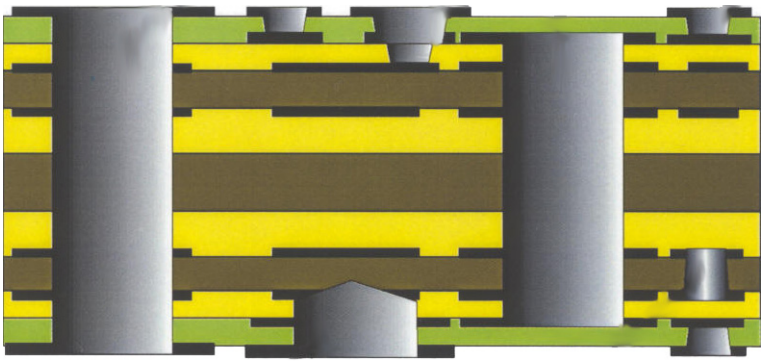

Figure 1-Types of Vias that can be filled

In Figure 1, the construction describes an HDI substrate with both plated through holes, filled buried vias and microvias. Certainly, all the via types described in Figure 1 are candidates for filling. The critical question is: What process (plating or paste fill) is indicated?

Generally, one hopes that the IPC will soon release a standards document to govern via filling. One such document is in the draft stage (IPC-4761). In general terms, one can describe the vias to be filled as follows:

- Completely plugged and overmetallized Via in pad
- Completely plugged buried vias over several layers as necessary
- Completely plugged and overmetallized buried vias over several layers as necessary

Certainly, filled vias may encompass multiple layers, depending upon the PWB design requirements for density and functionality. Some that espouse HDI as the technology of the future recognize that stacked and staggered microvias enable miniaturization. And to be successful in this endeavor, via filling processes must be utilized.

The concern of plugging through holes with a standard LPI resides in the fact that these inks are typically 60-80% solids content. During the drying/curing process, the solvent evaporates and the hole plug shrinks, often leaving a small gap between the through hole barrel and the plug. This of course, can lead to a lack of adhesion of the plug to the hole wall. There is a second risk: residual solvents from the LPI. During the curing process, operating conditions may lead to a "skinning over" of the plug. This scenario causes solvent to remain entrapped within the hole. The consequence is that the solvent will expand during the heat of the soldering operations, leading to cracking of the fill. As through hole aspect ratios increase, it may become impossible to evacuate all of the solvent. Process curing temperatures and ramp up time to cure must be carefully monitored, regardless of the technology level of the PWB. This issue will be presented in detail elsewhere in this paper.

However, as the introduction of stacked via and sequential build PWB technology exploded onto the scene, more attention must now be focused on via filling. Certainly, filling vias with LPI materials and hoping for success has been pretty much set aside in favor of newer processes. Leaving air pockets in the vias is not acceptable. These alternative technologies encompass either a filling of the vias with a thermal cured epoxy-ceramic filled material or plating the vias with a specially formulated acid copper process. The latter is often referred to as super-filling and has gained acceptance in the market place as a means to fill blind vias. Several firms, including Intel are very interested in plating vias so that they are completely filled.

It should be noted that with respect to paste-type fill materials, there are conductive and non-conductive formulations. For this particular research project, the authors will present data related only to the non-conductive paste material (in addition to reliability data related to plated copper via fill).

It will become clearer to the reader that the board design dictates which process to use and under what conditions. The authors will also present an overview of equipment and material considerations for the copper superfilling and the epoxy paste fill processes. Reliability of filled versus unfilled vias was also studied.

Common Via Filling Concerns

Whether the fabricator is asked to fill vias with epoxy paste or copper, the major concern is to accomplish the filling with little to no air pockets in the vias. The concern with air inclusions is that in effect, air is an insulator. Thus, air reduces both electrical and thermal conductance. While it is acceptable to endure very small voids in the via simply due to processing and material properties, it is desirable to minimize air voids through material property selection, via plugging techniques and equipment designs (1). Figure 2 shows examples of air pockets for paste material (left) and plated copper on the right.

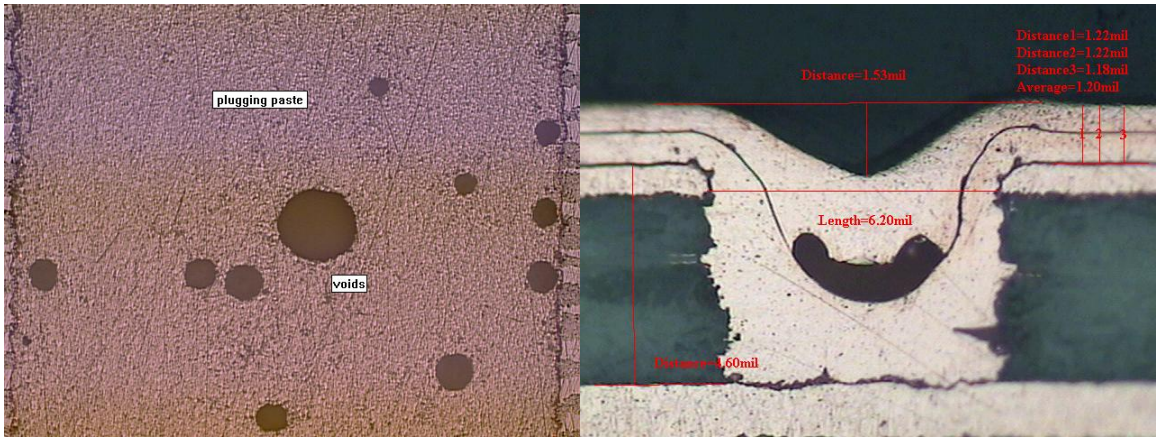

Figure 2 - Example of air voids from plugging paste process (left) and super filling process (right)

Other concerns and issues relate to dimpling (Figure 3). Minor dimpling has not been a concern from a component attachment perspective. Of course, excessive dimpling or shrinkage of a filled or plugged via may result in undesired

consequences that IPC-4761 will eventually address. Shrinkage of the plugged via may indicate unsatisfactory properties of the polymeric materials. These include improper curing of the epoxy paste, over curing and moisture absorption.

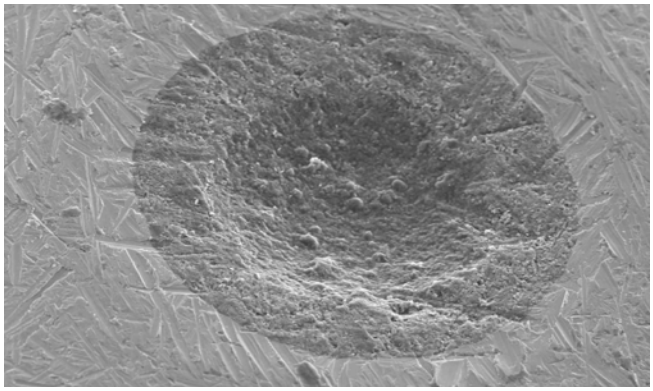

Figure 3 - Dimpling of Plugging Paste in Via (SEM photo)

With respect to superfilling with copper or with epoxy-based paste, a major concern relates to adhesion of subsequent layers of plated copper to the filled via. This includes over metallizing the filled via or attaching components during assembly. The fabricator must optimize up and downstream processes to insure adhesion of subsequent metallized layers.

Via Filling with Polymer (epoxy paste)
There are a number of techniques that are available for filling the vias with an epoxy paste. These are:

Roller coating
Plugging vias with the roller coating technique requires investment in capital equipment. Forcing the paste through the vias by means of a roller affects the plugging operation. Paste is held in a trough and the action of the roller picks up the paste on the underside of the roller. The PWB is pressed against the coating roller from above, and the paste that is located between the PWB and the roller is pressed through the vias. The board then passes through squeegees designed to remove excess paste.

The advantages and disadvantages of the roller coating process are detailed below.

Advantages:

- Rapid filling of vias
- No screen stencils required
- Ease of planarization due to relative cleanliness of surface
- Fewer process parameters to control versus screen process

Disadvantages:

- Vias not required to be plugged must be masked off
- Higher risk of dimple formation in the plug
- Trough volume of 8-10 kg's required(paste must have good shelf life)
- Aspect ratio limitations (maximum is 5:1)
- Blind vias difficult to fill

The issue of dimple formation is strongly correlated to flow characteristics of roller coating formulations. These particular formulations, due to viscosity requirements and flow, lead to capillary effects. Essentially this means that the smaller the hole diameter, the greater the dimple. This issue provides a limit to what roller coating for via filling can achieve. Newer formulations have been developed that have had their curing characteristics modified to eliminate this potential for sagging.

Screen printing
This process employs a stencil with the via pattern drilled to match the pattern of vias on the PWB. Screen printing requires that the vias be completely filled with one stroke of the squeegee. Otherwise, air will be entrapped within the plugging paste. One particular requirement for the screening process is that ink should protrude equally from both sides of the via. This requirement is met by placing a backup board (a stencil) drilled with the same hole pattern underneath the PWB. This allows the paste to fill the via while minimizing air inclusions. A small nail head is formed on the underside, ensuring a complete fill.

Of course, unlike the roller coating process where few operating parameters were considered critical, screen plugging of inks is a different matter. Screen mesh, screen tension, squeegee profile (rounded or right angled), off contact and squeegee hardness affect the quality of the fill. A manufacturer must make adjustments in these process parameters depending upon via aspect ratio. Often, several test panels must be processed in order to dial in the process.

Advantages of screen printing include:

- Vias not requiring fill are kept free of plugging ink
- Well known and easy to control process
- Wide availability of screen printing equipment
- Lower capital cost when compared to other options

Disadvantages are:

- Screen stencil required for each layout
- Stencils require regular paste print clean-up
- Some difficulty printing designs with significantly varying hole diameters
- Aspect ratio limitations-multiple passes to fill vias often required
- No method to evacuate air easily

Vacuum Plugging Application

The latest equipment iteration to gain the largest share of the via plugging market is based on automated vacuum plugging equipment. This equipment is designed to fill holes in printed circuit boards with conductive or non-conductive paste. The hole filling can be applied in through vias and in blind vias. The filling from blind holes is possible in a double sided mode in one step. The machine is equipped with a glass cover for visual quality control on both panel sides.

Functionality

Once the printed circuit board in vertical position has been hung upon pins, the door is closed and the vacuum process started. The vacuum builds up after about 30 seconds. The filling process begins with the paste being pressed out of a cartridge into the bores while the squeegee is moved over the printed circuit board. Both the kiss pressure of the filling heads to the printed circuit board and the filling pressure are adjustable. The vertical motion is realized by an adjustable servomotor. If there are still some hole voids, the operator can replug the same printed circuit board. That's the great advantage when "plugging under vacuum".

The paste is kept in refillable cartridges. Subject to the printed circuit format, different squeegee sizes are available.

Advantages of this option are:

- Use of controlled paste pressure and flow rates for the paste
- Ability to adjust vacuum to insure optimum fill
- Ability to fill through holes and blind vias at the same time
- Up to 24:1 aspect ratios can be filled

The major disadvantage is the capital cost of the equipment. Capital expenditures for most operations would include the purchase of a vacuum plugging machine and a planarizer. It is estimated that these costs could easily exceed $150,000 US. However, the versatility of the latest vacuum plugging type equipment provides the fabricator with the proper tools for filling very high aspect ratio vias as well as meeting high density requirements.

Newer equipment available today is designed to house the epoxy paste in 4 kilogram containers. These containers are strategically placed in a separate chamber contained within the equipment foot print. A high-pressure valve for dispending the paste is located under the traverse within the plugging machine. Paste is pressed from the large container into the cartridge or cartridges. When the cartridge or cartridges are full, the large container press is stopped. Paste is then dispensed using the high pressure valves from the cartridges into the via fill heads.

The large container option has several advantages:

- More controlled dosing of plugging paste to the via fill heads
- Use of a large container for storing the paste and supplying the via fill heads
- No filling from the supplier container into a separate large container. The container from the supplier is used directly, therefore there is less possibility of air entrapment.
- Easy switching back and forth between the large container system and cartridge only

- Ideal for a large volume PWB fabricator or contract via filling service

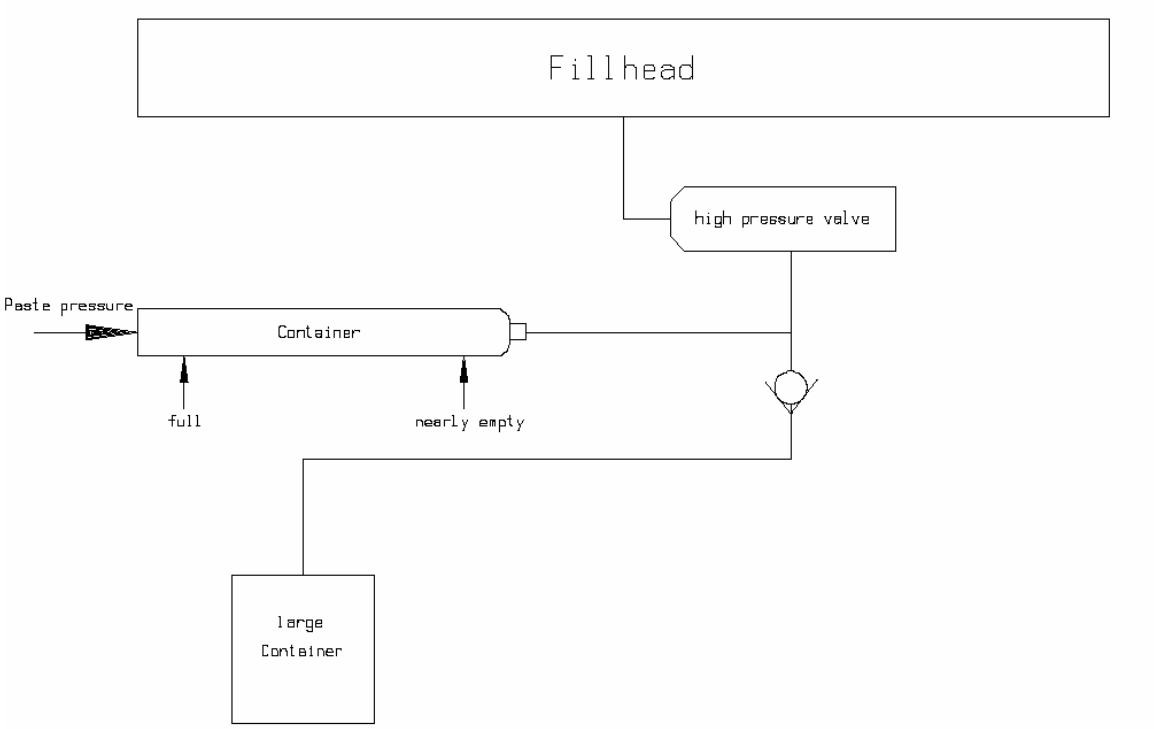

Figure 4-Schematic of the large container paste system.

The latest vacuum filling equipment is equipped with various options that allow the operator to vary critical parameters. Typically, these parameters can be adjusted by the operator to affect an optimal filling process:

- Filling head speed
- Vacuum
- Head pressure
- Scavenger speed
- Scavenger pressure
- Paste pressure

Fabricators must be able to understand the interactions of these parameters in order to determine the best course of action.

Superfilling with Acid Copper Plating

Not to be outdone in the grand stage of via filling, electrodeposition of copper metal into vias has gained acceptance as a consistent means of achieving a solid copper via solution. Again, driven by high density interconnect technology and the need for miniaturization, superfilling of microvias with copper plated metal relies on a thorough understanding of electroplating principles, cell design (including solution agitation and anode placement) and the functionality of organic addition agents. Fluid mechanics play a very important role in determining the extent of filling power in a blind via. Since a typical circuit board design may include through holes in addition to the blind vias, the fabricator must consider mass transfer and ohmic resistances in addition to fluid flow. As aspect ratios increase either due to increased PWB thickness or decreased via diameters, ohmic resistance increases. Thus, increases in ohmic resistance negatively influence throwing power in the through-hole vias. The authors consider this a serious issue and will address it throughout this paper.

Discussion of Key Plating Parameters Involved in Superfilling

Acid copper baths used for plating of PWBs consist of copper sulfate, sulfuric acid and chloride along with organic additives that function as brighteners, carriers (or suppressors) and levelers. In general when we are plating PWBs we use high throw formulations to improve throwing power into small holes on thick panels. For proper filling of blind vias we need to use formulations that are high filling solutions, which means that they are good at filling the blind vias on the panel without resulting in plating folds and without leaving large depressions. These high filling solutions may or may not be good at providing sufficient copper thickness in high aspect ratio holes. The theory and specific parameters for filling blind vias has been previously discussed. (8) There are three primary considerations to ensuring good filling of blind vias.

The first is the sulfuric acid to copper ratio. In high aspect ratio plating the sulfuric acid is typically 225 g/L and the copper concentration is 15 g/L. Thus the ratio of acid to copper is 15:1. For super-filling solutions the acid and copper concentrations are each 50 g/L, giving a ratio of 1:1. The effect of varying the ratio is shown in Figure 5.

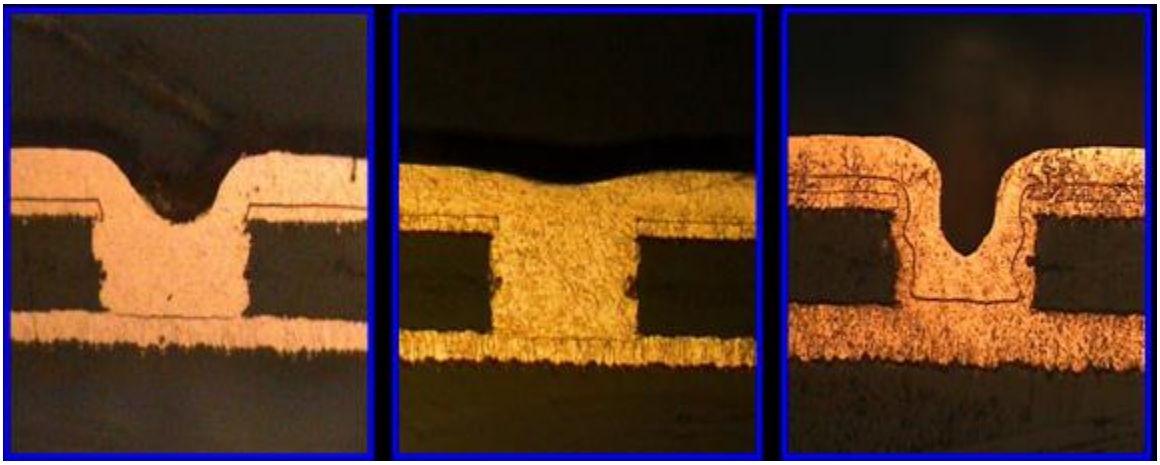

Figure 5 - Effect of Acid Copper Ratio (from left to right - ratios of 2, 1 and 0.5:1)

The second consideration is solution agitation. Solution agitation with bottom eductors tends to provide the most consistent results. Too little or too high of agitation will influence filling ability and throwing power. The eductors are usually spaced on either side of the panels and angled at 15° toward the panels.

The third consideration is plating additives. With high aspect ratio plating brightener and carrier concentration must be adjusted to give satisfactory plating in high aspect ratio holes. With superfilling solutions you have the added consideration of controlling the leveler concentration as well as the brightener to carrier ratio.

Reliability Testing

No discussion on via filling is complete without investigating the reliability of the vias. For this study, IST testing is used to quantify the reliability of vias filled with copper (microvias) and non-conductive epoxy paste (through-holes).

Description of Interconnection Stress Testing (IST)

IST (Interconnection Stress Testing) has emerged as a standard test methodology for the assessment of Printing Wiring Board (PWB) interconnects. IST has the capability of effectively and rapidly quantifying the integrity of the Plated Through Hole (PTH) and Blind Via (BV). In addition, IST is able to identify the presence & levels of post separations within the multilayer board (MLB). IST both complements and/or dramatically reduces the level of microsection analysis required for PWB interconnect quality assessment.

Interconnect Stress Testing (IST) was developed during the 1990s and has proven an invaluable tool with which to rapidly quantify interconnect reliability. This technique was necessary to help the authors understand and articulate the performance of vias that have been filled versus those that were unfilled. The research described herein furthered the understanding of the change in via life when subjected to multiple thermal excursions. In addition, by instituting preconditioning cycles at 230°C, the authors were able to assimilate lead-free assembly. The data generated through this testing program allowed the authors to quantify the effects of both tin-lead based and lead-free assembly on the reliability of filled and unfilled vias.

IST testing utilizes special test equipment to measure cycles to failure (CTF) on specially designed IST coupons placed on PCB fabrication panels. These IST coupons contain daisy chains of plated vias that are thermally cycled using ohmic heating (i.e., by using an internal resistance heater circuit) until failure which is defined as a 10% resistance increase of a plated via daisy chain. The IST test equipment has a number of advantages, including: a quick cycle time of 5 minutes per cycle or 288 cycles per day, the ability to thermally cycle IST coupons at assembly temperatures including lead-free peak temperatures at 260^{o}C, and the ability to obtain quantitative data on plated via CTF.

Test Vehicles

The test vehicles used were designed by PWB Interconnect Solutions (Ottawa, Canada). The GT 40800D vehicle (Figure 6) was chosen to measure PTH and interconnect integrity for paste filled versus non-paste filled vias. This coupon is designed on two independent grid sizes, .040” (1mm) and .080” (2mm). The maximum hole/pad size for the .040” (1mm) grid is .015”

(.38mm) drilled and pad size is .028" (.7mm), on both power and sense circuits. The maximum hole/pad size for the .080" (2mm) grid is .056" (1.42mm) drilled and pad size is .068" (1.73mm), on the power circuit. The geometries for the sense circuit on the .080" (2mm) grid are usually consistent with those used in the .040" (1mm) grid. Drilled hole sizes for this vehicle were 0.35 mm. Board thickness was 1.6 mm. All internal and outerlayer foil was 1 oz.

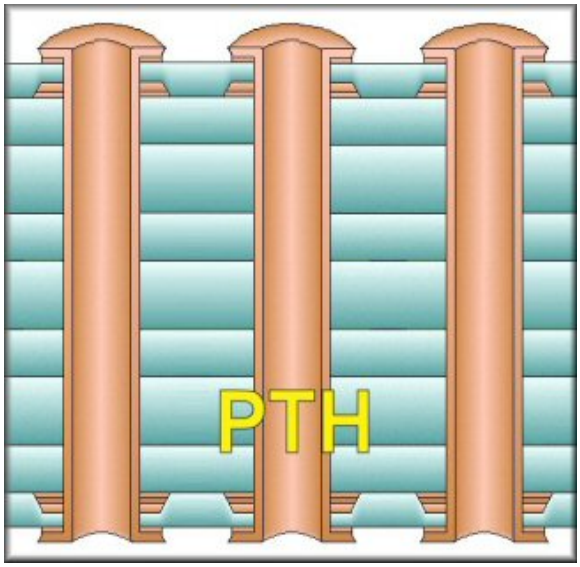

Figure 6 - Schematic of GT 40800D IST Test Vehicle

The schematic of the test vehicle used to test copper via filling is shown in Figure 7. This test vehicle is comprised of both through holes and blind vias. Panel thickness is 2.8 mm (0.110") with through hole diameters of 0.35 mm (0.014"). Microvia dimensions are 0.10 mm wide by 0.09 mm deep (0.004"x0.0035").

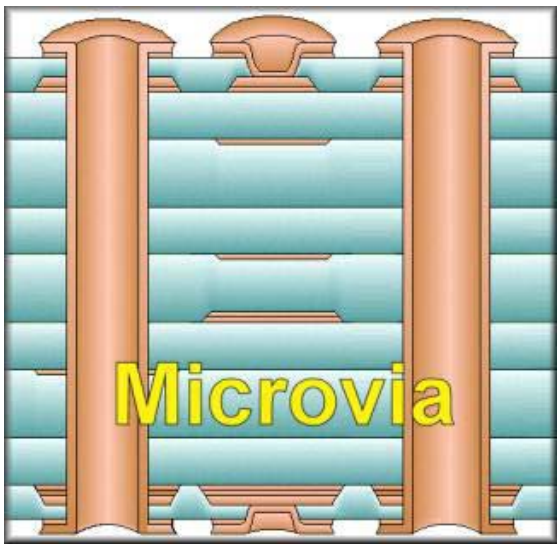

Figure 7 - Schematic of GM 40001A IST Test Vehicle

Paste Fill Testing and Results

For this study, the experimental conditions were as follows:

- One IST coupon design
- Paste filled versus non-paste filled vias
- Pre-conditioning at 230° C versus no preconditioning

The test vehicles were split into two separate lots. One lot was chosen to have the vias filled with an epoxy ceramic filled paste material (non-conductive). A via filling machine similar to the one shown in Figure 8 was used to carry-out the filling process. The second set of panels (identical to the part number used for via filling) was not filled with any material. Also,

one-half of each of the test vehicles was chosen for 230° C conditioning. The conditioning step is performed to assimilate lead-free assembly temperature excursions. The preconditioning often accelerates the failure mode.

Figure 8 - VCP Vacuum Via Plugging Machine-Mass GmBh

The results of the IST testing comparing paste filled and non-filled vias are shown in Table 1 and Table 2.

Table 1 - IST Results With No Pre-Conditioning

Fill Type	Post Cycles	Post %	PTH Cycles	PTH %	Fail Mode
Paste Fill	**1000**	1.3	**1000**	4.2	Accept
Paste Fill	**1000**	0.3	**1000**	1.2	Accept
Paste Fill	**1000**	1.1	**1000**	7.9	Accept
No Fill	**N/A**	0	**908**	10	PTH
No Fill	**N/A**	-0.1	**870**	10	PTH
No Fill	**1000**	0.1	**1000**	0.5	Accept

Table 2 - IST Results With Three Pre-Conditioning Cycles

Fill Type	Post Cycles	Post %	PTH Cycles	PTH %	Fail Mode
Paste Fill	**N/A**	0.5	**714**	10	PTH
Paste Fill	**N/A**	1.3	**669**	10	PTH
Paste Fill	**N/A**	7	**377**	10	PTH
No Fill	**202**	10	**N/A**	2.2	Post
No Fill	**N/A**	0.3	**543**	10	PTH
No Fill	**N/A**	1.1	**675**	10	PTH

Data Analysis of Paste Fill Test

A Box Plot showing the results of the filled versus unfilled vias (no conditioning and conditioning) is shown in Figure 9.

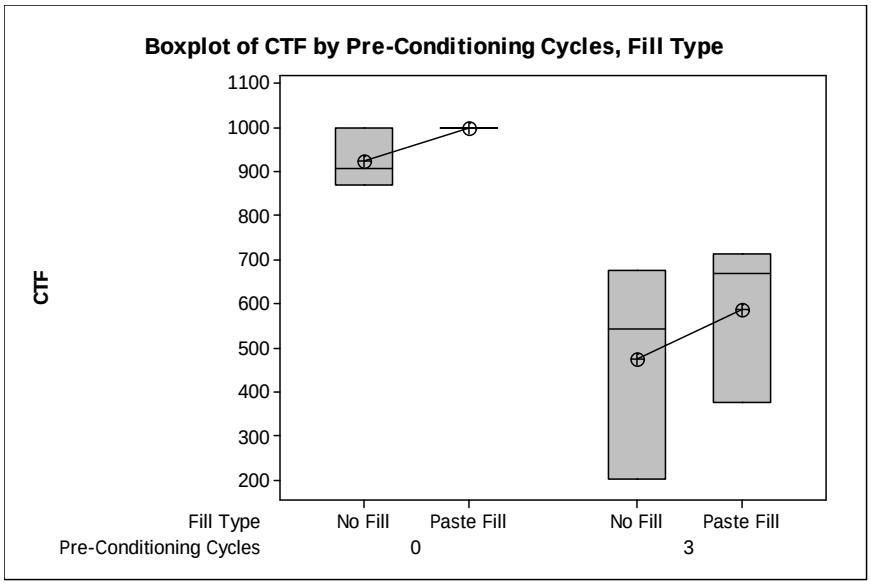

Figure 9 - IST Cycles

Statistical analysis of the data was limited due to the small sample size and due to the fact that the testing was stopped at 1000 cycles if the coupon hadn't failed by then. Two way analysis of variance (ANOVA) was performed and results are shown in Table 3.

Table 3 - Two Way ANOVA Table

Source	DF	SS	MS	F	P
Pre-Conditioning	1	562467	562467	23.07	.001
Fill Type	1	26320	26320	1.08	.329
Interaction	1	1160	1160	0.05	.833
Error	8	195033	24379		
Total	11	784981			

Results showed that, as expected, pre-conditioning significantly reduced the number of cycles to failure. There was not sufficient data to show that the plugged vias were superior, although the As Received samples indicate that plugged vias are more reliable and the difference may be statistically significant with a larger sample size and if the samples were cycled to failure.

Acid Copper Via Fill Testing and Results

For the acid copper superfilling of vias the panels were plated so that through holes had a minimum copper thickness of 25 microns (1 mil). We then ran IST testing on through vias and on blind vias. Three pre-conditioning cycles at 230°C were used for all of the tests. Results for through and blind vias are shown in Tables 4 and 5 respectively.

Table 4 - IST Results for Through Vias

Coupon ID	Post Cycles	Post %	PTH Cycles	PTH %	Fail Mode
1	N/A	0.4	578	10	PTH
2	N/A	0.7	338	10	PTH
3	N/A	1	441	10	PTH
4	N/A	-0.2	598	10	PTH
5	1000	0.9	1000	7.4	Accept
6	N/A	0	602	10	PTH
Mean	593	0.5	593	9.6	
Std Dev	225.4	0.5	225.4	1.1	
Min	338	-0.2	338	7.4	
Max	1000	1	1000	10	
Range	662	1.2	662	2.6	

Table 5 - IST Results for MicroVias

Coupon ID	Post Cycles	Post %	Microvia Cycles	MV %	Fail Mode
1	947	10	N/A	3	Post
2	807	10	N/A	2.4	Post
3	934	10	N/A	3	Post
4	930	10	N/A	3	Post
5	1000	5	1000	1.3	Accept
6	985	10	N/A	2.3	Post
Mean	934	9.2	934	2.5	
Std Dev	68.2	2	68.2	0.7	
Min	807	5	807	1.3	
Max	1000	10	1000	3	
Range	193	5	193	1.7	

In Table 5, the through holes failed before the interconnects. This is typically what occurs, especially on small holes. The mean CTF of 593 is good for this test vehicle when pre-conditioning is used. Variation is larger than expected and further investigation will be necessary. In Table 6, there were no failures in the microvias and the interconnects held up well. Microvias reaching 1000 cycles is also as expected because microvias see less stress than interconnects. Additional tests will focus on preferentially stressing the microvias to see if we can cause failures.

Discussion of Results

Based upon the testing program, one is prepared to discuss reliability results for via filling through the use of non-conductive polymeric plugging pastes and via filling (for blind vias) through electroplating.

For paste filling the IST data indicates that in both the as received and after conditioning samples the filled vias were equivalent to the non-filled vias. The As Received samples indicate that filled vias are more reliable and the difference would most likely be statistically significant with a larger sample size and if the samples were cycled to failure.

Superfilling of microvias is a reliable process. Care must be taken to ensure plating thickness and quality of plating in the through holes is sufficient to withstand multiple heat cycles. In some cases, depending upon aspect ratio microvias and through holes may need to be plated in separate plating processes.

Summary and Conclusions

High Density Interconnect Technology requires fabricators to process PWBs with increasingly tighter spacing, very fine pitch including via in pad technology and blind and buried vias. Such a technology shift necessitates the need to fill these vias with either a high temperature stabile, low CTE via filling paste or in the case of blind vias, filling with acid copper as an alternative. Via filling with polymeric paste is gaining larger market shares each month as more designers require builds with filled or plugged vias. The equipment and the materials are available to enable a successful conversion to this technology. In addition, the data supports the fact that filled vias are at least as reliable as unfilled vias.

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