# A Study of 0201's and Tombstoning in Lead-Free Systems, Phase II Comparison of Final Finishes and Solder Paste Formulations

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**Abstract**
Tombstoning, the phenomena where a chip component stands up on one end during the reflow cycle, is well-documented and understood in tin-lead systems. It is reported to occur more frequently in lead-free systems, and smaller components are at greater risk than larger ones.

A comprehensive DOE was undertaken to characterize tombstoning of 0201 components in different metallurgical solder systems. Factors included pad geometry, board finish, stencil geometry, solder paste type, print and placement offsets, and reflow profile and atmosphere. The experiment was divided into two phases; the results of Phase II are analyzed and reviewed in this document.

**Key Words:** Lead-free, miniaturization, tombstoning, reflow, 0201 components

**Introduction**
Tombstoning is a defect mode that has caused yield fallout since the very beginning of SMT assembly. Also known as "drawbridging" or "the Manhattan effect," it is the phenomena where a chip component seems to stand up on its end during the reflow soldering process.

The mechanics of tombstoning are based on the wetting forces of molten solder and the mass and geometry of the component. If the solder paste under one termination melts and starts wetting to the termination before the other side does, the force applied by the wetting action can pull that component up on its end. Typically, the smaller and lighter the component is, the more susceptible it is to tombstoning.

Factors in tombstoning can be classified into two main categories: design-related and process-related. Design-related factors would include pad design, pad definition (mask or metal), thermal balance between pads or unfilled microvias in the pads. Process-related factors are numerous, and often difficult to quantify. Many DOEs have been performed and published on the topic, often focusing on best practices for both design and assembly.

Most 0201 assembly processes were optimized prior to the transition to lead-free processing. The increasing production of lead-free products and the tighter process windows associated with lead-free now dictate a reassessment of the key parameters that can affect tombstone formation.

**Experimental Design**
After review of previously published studies and high-volume production experiences, a listing of factors that can influence tombstone defects resulted in 49 potential parameters. The investigators then used a C&E Matrix approach (rating influence

0, 3 or 9) to identify the 12 most influential parameters, and developed two DOEs to capture their effects. Parameters included:

- Padstacks. This includes pad sizes and spacing between pads. All pads were non-solder mask defined (NSMD), and did not have solder mask between the pads. Four sizes were considered. Three are considered public domain; the fourth is considered proprietary. In Phase 1, all 4 padstacks were used. In phase 2, the pad stack that performed the worst in phase 1 was used (IPC-L), as was the proprietary design.
- Solder Paste Volume. Stencil apertures were designed at 70% and 100% area of each pad size. 70% area represents the least acceptable transfer efficiency; 100% area represents the best possible transfer efficiency. For the feature sizes used in this study, apertures designed at 70% released about 50% of the paste from the apertures, and apertures designed at 100% released about 60%. The transfer efficiencies vary with each solder paste and the different apertures' area ratios. Both volumes were used in both phases of the DOE.
- Print offsets. To simulate alignment error, stencil apertures were designed at nominal pad position and with 0.1mm (4 mil) offsets in both X and Y directions, for a total of four combinations: (0,0; 0,0.1; 0.1,0.1; and 0.1,0.1). Prints were offset by the same amounts and in the same directions in both phases of the DOE.
- Component type. Both resistors and capacitors were used to capture the effects of component height and number of sides per termination. Both component types were used in both phases of the tests.
- Orientation. Components were mounted at both 0 and 90 degrees. Both orientations were used in both phases of the tests.
- Reflow profile. Straight ramp and high soak profiles were used in phase 1. Only straight ramp (worse case) was used in phase 2.
- Reflow atmosphere. Air and 100 ppm N2 atmospheres were applied in the soldering cycles in phase 1. In phase 2, only air was used. Although air did produce less tombstone defects than nitrogen atmospheres in phase 1, it produced more overall defects, including skewed parts and non-wets.
- Placement offset. Components were placed at two positions: their nominal 0, 0 (CAD) position, and a 0.1, 0.1mm (4 mil) offset in both X and Y concurrently. The same offsets were used for both phases of the DOE.
- Solder paste. In Phase 1 of the study, three solder pastes were used: no-clean SnPb, no-clean SAC305, and water washable SAC305. In Phase 2, the number of pastes was expanded to seven. All were lead-free, no-clean pastes. Six of the seven used SAC305 alloy; one used SACX0307 alloy.
- PWB final finish. In Phase 1, organic solderability preservative (OSP) was used. In Phase 2, both OSP and electroless nickel-immersion gold (ENIG) finishes were used.

Tables 1 and 2 show the experimental matrices for both phases of the tests.

| Final DOE Phase 1 | | | | | |
|---|---|---|---|---|---|
| | Levels | | | | |
| Padstack | 4 | A | B | C | D |
| paste volume | 2 | 100 | 70 | | |
| paste off x | 2 | 0 | 0.1 | | |
| paste off y | 2 | 0 | 0.1 | | |
| comp type | 2 | R | C | | |
| rotation | 2 | 0 | 90 | | |
| | 128 | Combinations | | | |
| | 6400 | Parts Placed | | | |
| | | | | | |
| Profile | 2 | HS | SR | | |
| Atmosphere | 2 | Air | N2 | | |
| Place off x | | 0 | 0.1 | | Placement |
| Place off y | 2 | 0 | 0.1 | | 0,0 0.1,0.1 |
| Place off theta | 1 | 0 | | | |
| | 8 | | | | |
| paste | 3 | NC-SnPb | WS-SAC305 | NC-SAC305 | |
| | | | | | |
| boards | 24 | | | | |
| Replication *2 | 48 | | | | |
| | | | | | |
| Parts Placed | 307200 | | | | |

**Table 1. DOE Phase 1 Design Matrix**

| Final DOE Phase 2 | | | | |
|---|---|---|---|---|
| | Levels | | | |
| Padstack | 2 | A | D | |
| paste volume | 2 | 100 | 70 | |
| paste off x | 2 | 0 | 0.1 | |
| paste off y | 2 | 0 | 0.1 | |
| comp type | 2 | R | C | |
| rotation | 2 | 0 | 90 | |
| | 64 | Combinations | | |
| | 3200 | Parts Placed | | |
| Profile | 1 | SR | | |
| Atmosphere | 1 | Air | | |
| Place off x | | 0 | 0.1 | Placement |
| Place off y | 2 | 0 | 0.1 | 0,0 0.1,0.1 |
| Place off t | 1 | 0 | | |
| Final Finish | 2 | OSP | ENIG | |
| paste | 7 | NC-SAC305 | NC-SACX | |
| | | | | |
| boards | 28 | | | |
| Replication*2 | 56 | | | |
| | | | | |
| Parts Placed | 179200 | | | |

**Table 2.** DOE Phase 2 Design Matrix

The factors listed in the top portions of tables are designed into the test vehicle shown in Figure 1. The factors in the bottom half of the tables were varied during the assembly process.

**Test Vehicle**

The test vehicle shown in Figure 1 contained 48 individual test cells. Four different pad designs were used, each appearing twelve times on the test vehicle, six times per row of cells on two rows. Each cell had 50 resistors and 50 capacitors oriented at both 0 and 90 degrees for a total of 200 per block, as shown in Figure 2. Eight cells per padstack were assembled per board, for a total of 1600 placements per padstack per board. In phase 1, all four padstacks were used, resulting in 6400 components placements per board. In phase 2, only footprints A and D were used, resulting in 3200 placements per board.

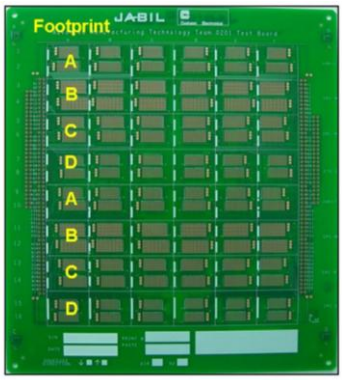



**Figure 1. 0201 Test Board Layout. Each row has six test cells. Eight rows duplicate four footprints two times.**

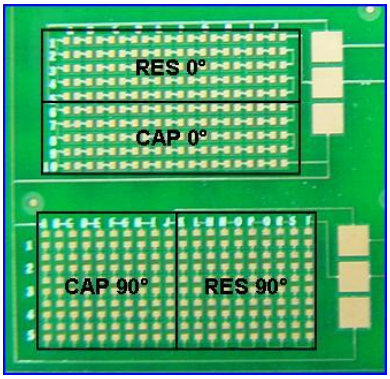



**Figure 2. Individual test cell. Each test cell has 50 capacitors and resistors oriented at 0° and 50 of each component type oriented at 90°.**

**Stencil Design**
To achieve all the combinations of aperture reductions and offsets in a single print, the following modifications were made to the stencil design. Moving left to right, of the six columns of test cells, the first two columns had apertures reduced to 70% of their pad area, the middle two columns were not populated, and the last two columns had no aperture reductions applied. Within each group of aperture reductions the test cells were divided into 4 segments, with each segment having a different aperture alignment offset.

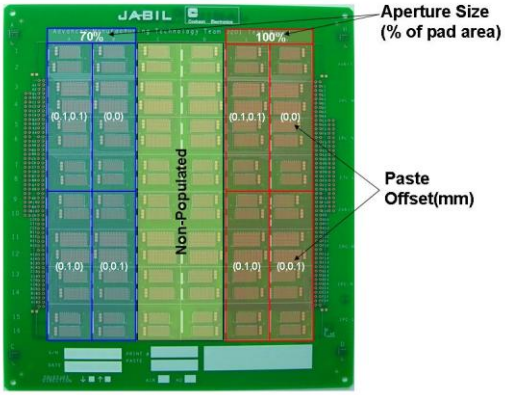



**Figure 3. Stencil design modifications**

Using the design shown in Figure 3, each combination of padstack design, aperture reduction, and alignment offset appears twice per board. Two replicates were used, so each combination was assembled in four test cells. The same stencil was used in both phases of the test.

**ASSEMBLY**
Upon receipt of the components, samples were inspected, which included dimensional measurements and XRF screening to insure lead was not present in the system.

All test vehicles were assembled in the Advanced Manufacturing Technology laboratory of Jabil Circuit in St. Petersburg, FL using the following equipment:

- MPM Ultraprint 3000 stencil printer
- Koh Young KY3030-VAL paste measurement system
- Fuji AIM pick and place
- Vitronics-Soltec XPM$^2$ reflow oven
- Vi Technology Vi3K$^2$ automated optical inspection
- Phoenix Nanomex X-ray inspection

Details of the assembly process development are described below.

**Stencil Printing**
The investigation included high and low paste volume settings. In order to achieve two levels of paste volume, the stencil apertures were reduced. To identify the most appropriate aperture reduction, a prescreening study was performed. Stencil apertures were sized at 100%, 80% and 60% of their corresponding pad areas for all four footprints. It was determined through the prescreening DOE that 70% pad area, or 30% reduction, would be appropriate for the low setting. 100% pad area and 70% pad area equate to transfer efficiencies of roughly 60% and 50% respectively, and varied slightly with the individual solder pastes and aperture designs.

The stencils used in the study were electroformed nickel with 125 micron (5 mil) foils. All solder pastes were printed at the same parameters: 2 inch/sec squeegee speed, 1.25 lb/in squeegee pressure, slow separation speed.

**Paste Volume Measurement**
The Koh Young KY-3030VAL solder paste inspection system was used to measure paste volume deposition in all phases of the experiment. This proved to be especially useful in the pre-screening experiment to determine the appropriate aperture reduction to apply to the stencil design.

The equipment employs a proprietary Phase Shift Profilometry (PSP) algorithm using a moiré light projection technique. This technique uses opposing dual source LED lighting to capture 8 images (4 from each side) for every solder deposit.

Using a reconstruction algorithm, the 8 images are combined to form a 3D model of the solder deposit. The dual source lighting technique is advantageous because it reduces the shadowing effect associated with single light source systems. With a pixel size of approximately 20um x 20um, it is very important to have the most accurate information possible, particularly with the 0201 deposits in the size range of 10-19 mils.

To ensure system capability, a rotational Gage R&R was performed using Minitab's crossed ANOVA method. The Total Gage R&R figure needs to be below 30 in order for the system to be used as an acceptable measurement instrument. Using a process tolerance window of +/-25%, the Total GRR for the test vehicle was around 20, with a repeatability figure below 3.

The cycle time for the equipment to measure nearly 20,000 solder deposits was approximately 55 seconds.

**Placement**

The Fuji AIM board assembler is a two gantry, 4 head placement machine that handles devices from 0201s to 74 mm square. It has 180 feeder inputs and can feed from tape and reel, strip tape, sticks, and matrix trays. Its speed is rated at 20,300 chips per hour.

The machine was installed in the laboratory and calibrated prior to the test. A GR&R study was not performed prior to the test.

**Reflow Soldering**

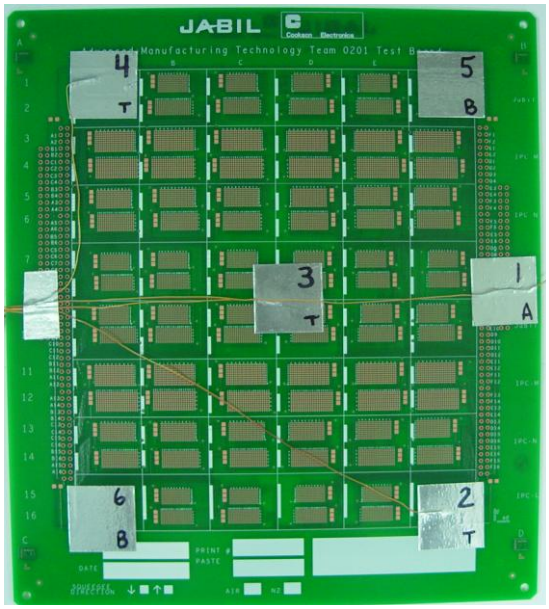



**Figure 4. Thermocouple attachment. Locations 1 though 4 are on the top side; 5 and 6 are on the bottom side.**

Six thermocouples were used to profile the assembly. Four were attached to the top side; two were attached to the bottom side as shown in Figure 4.

The reflow profiles depicted in Figure 5 and Figure 6 were developed on unpopulated PWBs.

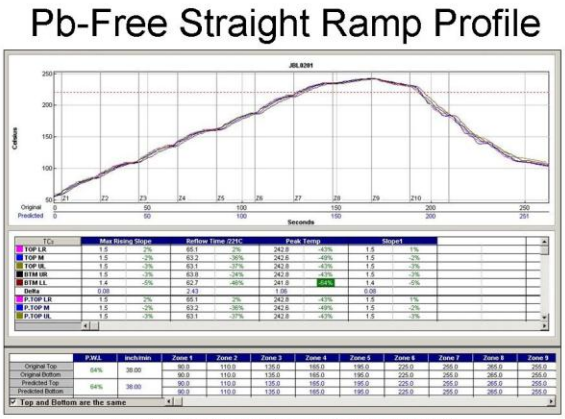



**Figure 5. Straight ramp profile, SAC 305**

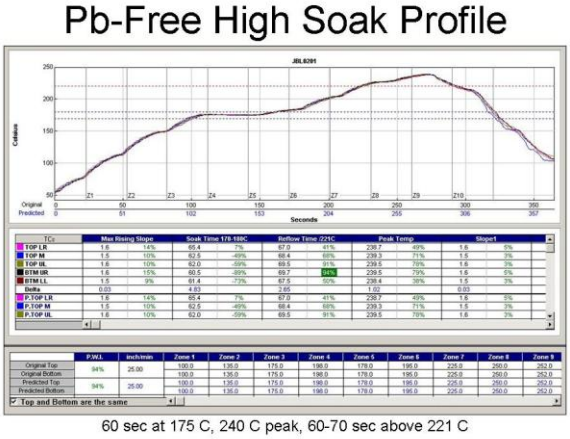



**Figure 6. High soak profile, SAC 305**

**Automated Optical Inspection**

The Vi Technologies Vi3K2 AOI system was used to inspect boards pre- and post-reflow. Starting from the same CAD information, both programs were generated using the equipment manufacturer's standard library. The machine combines high end optics and hardware with software technologies such as vectoral imaging and sub-pixelization to provide accuracy and repeatability that allows Automated Optical Measurement (AOM). In the data presented below, the system was used to detect full and partial tombstones, and positional errors in X, Y, and theta. For this test, the equipment was installed and calibrated by the manufacturer; a GR&R study was not performed prior to the execution of the experiment.

**X-Ray Inspection**

The Phoenix Nanomex X-ray machine was used to inspect for solder balls. PWBs were X-rayed, the resulting images were visually interpreted, and the solder ball count was manually recorded for each quadrant of the PWB. Solder ball defects were recorded for each PWB, but not uniquely associated with individual components.

**DATA COLLECTION**

Defects were classified as:

- Full tombstones, where the component stands completely up on one end at approximately a 90 degree angle to the plane of the PWB.
- Partial tombstones, also known as drawbridges, where the component is soldered at one termination but not at the other and stands at an angle between 0 and 90 degrees to the plane of the PWB
- Non-wets, where the component remains planar to the board surface, but the solder has not adequately wetted to one or both of the terminations.
- Positional errors, where one or both component terminations are offset from the edge of the pad by greater than 50% of the termination width in x, y, or theta.

- Solder balls, or spheres of solder that remain after the soldering process. The minimum size recorded was that which was visually perceptible on X-ray images, approximately 75 to 100 microns (3-4 mils) in diameter. Workmanship criteria such as locations relative to the components or levels of encapsulation were not recorded.

Examples of the defect modes are depicted in Appendix A.

**RESULTS & DISCUSSION – Phase II Data**

Phase II used some of the worst case conditions: the smallest pad stacks with a straight ramp profile in an air environment. While this helped to differentiate performance factors among solder pastes and PWB final finishes, it did raise the overall defect rate. In phase I, the average defect rate (excluding solder balls) was 7,845 ppm, whereas in phase II the overall defect rate was 26,814 ppm. Due to the difference in input parameters and overall defect rates, the bulk data sets should not be directly compared. The subset of phase I data that shares equivalent input parameters with phase II will be analyzed and reported separately.

In phase I, defect rates were originally analyzed with the inclusion of solder balls as defects. Depending on their size and location, solder balls may or may not be considered defects, but regardless of their quality status, their formation during the reflow process can be considered a performance indicator. In Phase I they occurred as frequently as the top defect mode, and their inclusion in overall results was sometimes misleading. In some cases, solder balls were the most common defect mode, and parameter sets that minimized solder balls maximized other defects. Phase I defects were eventually calculated and reported with and without solder balls.

The phase II data analysis was performed without the inclusion of solder balls because excluding them significantly improved the fits of the statistical models. Another departure from the phase I analysis methods was to use all soldering defects as the response variable instead of tombstones only. In phase I, the top factors that were reported were those that had the largest effect on tombstone defects, not all soldering defects. The difference between the analysis methods is extremely subtle, as the general trend in phase I was that input parameters which minimized tombstones also minimized all other soldering defects. This change was implemented because, in practical terms, any of the five soldering defects recorded require similar amounts of rework with similar costs and associated risks. Overall process optimization requires mitigation of all the defects listed.

**Defect Overview**

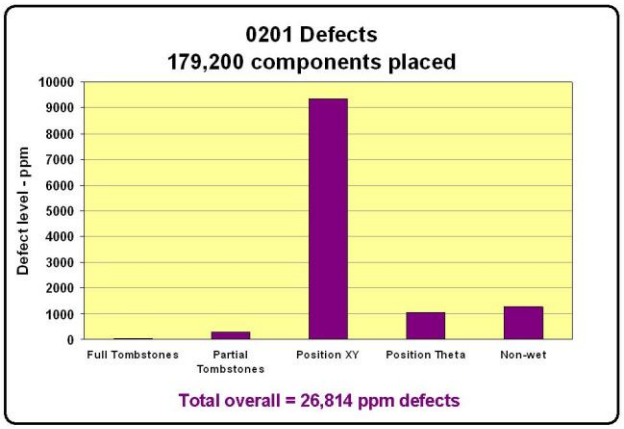



**Figure 7. Distribution of all defects**

Phase II of the experiment placed 179,200 components and had a defect rate of 26,814 ppm. As shown in figure 7, the vast majority of the defects modes are positional errors in the X or Y axis, at 9432 ppm. The next largest effect was non-wets, at 1278 ppm, nearly an order of magnitude smaller. A positional error is a situation where the component termination overhangs the edge of the pad by more than 50% of the termination's length or width.

The top four factors in defect creation were component type, solder paste formulation, component orientation, and pad stack.

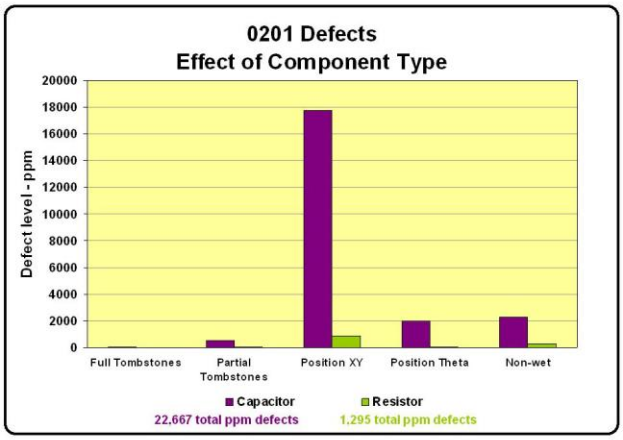



**Figure 8. Effect of component type**

Component type was the largest factor influencing defect rates. Figure 8 illustrates the difference between capacitors and resistors, with roughly 95% of all the defects associated with capacitors.

Component Dimensions

mm

| Comp Type | X | Y | Z | Lead length | Lead width |
|---|---|---|---|---|---|
| C | 0.27 | 0.53 | 0.26 | 0.12 | 0.26 |
| R | 0.26 | 0.58 | 0.21 | 0.15 | 0.27 |

mils

| Comp Type | X | Y | Z | Lead length | Lead width |
|---|---|---|---|---|---|
| C | 10.8 | 21.1 | 10.3 | 4.8 | 10.2 |
| R | 10.3 | 22.7 | 8.2 | 5.9 | 10.6 |

**Table 3. 0201 component dimensions. Ten of each component type were measured and average values are shown.**

The main differences between capacitors and resistors are their heights (table 3) and termination geometries (figure 9). Capacitors are 25% taller than resistors, have a higher center of gravity, and offer more wettable surface area in contact with the solder paste.

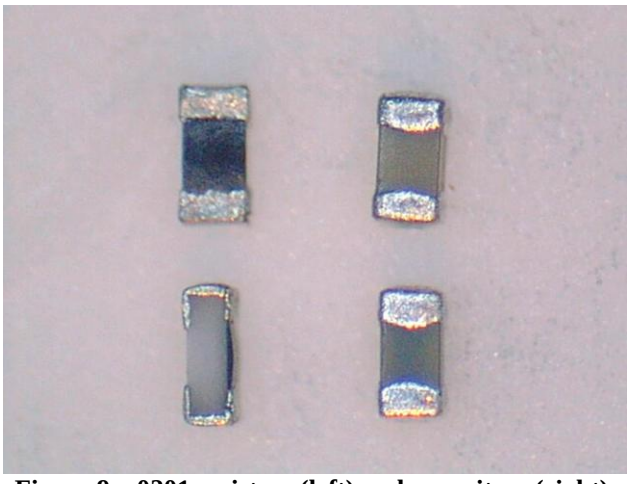


**Figure 9. 0201 resistors (left) and capacitors (right).**

**Effect of Solder Paste Formulation**

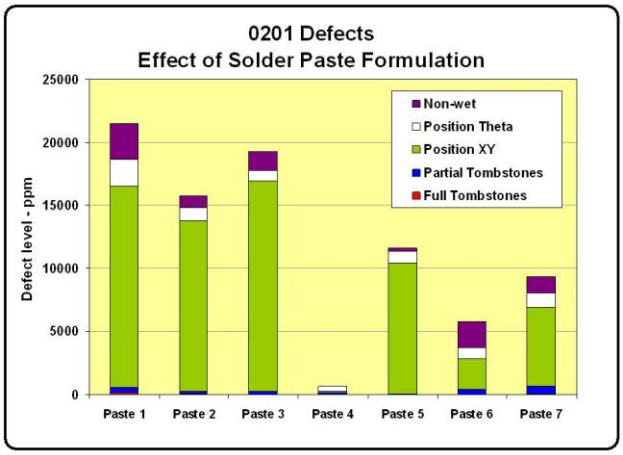



**Figure 10. Effect of solder paste formulation**

Of the seven solder pastes used, defects varied from 664 ppm to 21,445 ppm. All solder pastes (1 through 7) were no-clean products, each with a different flux formulation. Pastes numbered 1 through 5 used SAC305, type 3 solder powder. Number 6 was a SACX0307, type 3 product, and number 7 was a SAC305, type 4 powder.

**Effect of Component Orientation**

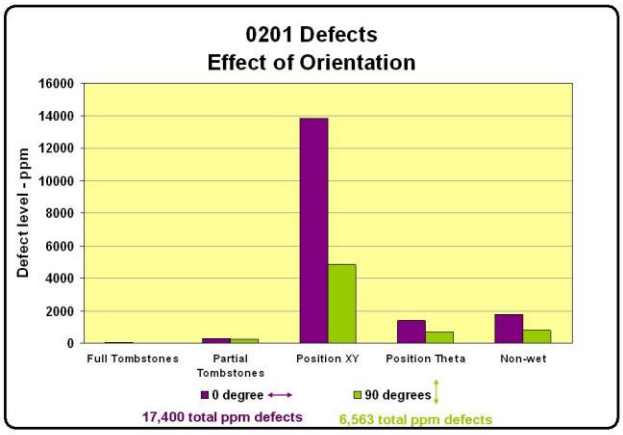



**Figure 11. Effect of component orientation**

The third most considerable effect was that of component orientation with respect to direction of travel through the reflow process. Components oriented at 0 degrees, or parallel to the direction of travel through the oven, exhibited a defect rate of 17,400 ppm, while components oriented at 90 degrees, or perpendicular to the direction of travel, exhibited a defect rate of 6563 ppm. The results are shown in figure 11.

The components oriented perpendicular to the direction of travel showed far fewer defects than those oriented parallel to the direction of travel, presumably due to thermal gradients across the component. When a component is oriented at 90 degrees, both terminations enter reflow at approximately the same time. When a component is oriented at 0 degrees, the leading termination enters reflow before the trailing termination.

**Effect of Padstack**

One of the padstack designs was IPC-L, in which each pad measures 0.3mm square with a gap of 0.25 mm between them. The dimensions of the other padstack are considered proprietary, so discussion of the results is limited to the general trend. IPC-L, the smaller of the two footprints, produced more defects than the larger one, particularly when capacitors were placed on them.

**Effect of PWB Final Finish**

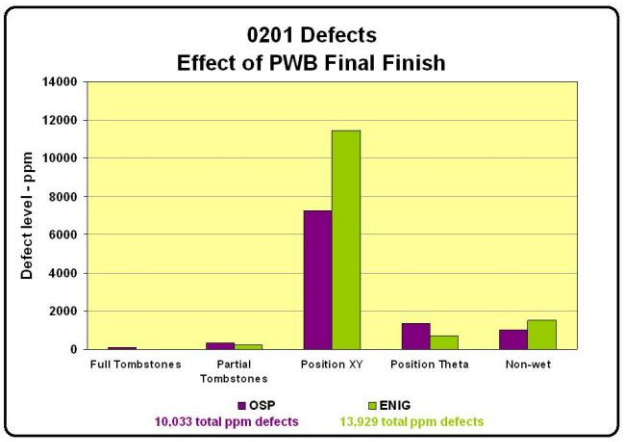



**Figure 14. Effect of PWB final finish**

PWB final finish was not one of the top five factors in defect formation, but its effect was significant. ENIG finishes produced roughly 40% more soldering defects than OSP finishes. Defect rates were 10,033 ppm on OSP and 13,929 on ENIG. The breakdown of defect modes is shown in figure 14.

**CONCLUSION**

The conditions that were varied in this phase of the experiment were component type, padstack, paste volume, paste offset, placement offset, solder paste formulation and PWB final finish. Reflow profile and atmosphere were held constant: ramp profile and air environment. Only two of the four original pad stacks were used.

The top four contributors to defect generation were component type, solder paste type, component orientation and padstack dimensions.

Final finish was also a factor, with OSP producing 30% fewer defects than ENIG.

**REFERENCES**

The following papers were used as reference documents in the design phase of the experiment:

[1] "Designing a High-Yield 0201 Assembly Process for New Product Introduction", D. Baldwin et al, Proceedings of SMTA International 2002

[2] "AOI: Facing the Challenges of 0201…" JM Peallat & M. Norris, Proceedings of SMTA International 2002

[3] "PCB Design Optimization of 0201 packages for Assembly Processes", Proceedings of SMTA 2002

[4] "Process Characterization of PCB Assembly Using 0201 Packages with Lead-Free Solder", Geiger et al, Proceedings of Telecom Hardware Solutions Conference, 2002

[4] "Conquer Tombstoning in Lead-free Soldering", B Huang & NL Lee, Proceedings of APEX 2004

[5] "Yield Enhancement and Yield Modeling from Mass Reflow Process of 0201 Components", Lu et al, Journal of the SMTA Volume 17 Issue 4, 2004

[6] IPC-A-610D, Acceptability of Electronic Assemblies, IPC, Bannockburn, IL, 2005

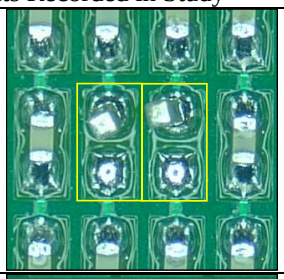
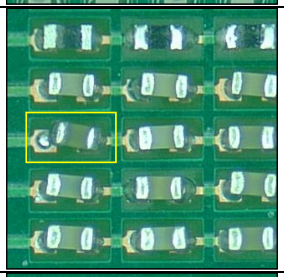
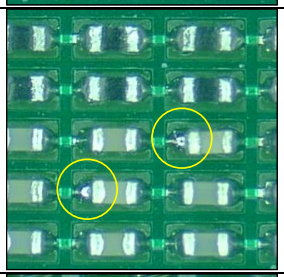
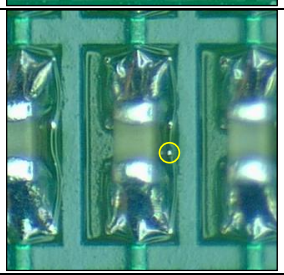
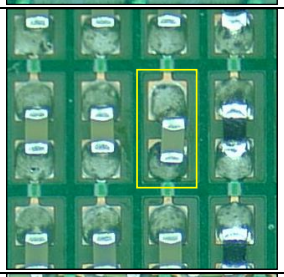
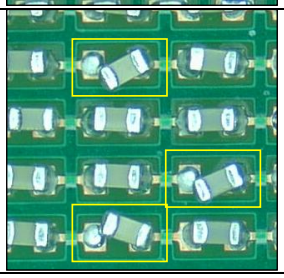
[7] IPC-7351A, Generic Requirements for for Surface Mount Design and Land Pattern Standard, IPC, Bannockburn, IL, 2005

The results from Phase I can be reviewed at:

[8] "A Study of 0201's and Tombstoning in a Lead-free System," Neathway, P., et al, Proceedings of SMTA International, 2007

APPENDIX A

Chip Component Defects Recorded in Study

| | |
|---|---|
| **Full Tombstone** |  |
| **Partial Tombstone Or Drawbridge** |  |
| **Non-wets** |  |
| **Solder Balls** |  |
| **Position X-Y** |  |
| **Position Theta** |  |