Base Material Consideration for High Speed Printed Circuit Boards

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Abstract

Over the years, the EU RoHS restriction and lead-free capability is the hottest environmental protection subject. In technology trends, signal integrity performance gets more critical based upon today's higher signal transmission speed demand in every field of applications such as computer CPU and GPU chipset levels, system operation frequency and a variety of communication bus and cables like PCI express, SATA II and AGP bus for computer systems. Signal communication speed will shift from 1-5 Gbps range up to 5-10Gbps depending on applications. In order to meet lead-free requirements and severe processes conditions with good signal integrity performance, the laminate material will play a more and more critical and sensitive role in the system.

From consumer products to high-end applications, there is a need for certain electrical and thermal performance; it is essential to meet those requirements with cost effectiveness. As a base material supplier, we will hereby discuss material design and factors that influence signal integrity, including epoxy and hardener, resin chemical construction, laminate ply-up construction, amount of resin content, fabric weaving density, moisture pick-up and environment factors etc. for a massive mainstream application and low loss application under the hypothesis of lead-free capability.

Introduction

The IPC international technology roadmap 2006-2007 included a quantitative summary of the expected changes and trends in PC board, component, material and assembly technology from 2006 to 2016 and rank in RCG and SoA two categories for reference. It says that communication clock frequency will increase for E1 to E8 all categories. Take E2 consumer products and E4 mid-range performance application for instance, clock frequency for RCG increases from 130MHz and 1000Hz up to 1000Mhz and 3500MHz respectively in the coming 10 years, and the desired base materials are CEM3 and high performance, RoHS capable FR4.

The demand for low loss material focuses on wireless, high performance, microwave and RoA fields only. Even the backplanes long-term feature assessment is for a dielectric constant of 4.3 and dielectric losses of 0.015 from now till 2016.

The product's operating frequency trend tell us we need a high speed low loss material, however the material trend, on the other hand has shown us that it is not necessary to have a very low Dk/Df material. Why are they conflicting each other? One of key factor is that the advancement of print circuit board manufacturing skill and lay out design technology, like HDI, back-drill and emphasizer etc., can cover the increasing signal integrity requirements. Another reason is reduced signal transmission length for a thinner and lighter consumer product. On top of this, cheap epoxy based material has an electrical

performance near to its maximum limit. Thus the PCB industry enjoys the benefit of well-developed processes and cost structure. Does this mean that the current existing FR4 materials are sufficient for the next 10 years? We believe the answer is yes and no whether you are referring to a lead-free market or signal integrity market.

For each laminate performance segments, it is a big challenge to keep the dielectric constant and dissipation factor as low as possible while being RoHS and lead-free process capable and at a reasonable cost.

We will hereby separate materials electrical performance in three categories, regular FR4 material (Df ~ 0.020), mid-loss material (Df ~ 0.015) and low-loss material (Df ~ 0.010). From here we will discuss what we should know and what we can do to get the best signal integrity performance.

Resin Impact on Signal Integrity

The implementation of RoHS restriction and lead-free soldering process imposes a new challenge for base material which are now expected to withstand about 20~40^{o}C higher assembly temperature. The common solution in the market is to use a phenolic-cured resin systems. Compared with conventional High Tg DICY-cured material, leading phenolic-cured materials perform superior only in thermal performance. Their inferior electrical performances make a negative impression and slows down their usage in signal integrity concern applications. As for modified epoxy laminate, under the category of mid-loss and low-loss; it has a more challenging situation of balancing the thermal and electrical performance.

The laminate resin recipe is composed of an epoxy part and a hardener part. In the market, a variety of basic resin systems are commercialized as shown in Figure 1. The common polymer backbone constructions include bisphenol A, phenol novolac, bisphenol A novolac, bisphenol F novolac, DCPD and cresol novolac, styrene copolymer and triazine etc. with epoxy, amine, anhydride, ester and benzoxazine etc. as end groups for the curing reaction. Unfortunately, suitable and affordable resin systems for high Tg CCL laminate are limited.

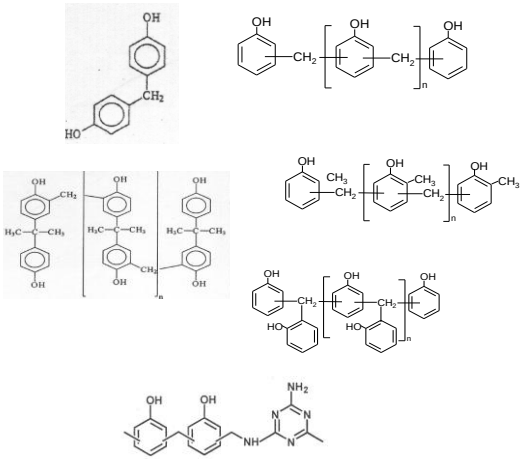
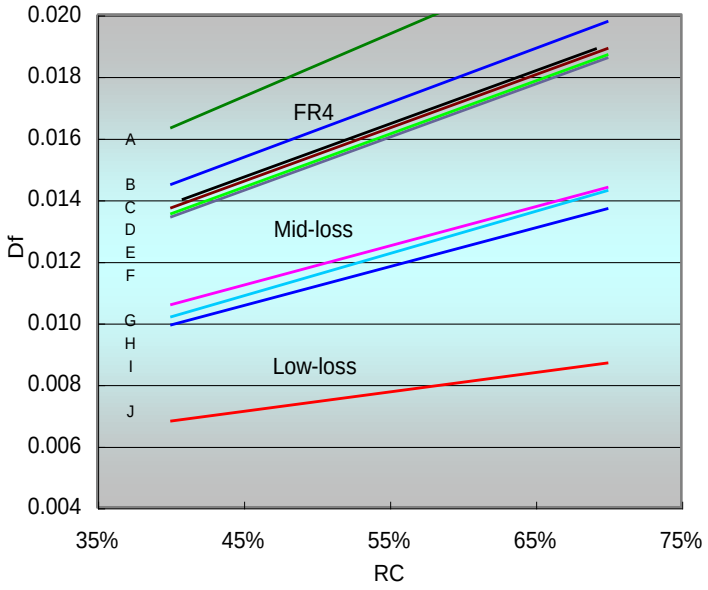


Figure 1 : Common back-bone type for hardener

Figure 2 is a dielectric loss comparison study in terms of base resin system and resin content. Material resin content is one of significant factor for dielectric constant and dissipation factor. Dissipation factor is directly proportional with resin content; however mid-loss and low-loss materials can mitigate the effect of resin content.

Conventional dicy-cured high-Tg systems perform the best in dissipation factor of the regular FR4 category. Here we can easily find that the most common lead-free material is the bisphenol A novolac resin system which shows a much higher dissipation factor than other resin system and the dicy-cured Hi-Tg and phenol novolac base systems which show superior dissipation factor performance compared to the bisphenol A novolac and blended resin system. Is the phenol novolac type resin system the best candidate for the near future? Actually, a formulation using phenol novolac as a major base resin is not processed easily in PCB fabrication and on top of this, it may not lead-free compatible. Generally, from formulation point of view a material's electrical performance and PCB process friendly / lead-free performance go in opposite directions. Currently, EU RoHS restriction is a hot topic and therefore the bisphenol A novolac base system is the mainstream solution in order to have a higher Td, T288 etc. to address the lead-free and PCB process window barrier issue; this requires us to put electric performance aside.



A : bisphenol A novolac system, B : bisphenol A + phenol novolac system, C : TUC mid-Tg material
D : TUC Hi-Tg material, E : Hi-Tg Dicy-cured system, F : phenol novolac system, G : TUC mid-loss material
H : anhydride base mid-loss system, I : BT/Epoxy base system, J : TUC low loss material

Previously we conducted a series of lead-free studies covering the areas of the base resin system, laminate basic properties and PCB processing. The final PC board performances under thermal reliability testing such as TCT and IST were also noted. We found that in order to have a good PCB process window for the low to mid end application, a balanced and moderated basic physical performance of the laminate is important. By selecting a suitable modified novolac-cured system instead of a dicy-cured system because the modified novolac filled system has the most critical performance, we were able to achieve a low alpha one coefficient of thermal expansion with a moderate Td. (However, IPC guidelines suggest that the Td of the material need to be a least 320°C, in order for it to classify under lead free category. And a higher Td implies that the PCB processing window is narrower.)

For better understanding of varies material performance in signal attenuation, we model a 4L board stripline pattern. It was configured with about 4mil line width up 4 inches long difference and the construction has the average resin content 55%. The circuitry was designed with 50 ohm impendence and this follows most high layer count and high speed applications. In order to minimum the noise generated from the through holes and connectors, we reduce the through hole diameter size to 6 mil and used a 20GHz frequency capable SMA connector. Figure 3 shows the board construction and pattern of connection area.

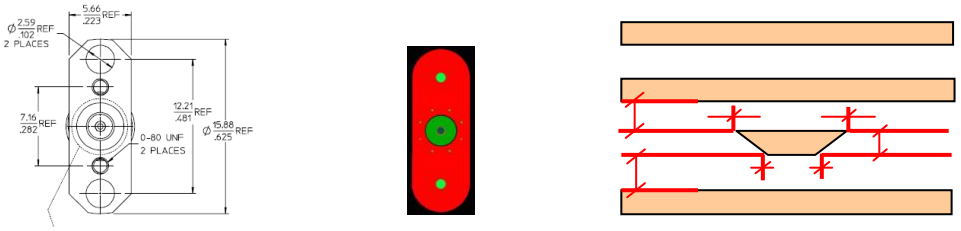


Figure 3 : connector dimension ; board-side pattern ; Test board construction / 4L

Using dicy-cured High Tg FR4 and phenol novolac cured materials as a baseline, the lead free compatible Bisphenol-A novolac base high Tg FR4 material has about 0.083dB/in higher signal attenuation loss at 5GHz as is shown in Figure 4. If we use –3dB to judge the bandwidth with highest frequency without major degradation, leading-edge materials get about additional 1GHz higher bandwidth as Table 1 shows. Now most consumer product, hand held product and mid-range performance system made out of regular FR4 materials need a higher bandwidth with the same cost or lower. Choosing a suitable regular FR4 grade material can effectively avoid upgrading FR4 to mid-loss grade materials and/or reserve more bandwidth for bus and chip components.

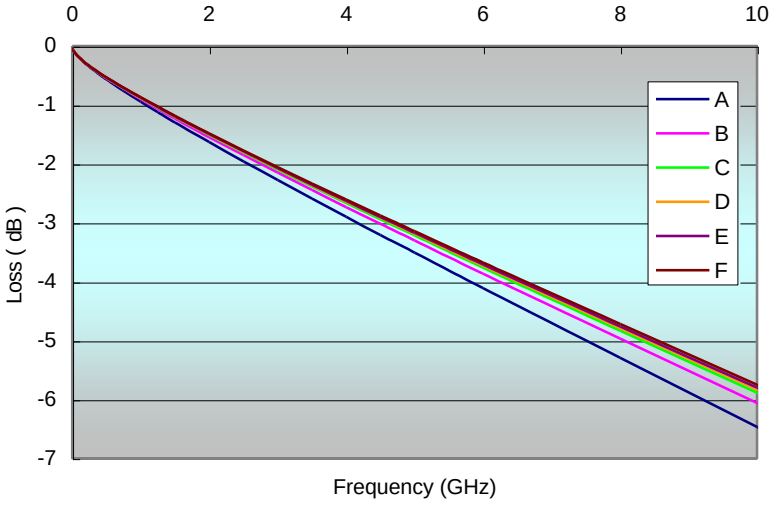


Figure 4 A : phenol novolac system, B : Hi-Tg dicy-cured, C : TUC Hi-Tg material, D : TUC mid-Tg material system, E : bisphenol A + phenol novolac system, F : bisphenol A novolac system

Table 1: Attenuation loss comparison in terms of frequency and materials.

Loss Ratio	A	B	C	D	E	F
1.0 GHz	108.6%	103.7%	101.6%	101.0%	100.6%	100%
3.0 GHz	110.7%	104.6%	102.0%	101.3%	100.8%	100%
5.0 GHz	111.6%	105.0%	102.2%	101.4%	100.8%	100%
BW : -3dB	~4.2GHz	~4.5GHz	~5.1GHz	~5.2GHz	~5.2GHz	~5.2GHz

Another materials category is the mid-loss and low-loss materials. The feature of the market for mid-loss materials shows FR4 level dielectric constant with lower dielectric loss properties. Designers do not need to change the circuit board pattern layout; therefore they gain wider bandwidth directly.

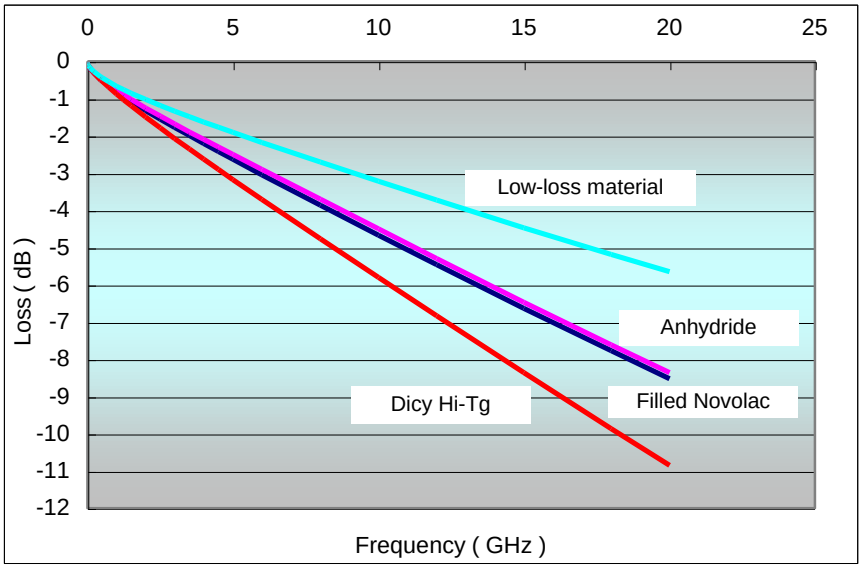


Figure 5: Attenuation loss comparison for different grade

Figure 5 is another comparison chart for two different grade materials. The pattern design is the same as previous case and has a stripline construction with 50 ohms impendence.

Table 2 : Transmission length for different resin system

Mat'l / -3dB	3GHz	5GHz	8GHz	BW
Dicy Hi-Tg	5.6 in	3.7 in	2.4 in	5.2GHz
mid-loss : Filled Novolac	6.7 in	4.5 in	3.1 in	5.9GHz
mid-loss : Anhydride	6.9 in	4.6 in	3.1 in	6.2GHz

The two mid-loss two materials reduce signal loss by about 0.16dB/in at 5HGzand gain an additional ~1GHz bandwidth and transmission length in terms of frequency versus the leading FR4 materials as shown in Table 2.

Although mid-loss anhydride cured system and modified novolac filled mid-loss resin system get similar signal integrity performance, the modified novolac filled system have an advantageous position in thermal properties like lower thermal expansion and higher decomposition temperature etc. As we know, low CTE is one of critical material factor for IST and TCT long-term reliability. Refering to IPC roadmap material's trend, filled novolac epoxy are expected to be the mainstream for E4 mid-range and E5 high performance applications. Besides that, modified novolac filled system possess competitive resin cost construction for mid-loss range application.

Copper Foil Type Impact on Signal Integrity

Circuit Rdc and Rac resistance make up conductor loss. Dielectric loss and conductor loss are the two parts of overall attenuation. The Rdc is related to circuit geometry and the Rac skin effect corresponds with frequency. The following equation can provide more clear idea.

Attenuation = dielectric loss + conductor loss
= loss cause by base material + loss cause by circuit trace
= material Dk / Df + circuit geometry and roughness
= 2.3 * freq (GHz) * Df * sqrt(Dk) (unit : dB/in, [1])

Therefore attenuation is a complex overall result in terms of frequency. The skin effect term dominates the attenuation in the low frequency range and the dielectric loss start to dominate attenuation in the high frequency range. The crossover dielectric loss domination point depends on the combination of materials performances and circuit patterns.

To judge the influence of skin effect foil roughness we fabricated two identical test boards made of low-loss material. One was constructed with standard HTE roughened foil while the other was constructed with reverse treated smooth foil. For smooth foil construction another option is VLP or "very low profile" grade foil. However this is not a common grade in the industry and can't reflect the actual attenuation performance in application. Result show that choosing a right copper foil is a key factor to reduce signal loss as Figure 6 demonstrates. Test boards with roughened foil had an increased loss level of 0.03dB/in versus smooth foil under the same 5GHz range of frequencies. The circuit cross-section and foil roughness level for matted side and shining side are as shown in Figure 7 and Table 3.

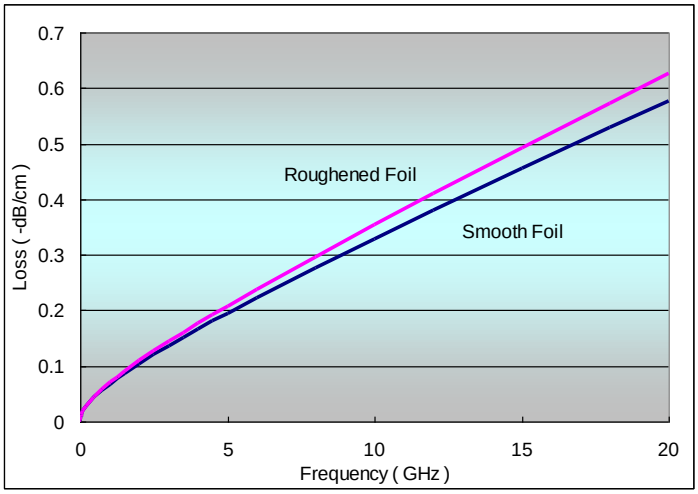


Figure 6: Copper foil type impact for signal loss.

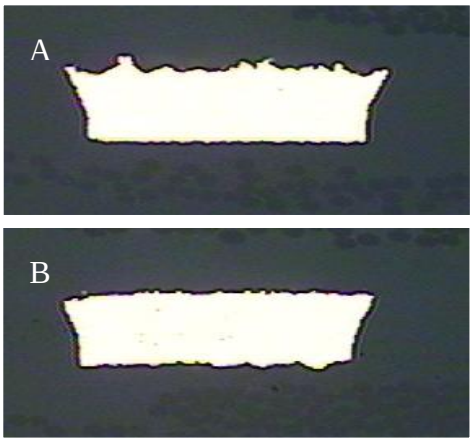
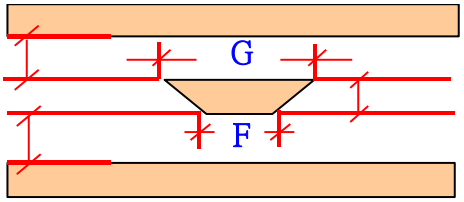


Figure 7: cross-section pictures (A) HTE foil; (B) smooth foil

To isolate material loss from overall loss and expand our estimate of the attenuation in other construction designs, we can extract the dielectric constant and dissipation factor values from the measured attenuation loss. We have created a model based on actual circuit dimension data, including circuit Rdc resistance; material dielectric constant and dissipation factor at low frequency range plus using IBM 2-D field solver simulation software [2]. We use this model to iteratively compare measured and simulated attenuations to get matched frequency dependant R(f), L(f), C(f), G(f) properties.

Table 3 : Circuit trace surface roughness level

Type	Position	sample N	Roughness
HTE Foil	F : shinning side	14	0.115 mil
	G : mate side	14	0.313 mil
RTF Foil	F : shinning side	14	0.192 mil
	G : mate side	14	0.207 mil



Once the simulation and measurement fit is determined. The R(f), L(f), C(f) and G(f) parameters are used to extract the laminate material's "Effective" Dk / Df characteristics. The word "effective" means that the output dielectric constant and dissipation factor lump the copper roughness impact of skin effect with laminate dielectric losses. We can use the effective dielectric constant and dissipation factor to estimate others attenuation.

Figure 8 is the effective dissipation factor trend in terms of frequency based on a low loss material that was composed of HTE (high temperature elongation) foil and RTF (reverse treated foil). The roughness of HTE and RTF foils are 0.31mil and 0.20mil respectively. The influence of copper foil roughness gives an ~0.002 higher effective Df value in this case. Foil with a high roughness level and/or oxide treatment with high weight gain or loss will increase the signal loss and narrow the bandwidth significantly [3]. The dashed line in the chart is measured by common split post dielectric resonator method This uses a resonant cavity with fixed frequency to measure a bare core material specimen. The effective Df line with RTF foil is slightly higher and next to the material Df value. Basically, the effective Df represents the material Df in a smooth foil construction.

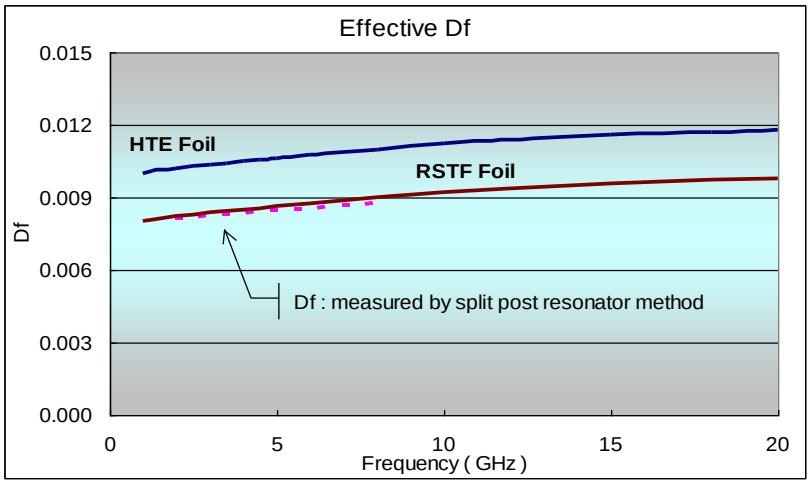


Figure 8 : Effective dissipation factor results in terms of frequency, foil type and test method

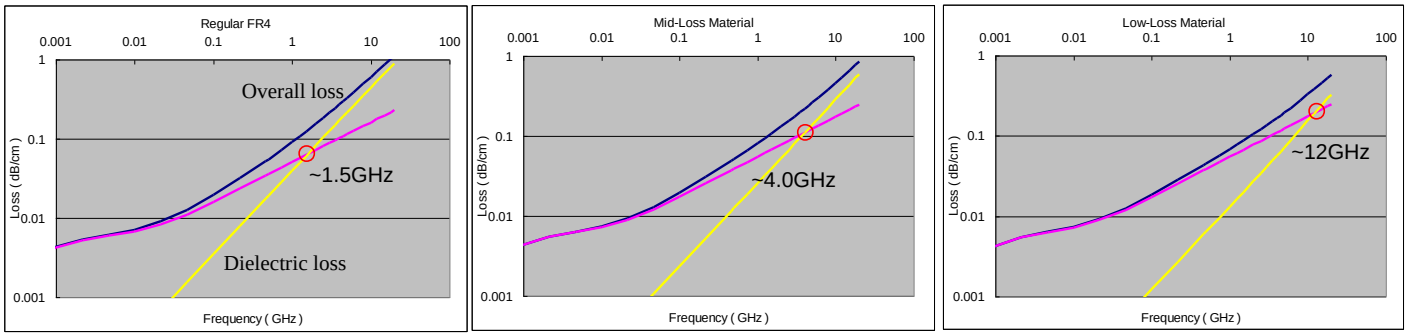


Figure 9: Loss relationship between overall loss, dielectric loss and conductor loss for different materials

Figure 9 is a relationship chart showing dielectric loss, conductor loss and overall attenuation. It includes regular FR4 material, mid-loss material and low-loss material properties. In the charts, the blue line is overall attenuation, the pink line is conductor loss and the yellow line is dielectric loss. The dielectric loss crossover point depends on material types, foil grade and process conditions. Here the crossover points locate at ~1.5GHz, ~4.0GHz and ~12GHz respectively. It's easy to see that while utilizing better and better base laminate materials, the conductor loss will be the bottleneck for a higher bandwidth. Therefore reverse treated foil material was considered to be the preferred option over conventional HTE grade foil.

Construction Impact on Signal Integrity

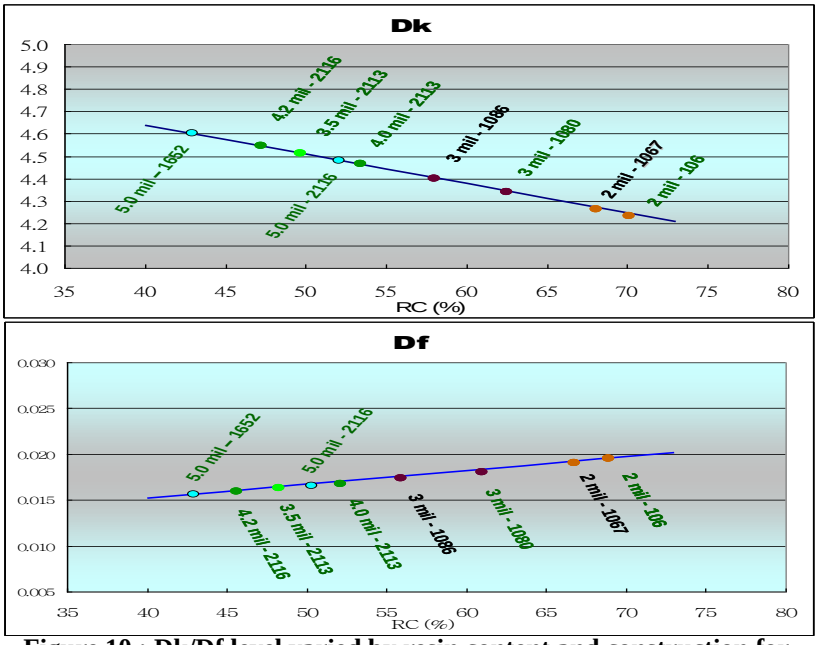


Figure 10 : Dk/Df level varied by resin content and construction for FR4.

When talking about glass fabric reinforcement, the first topic of concern is dimensional stability. However when we change the laminate construction from one type to another, the resin content is changed and this leads to different dielectric constants and dissipation factors accordingly. Figure 10 shows the FR4 grade material resin content, dielectric constant and dissipation factor variance for several common laminates thickness from 2mil to 5mil .The variance of resin content between constructions is about 5% to 10%. What's the impact level for construction in signal integrity? Here we use regular 106 and 1067 fabrics separately to build a stripline at high resin content group (63%~70%) constructions and we use regular 2116 and 1652 fabrics separately to build a stripline at low resin content group (43%~53%) construction in order to compare the

influence of laminate construction and resin content under FR4 grade material. Currently utilizing thinner and thinner laminate material (higher resin content) in design is the trend. Unfortunately this trend will deteriorate signal loss level seriously. Referring to figure 11, the material signal loss will increase 0.18dB/in at 5GHz while driving laminate core thickness from 4~5mil low resin content materials construction down to 2~3mil high resin content material construction. Therefore, by choosing alternative weaving design density and pattern fabric we can slightly reduce resin content level by 5~10% for identical dielectric thickness material and gain 0.01db/in ~0.02dB/in at 5GHz back in signal loss. Beside improving electrical performance, this also has a benefit in dimensional stability.

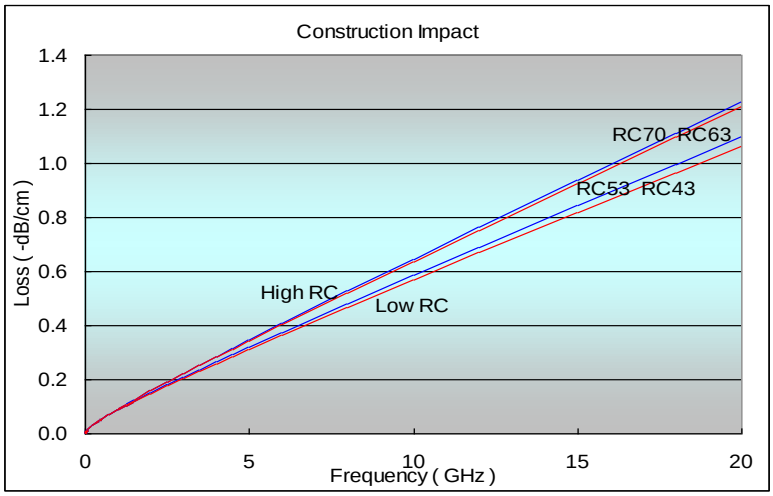


Figure 11 : Resin content and construction impact for attenuation loss

Fabric weaving Impact on Signal Integrity

E-glass fabric is an intertexture material. Interweaved warp and fill direction yarns will generate regular node areas as Figure 12 shows. Beside node areas, there are also regular "hollow windows." The size of the window area is roughly 10mil square for 1080 fabric type. This will cause signal skew issues especially for differential lines when the circuit trace crosses over resin rich area versus the resin poor areas as Figure 12 shows (fabric nodes and window areas).

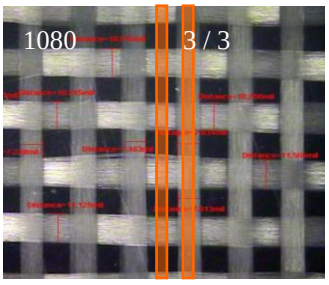


Figure 12 : 1080 fabric

This micro-uneven resin content situation centers on dielectric thickness less than 5 mil in construction. Some studies show that rotating the CCL laminate fabric weaving or circuit line layout a certain degree (~5 deg) relative to the fabric can overcome this issue but this is seen as a high cost solution. Material-wise some measures could moderate the awkward situation.

From the material's side one approach includes using open-filament fabric or high weaving and a flat design fabric and/or two-ply construction instead of one ply construction. This approach could moderate and compensate for the resin

micro-uneven phenomenon.

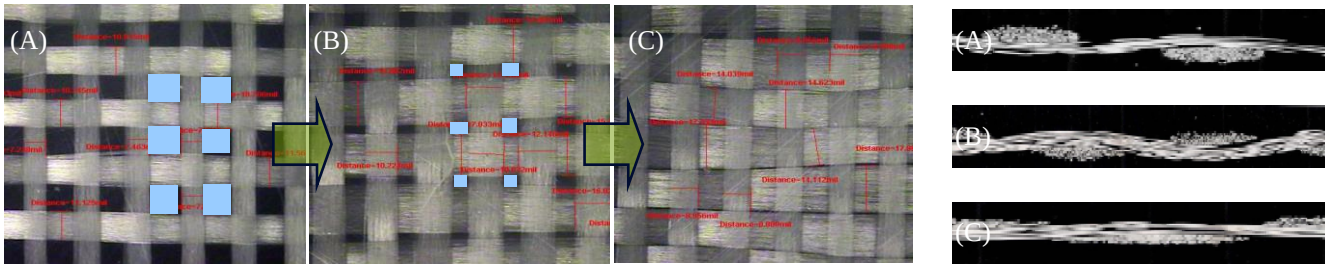


Figure 13: fabric microscope and x-section pictures (A) regular type ; (B) open-filament type ; (C) flatten design

Figures 13 are the pictures of regular 1080 fabric, open-filament type and flat design fabrics. Here we can find that open-filament treatment reduce the hollow window size significantly. Flatten design fabric can eliminate the hollow window issue almost completely. Table 4 shows the fabric hollow window coverage area ratio between different fabric treatments and fabric designs. Take 2mil construction for example. This approache can reduce the resin rich spot area from 30% down to nearly zero and will give a more uniform resin and fabric matrix. Two-ply construction is another solution, but it's only suitable for 4~5mil and slightly thicker thin materials.

We are still in the construction stage of our plan to measure and understand the actual influence of fabric treatment in signal integrity. Although we have no solid data to share this time we will publish those results in a future paper.

Table 4 : Fabric hollow window area ratio in terms of fabric construction and design

Window Area Ratio	Regular Type	Open-filament Type	Flatten Design Fabric
2 mil	~30 %	~15 %	~1 %
3 mil	~25 %	~8 %	~3 %
4 mil	~10 %	~3 %	~1 %

Moisture Impact on Dielectric constant and Dissipation factor

The water dielectric constant and dissipation factor are about 80 and 0.1 at 1GHz respectively. It is no doubt that the quantity of moisture in the base materials is one of significant factor for the material dielectric constant and dissipation factor. For a given environment humidity level the soaking time, board thickness, board construction and system on-off status etc., are all factors in the moisture absorption and purge mechanisms of the board.

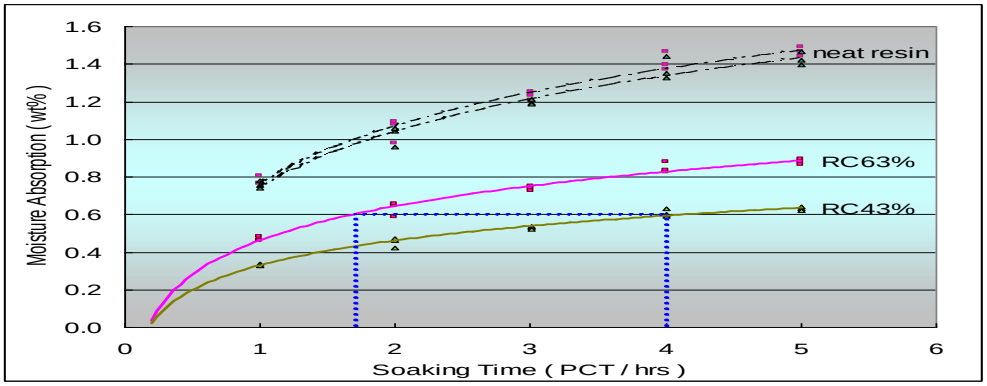


Figure 14 : Moisture pick-up rate varied by construction and moisture soaking time

Figure 14 is a moisture pick up acceleration test in terms of soaking time and construction. Here we compare the moisture absorption behavior of high resin and low resin content constructions to neat resin base. The neat resin moisture absorption rate and quantity behavior for two constructions are close and similar as shown by the dashed lines in chart, but the soaking time for two constructions to reach identical moisture absorption level is totally different. Therefore, it's hard to quantitatively analyze the moisture impact in complex print circuit board construction and situation.

To characterize the moisture impact for final attenuation loss in board we used a split-post dielectric resonator method to measure bare core Dk and Df variance that was caused by actually absorbed moisture instead of measuring attenuation loss with different environment condition method. Upon measuring Dk and Df we used simulation software to estimate the variance for embedded stripline construction attenuation loss.

Figure 15 shows dielectric constant and dissipation factor variance in terms of moisture pick up quantity for low resin content construction and moisture absorption levels in various resin systems. Resin systems play a key factor in the moisture absorption maximum level. Basically the moisture impact for dielectric constant at high frequency is minor, but it increases

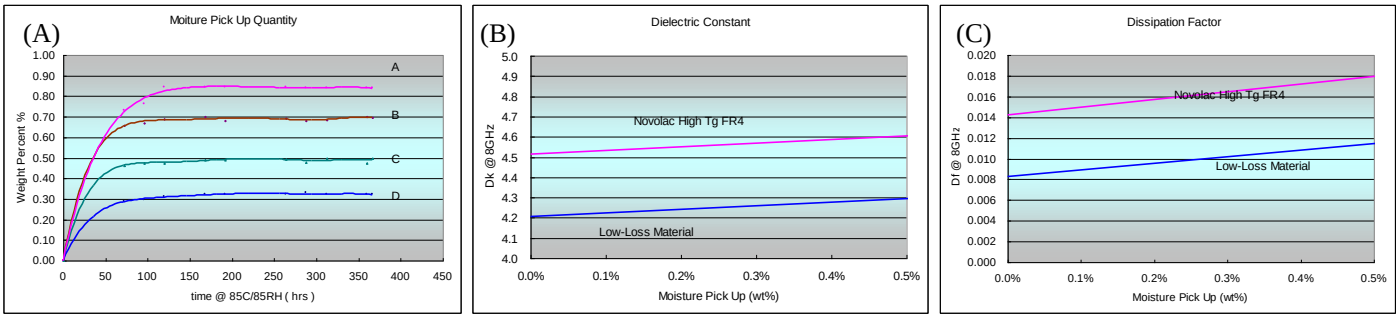


Figure 15: (A) Moisture Absorption A: Dicy High Tg, B : Novolac High Tg, C : Modified-Novolac FR4, D : Low-loss material. (B),(C) : Dk and Df variance by moisture pick up quantity for high Tg FR4 and low-loss materials

the dissipation factor by a 20~30% minimum under severe environmental condition of high humidity. It's easy to estimate that moisture will increase signal attenuation loss by 20~30% roughly based on our previous simple equation. Another dominate environmental factor is temperature. It's more critical for harsh environmental applications and we plan to look at it in our future study matrix.

Conclusions

Signal integrity is a very complex question. From the material perspective it's hard to say which basic property factor is the most critical one. Each system has its own limitations and may have different critical items.

In brief and under simplified conditions, for good signal integrity in the IT industry, choosing a suitable basic resin system with smooth foil type is the most important factor. A good and suitable resin system provides a balanced trade-off between physical performance, electrical performance and system cost. Designers get broader space to operate and need less fencing for signal integrity concerns and lead-free compatibility. Another consideration is the signal consistency across the board. Material construction is a solution which can reduce resin content, micro-variance and thus moderate signal skew phenomenon and impendence variance.

Reference:

[1] Dr. Eric Bogatin; “Practical Characterization and Analysis of Lossy Transmission Lines”, Designcon 2001.

[2] Alina Deutsch, Fellow, IEEE, Thomas-Michael Winkel, Gerard V. Kopcsay, Member, IEEE, Christopher W. Surovic, Barry J. Rubin, George A. Katopis, Fellow, IEEE, Bruce J. Chamberlin, and Roger S. Krabbenhoft ; “Extraction of □□(f) and tan□ (f) for Printed Circuit Board Insulators Up to 30 GHz Using the Short-Pulse Propagation Technique”, IEEE TRANSACTIONS ON ADVANCED PACKAGING, VOL. 28, NO. 1, FEBRUARY 2005

[3] Bruce Lee, Roger S. Krabbenhoft, “Effects of Adhesion Promotion Treatment on Electrical Signal Attenuation”, IPC Printed Circuits Expo, APEX and Designers Summit 2007.

PRINTING PROCESS OPTIMIZATION FOR 0.4MM PITCH AREA ARRAY PACKAGES

Fredrik Mattsson
Dr. Dongkai Shangguan
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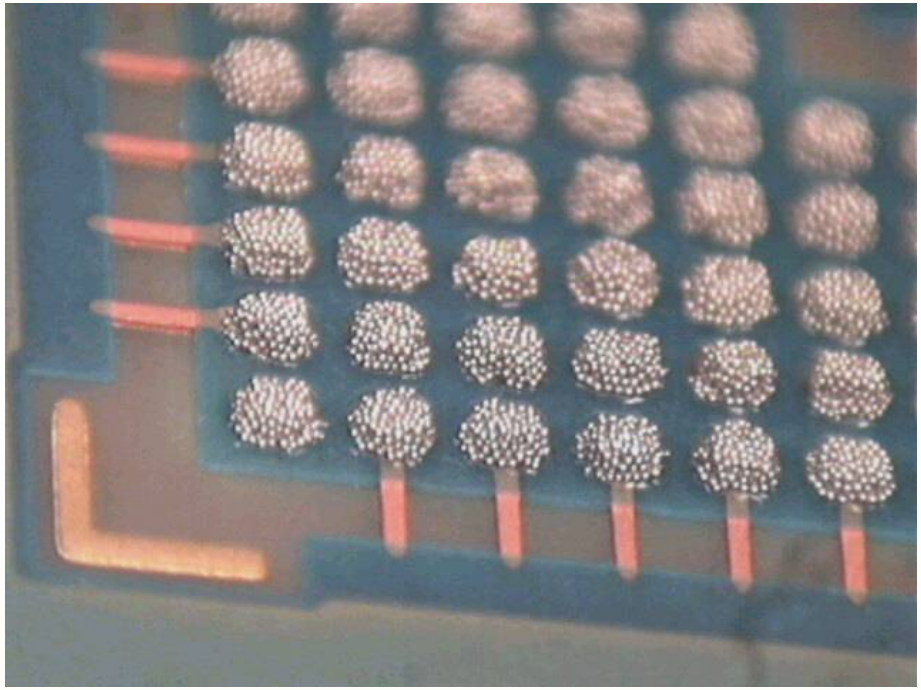


Introduction

- In miniaturized electronics, Chip Scale Packages are moving from 0.5mm to 0.4mm pitch

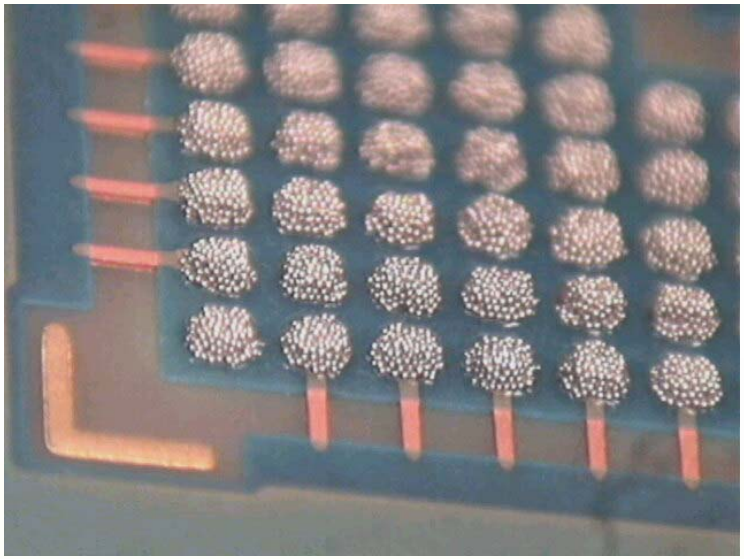
- When functionality and complexity increases, so does the number of I/Os and thus the number of solder joints

- This forces reduction of DPMO (Defects Per Million Opportunities) to maintain or improve a high product yield

- A study, designed to capture the root cause of low level randomly distributed print defects.

Introduction

- Reduction of board area for 0.4 compared to 0.5mm pitch package: 33% (Full array package with 196 I/Os)
- Solder paste printing needs improvement to meet the new requirements



Background

- Process and design optimization was done to eliminate systematic defects until volume Cp/Cpk is acceptable & only random defects remain

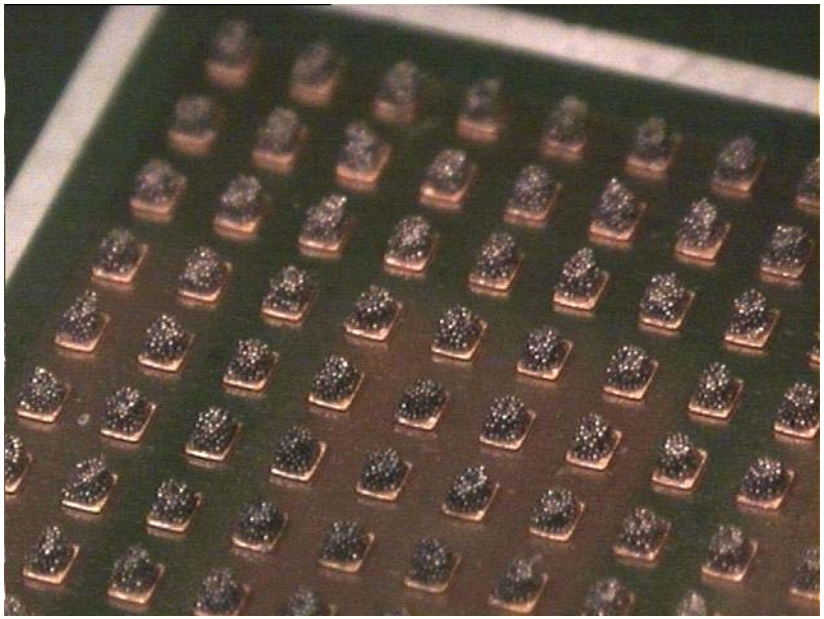
- A quarter of a million solder paste deposits printed, inspected and volumetrically measured

- Each defective deposit, as well as the top and bottom side of the stencil, were inspected and analyzed separately

Printing Process

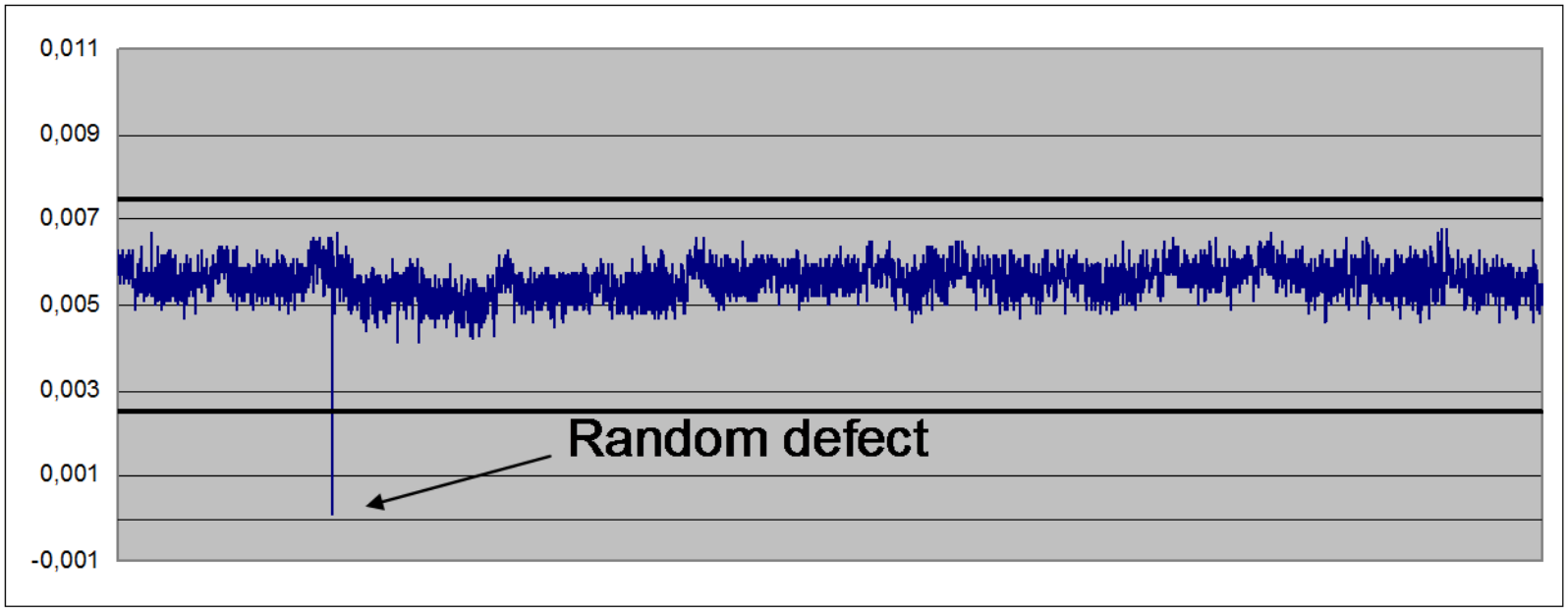
Many factors influence the quality of the screen printing process

- Stencil thickness
- Solder paste characteristics
- Solder paste type (particle size)
- printing parameters:
- Printing speed,
- Pressure
- Separation speed



- Mechanical condition of the stencil,
- Cleaning frequency,
- Flatness of the printed circuit board,
- Method of supporting the PCB during

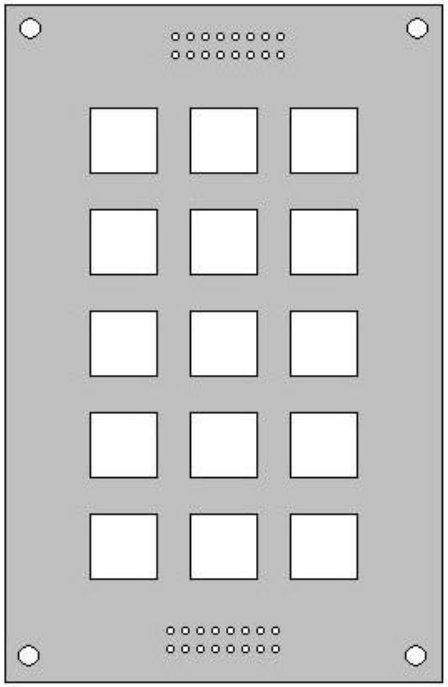
Random Defects



- Previously optimized printing process for lead free 0.4 mm CSPs is examined
- Focus on the randomly distributed defects that remain
- The objective is to identify the root cause of those remaining defects

Test Vehicle

- Size 132 x 77 x 1 mm
- 15 CSP sites, total 5400 deposits
- FR-4 laminate core material, 6 copper layers
- Solder mask between the soldering surfaces
- Similar to drop test boards per JESD22-B111
- Resembles real applications in material and design



Stencil Material & Tolerances

- 4mil (~100um) thick, Laser cut, electro-polished, stainless steel
- Standard, low-cost option for volume manufacturing

Electroformed stencils or thinner stencils could perform better but:

- Thinner stencils do not give enough solder paste for large components
- E-formed cost more, vary in thickness & are not globally available at consistent quality
- Sample apertures measured to ensure the specified tolerances

Aperture Design

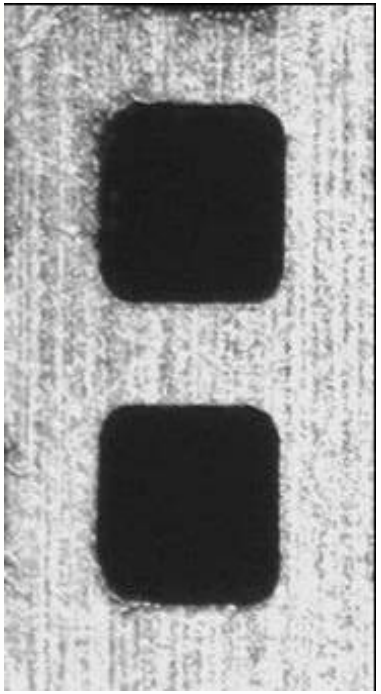
•Based on Flextronics experience with fine-pitch printing, optimal stencil aperture was calculated

• Area Ratio and bridging-risk considered and tested

• Chosen aperture size has been tested and optimized

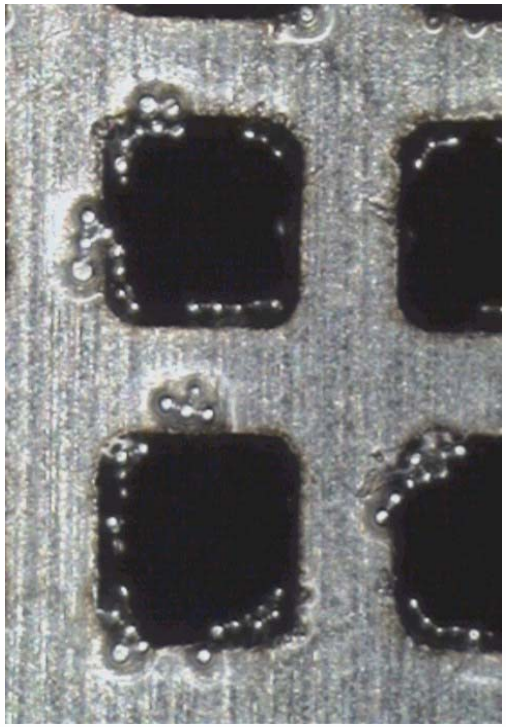
• Aperture size was not varied in this experiment

• Area Ratio was calculated to 0.67



Solder Paste Printing

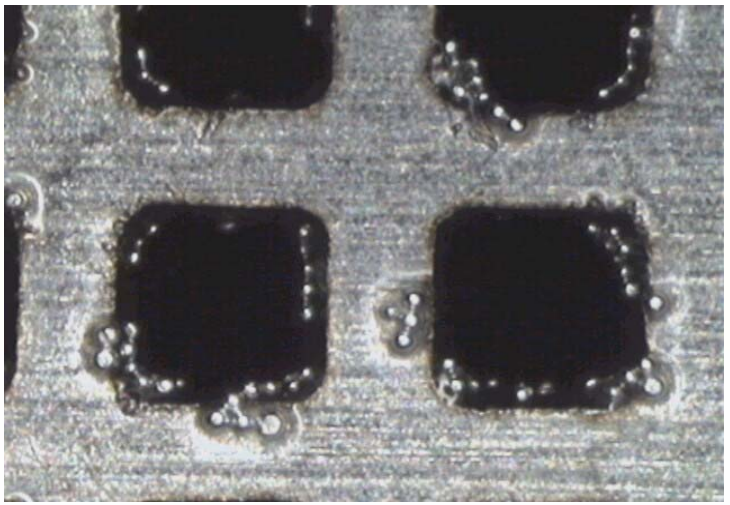
- 3 batches, 2 pastes & total 253.800 deposits
- 2 previously evaluated lead free pastes compared
- 11 PCBs with brand A (particle size 25-38um)
- 10 PCBs with brand B (particle size 25-45um)
- 25 PCBs with brand B (particle size 25-45um)
- Metal blades 60^{o} and full block support + vacuum
- No auto-wipe; some smearing but no defects



Printing parameters

- Printing pressure 12 kg
- Printing speed 40 mm/sec
- Separation speed 10 mm/sec

Separation speed =>strong influence!

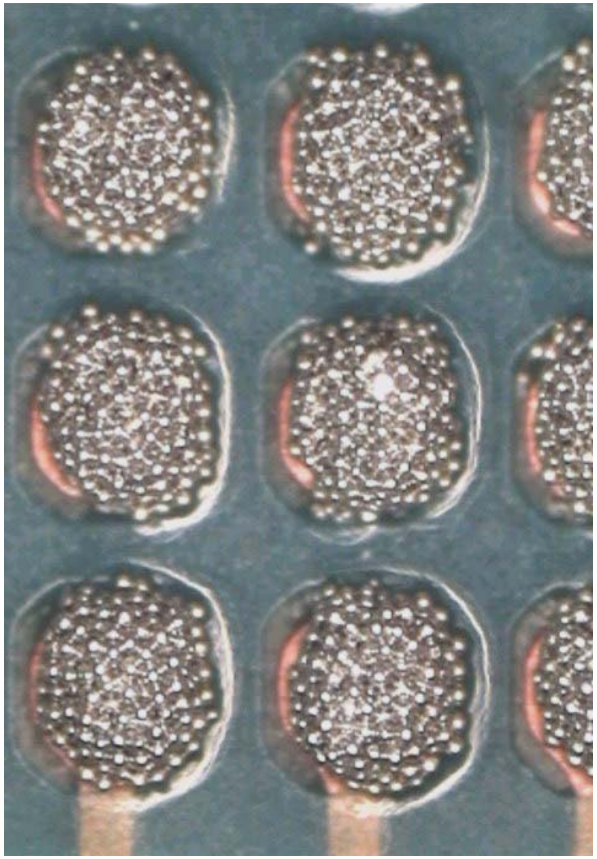


Brand	A	B
Alloy	SAC305	SAC305
Particle size	25-38um	25-45um
Flux	NoClean (ROL0)	NoClean (ROL0)
Metal content	89.1%	89.0%

Solder Paste Inspection

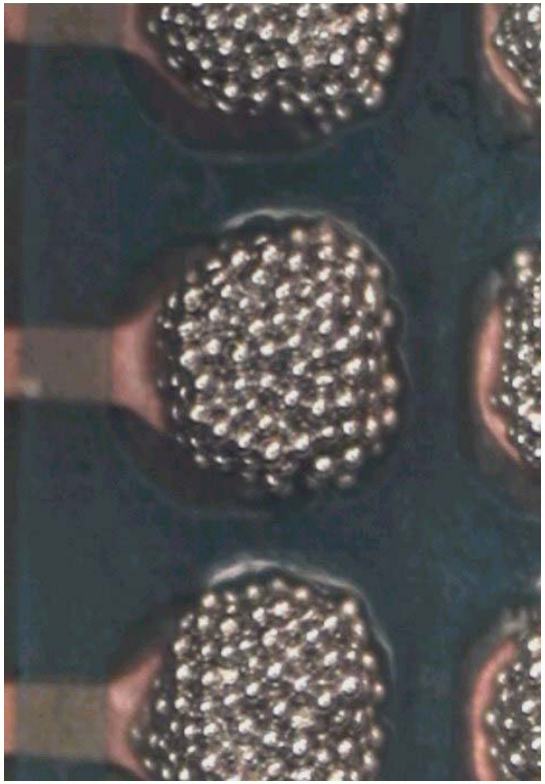
- 3D volume measurement of each deposit
- Standard resolution machine used to find defects
- Additional high resolution volume measurement
- Stop On Fail, PCB & stencil inspected in 400X
- Defect criterion <50% volume and bridges
- Manual visual inspection using optical microscope

Some flux bleeding observed, overall well defined and uniform deposits



Solder Paste Volume

- Cp 2.3 for 253.800 deposits
- Specification limit: +/-50% of avg. measured volume
- Gauge Repeatability & Reproducibility 15%
- GR&R for 0201 size deposits 9%
- Solder paste brand did not influence Cp or defect rate
- Pastes performed equally in every aspect of this trial



Defect distribution

10 defects found in 253.800 deposits => 39 DPMO

One instance of Drop paste caused 10 low deposits, which is counted as 1 defect

All other defects are singles

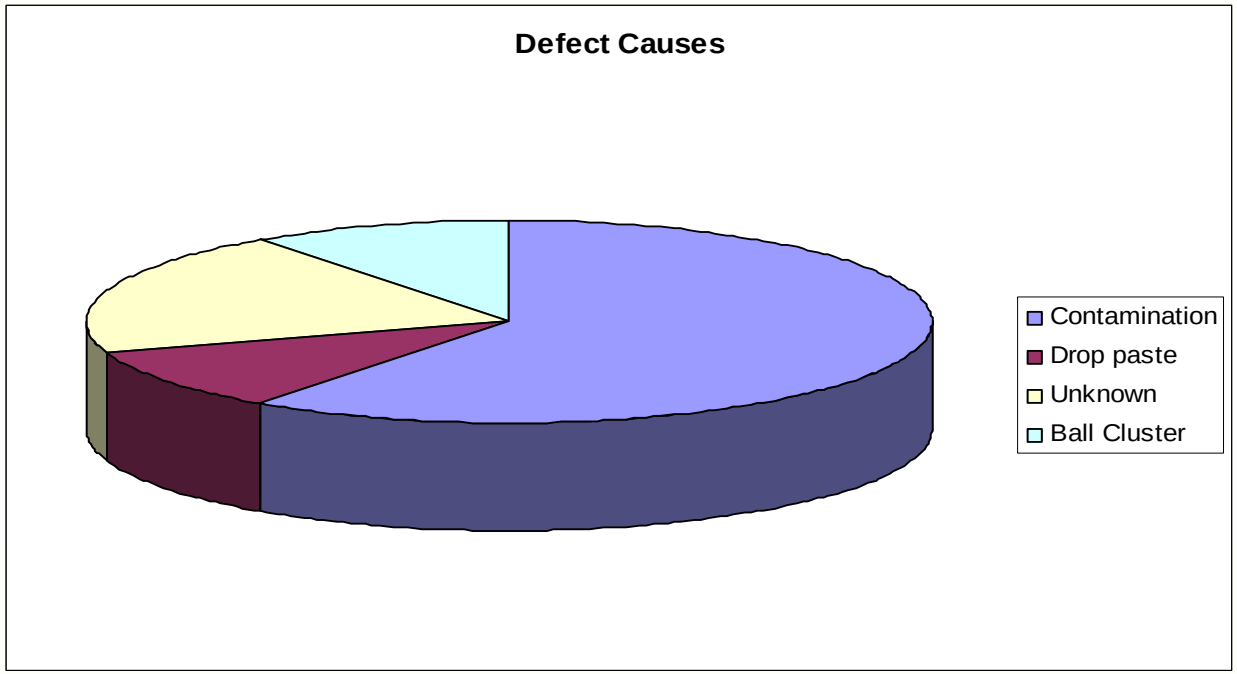
<u>Out of these 10 defects:</u>

6 contaminations

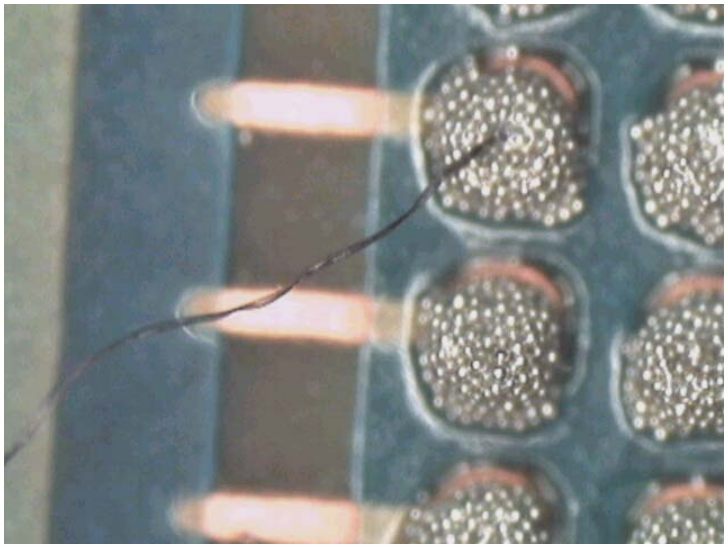
1 drop paste

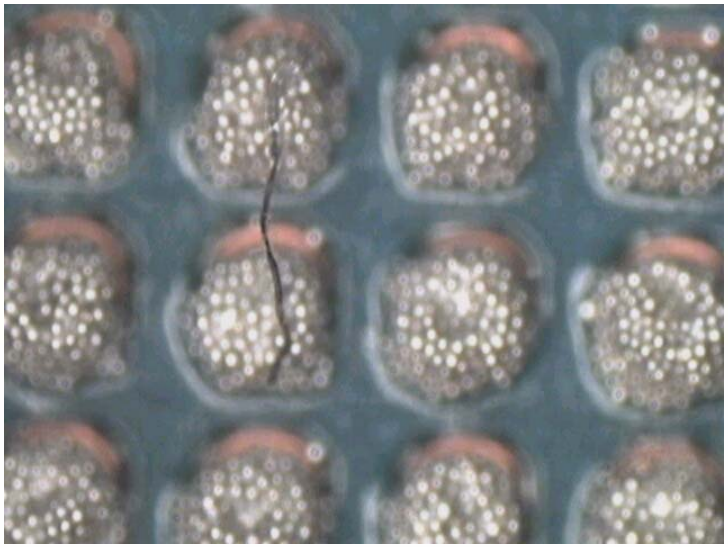
1 solder sphere cluster

2 Unknown



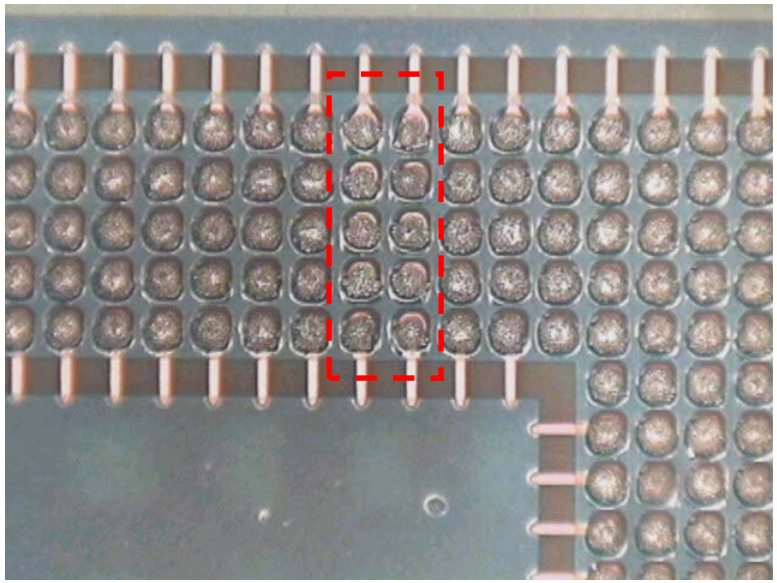
Fibres

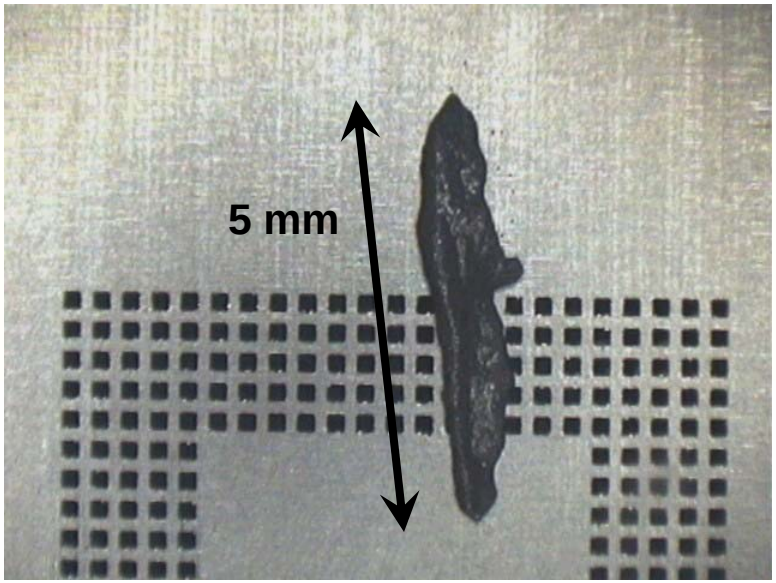




Fibres were relatively common on the boards, but not seen to cause defects

Dropped Paste





Symptom: One or multiple adjacent deposits have paste present, but volume, and especially height is low

Cause: Paste dropped on stencil

The defects on the left are typical for paste dropped on the topside of the stencil, after the squeegee has passed, but before separation

Flakes

• Main cause of defects was transparent flake. This contamination was found on 4/6 defective deposits caused by foreign particles

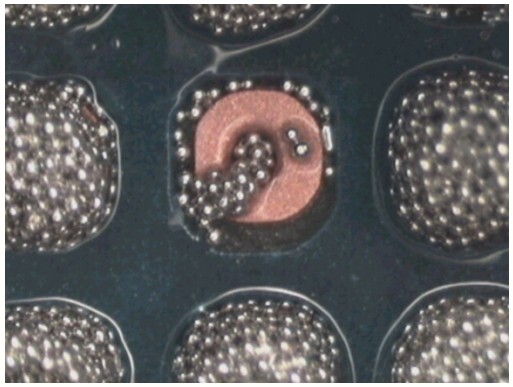
• Flakes found on stencil bottom-side. Conclusion: they were on the board when loaded into the printer and transferred to stencil during the printing operation

• Size of flakes is in same range as the aperture. Flakes were found to be of firm matter and could be manipulated as solid particles

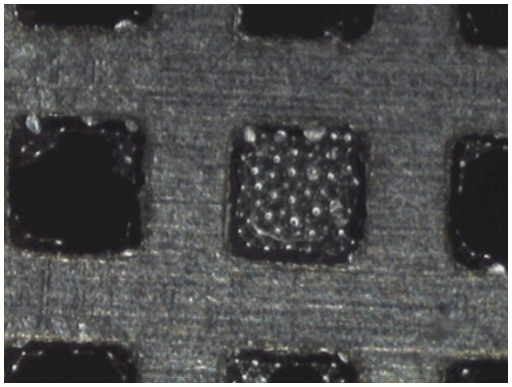
• Even though material analysis was inconclusive, it is suspected that particles originate from PCB manufacturing processes; solder mask or drilling/milling debris

• The two samples analysed, were found to have different material compositions

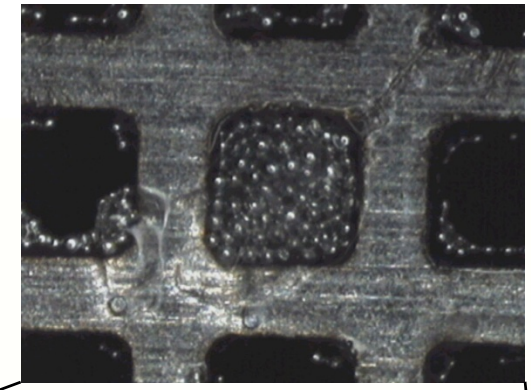
Flakes, Paste A



Defect on board

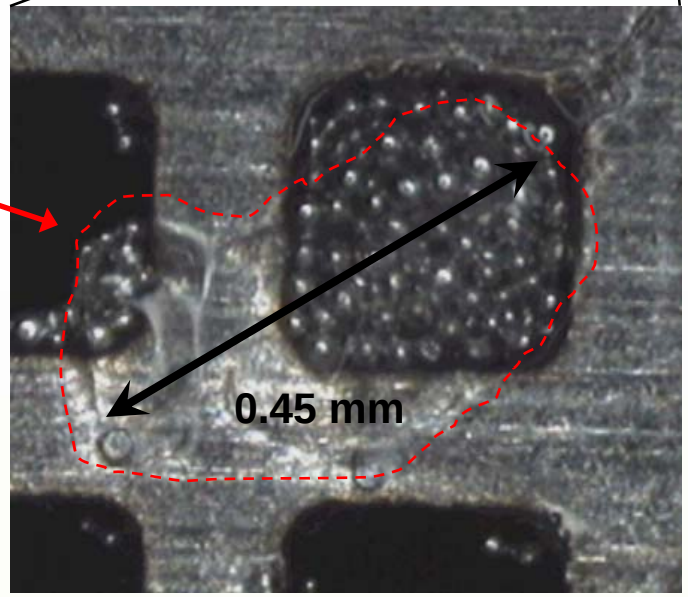


Topside stencil

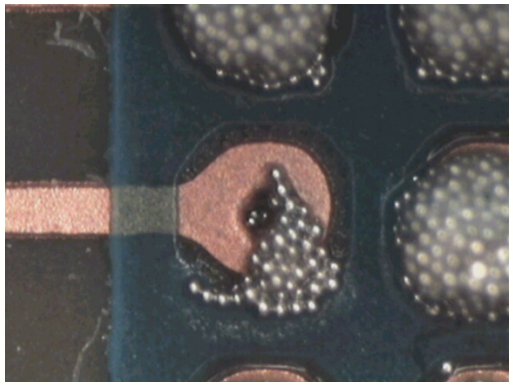


Bottomside stencil

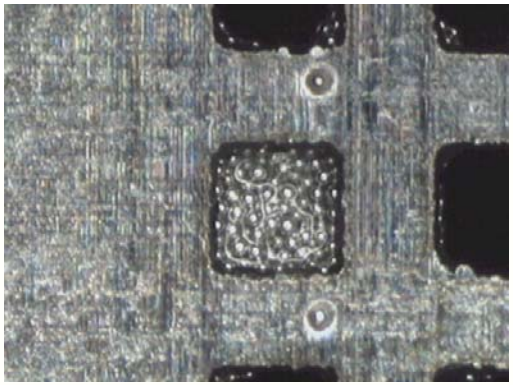
A transparent ”flake” is covering large part of the aperture. It is of firm matter and could be moved like a flake. Origin is unknown



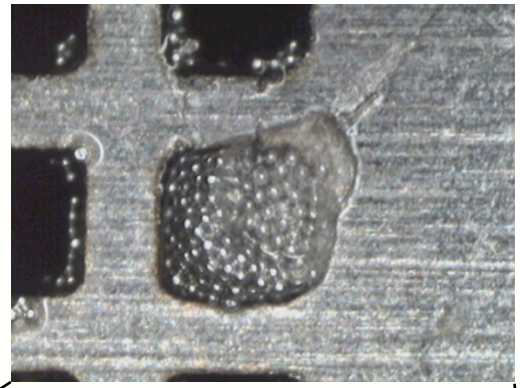
Flakes, Paste B



Defect on board

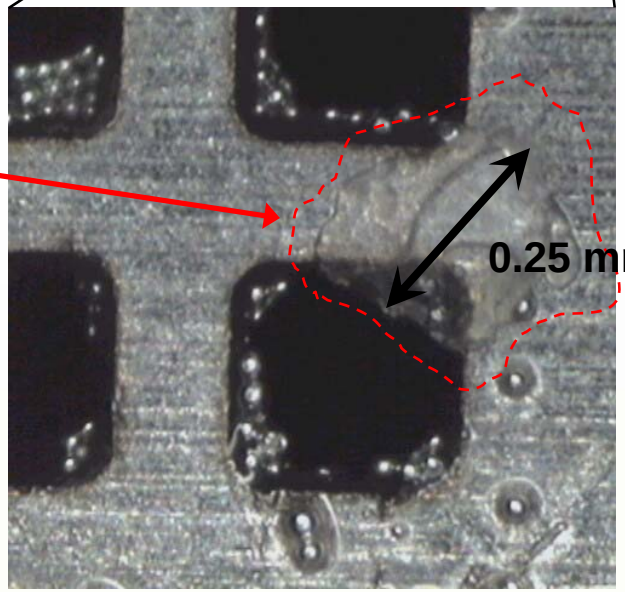


Topside stencil

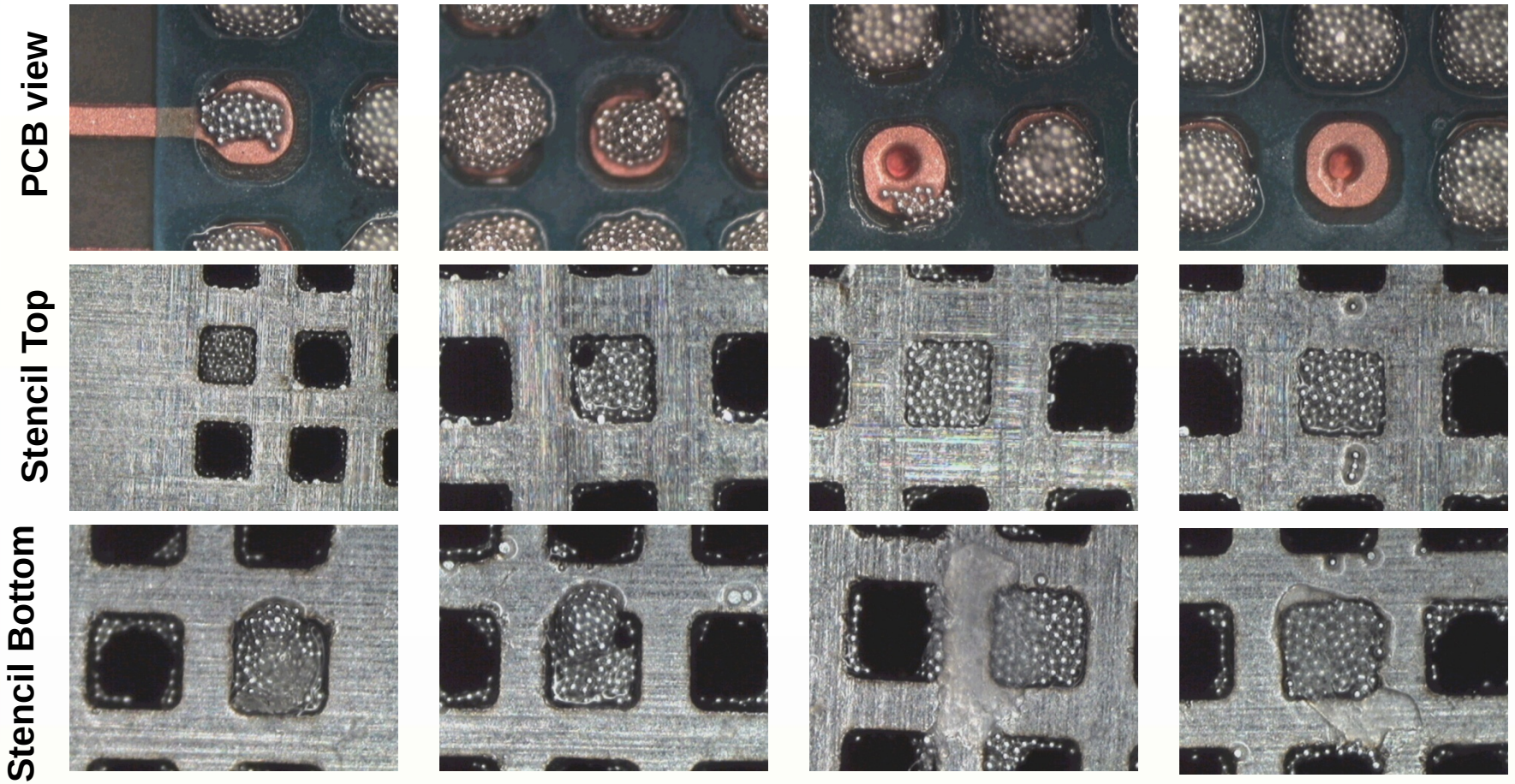


Bottomside stencil

Again, a transparent ”flake” is covering
Large part of the aperture. It is of firm
Matter and could be moved like a flake.
Original position above.
Origin is unknown



Flakes, Paste B, 2nd batch

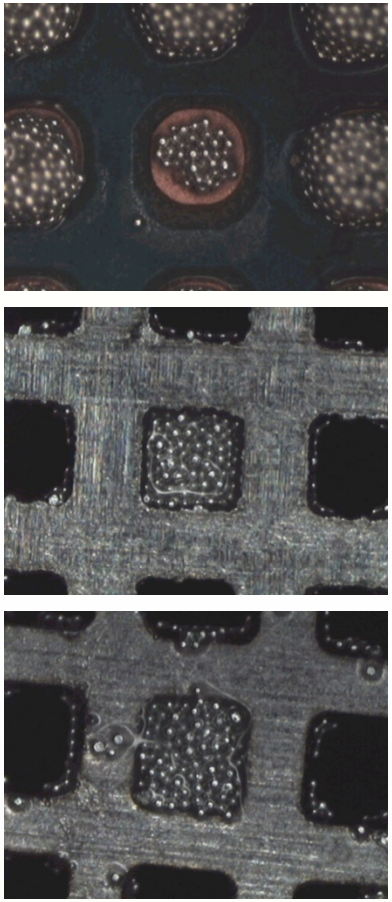


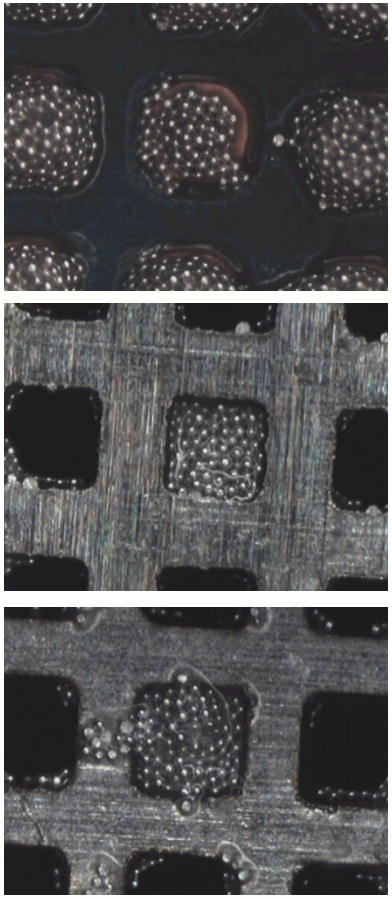
Flakes, Paste B, 2nd batch

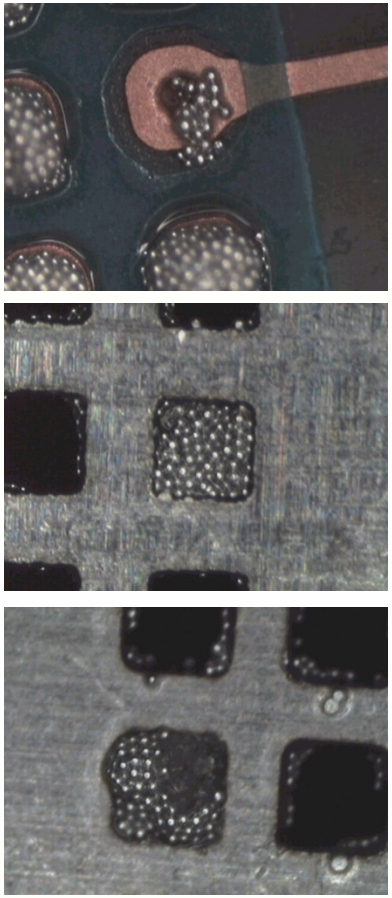
PCB view

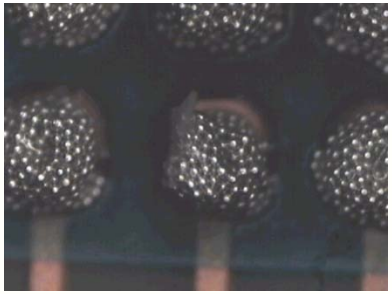
Stencil Top

Stencil Bottom









17um thick flake

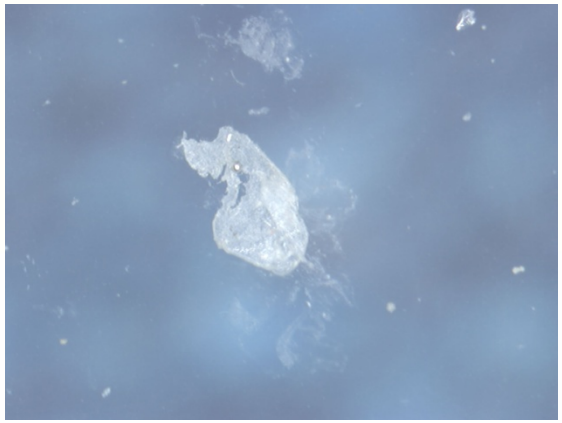
Unknown cause

Ball cluster?

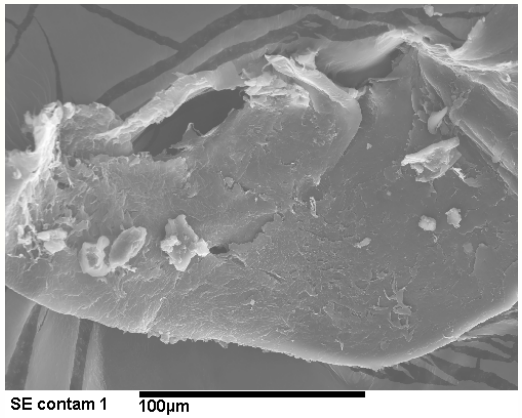
Dark lump

Particle Analysis, 1

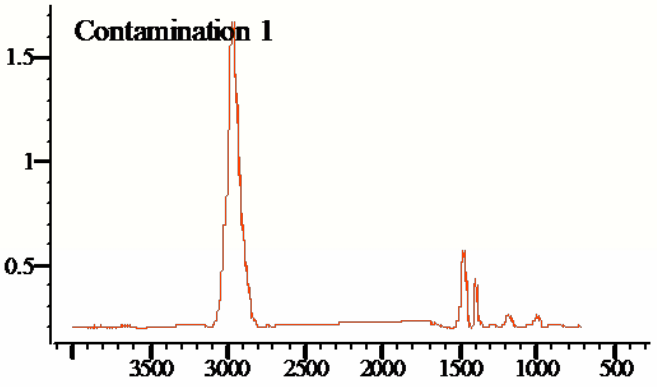
Two particle samples which caused printing defects were inspected with high magnification light microscopy as well as SEM (Scanning Electron Microscope), FT-IR (Fourier Transform Infrared spectroscopy) and EDX (Energy Dispersive X-Ray Spectroscopy)



Contamination 1, light microscopy

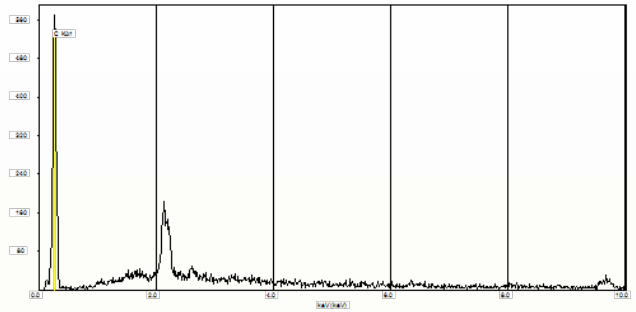


Contamination 1, SEM



FT-IR spectra indicative of aliphatic hydrocarbon

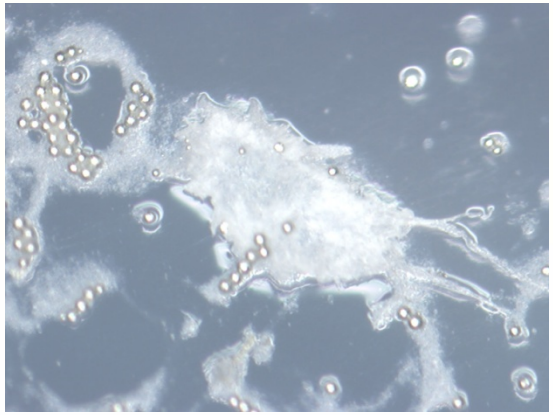
The first sample appeared homogeneous and was found to be composed of aliphatic hydrocarbon, e.g. oil and polypropylene & polyethylene. Plastics are a likely source of this material



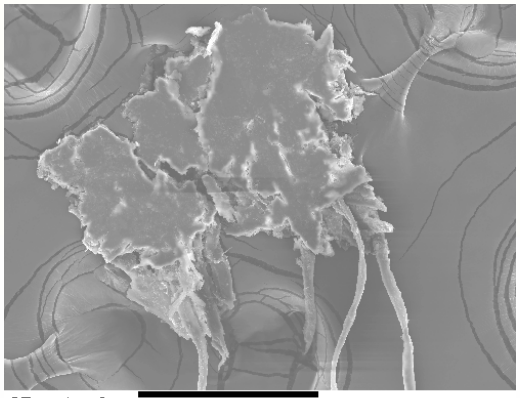
EDX Spectrum. Note sample is gold coated for analysis

Particle Analysis, 2

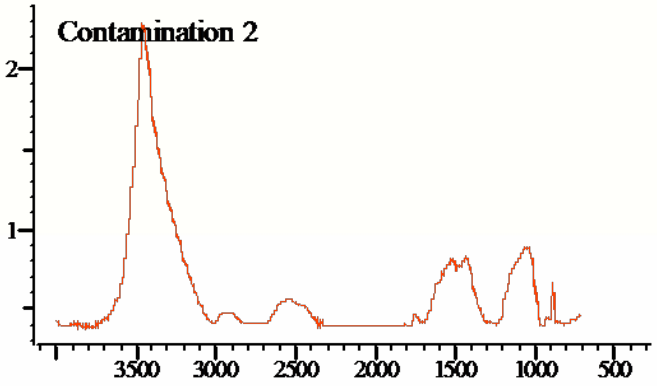
The second sample appeared to have fibres as well as a bulk material base
Bulk material contains carbon, oxygen, aluminium, silicon, and calcium.
Fibres contain carbon, chlorine, and calcium.



Contamination 2, light microscopy

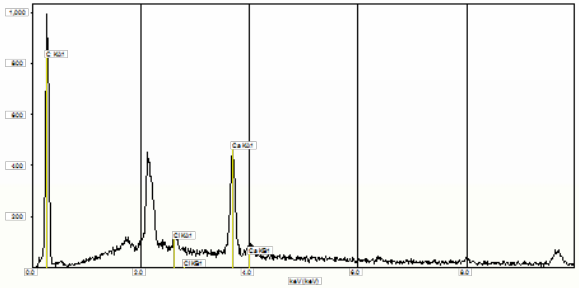


Contamination 2, SEM

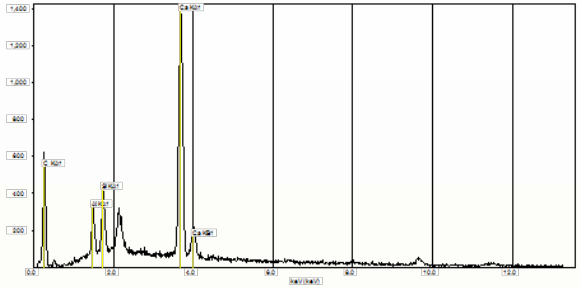


FT-IR spectra without positive identification

A sample of the flux was also analysed to eliminate this from the final result



EDX Spectrum showing bulk material
Note: sample is gold coated



EDX spectrum showing2 fiber
Note sample is gold coated

SUMMARY

To improve the printing quality for fine pitch CSPs, it is necessary to first eliminate systematic print defects by optimizing the pad and aperture design, printing parameters, board support as well as choosing the right solder paste and controlling the stencil tolerances and quality to reach a low DPMO.

Thereafter, foreign particle contamination on PCB can contribute significantly to the defect count in the solder paste printing process. In addition, the dropping of solder paste from squeegees must be avoided.

Acknowledgements

The authors would like to thank

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Magnus Carlsson

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Thank you