Implementation of Flip-Chip and Chip-Size Package Technology

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Abstract
As new generations of electronic products emerge they often surpass the capability of existing packaging and interconnection technology and the infrastructure needed to support newer technologies. This movement is occurring at all levels: at the IC, at the IC package, at the module, at the hybrid, the PC board which ties all the systems together. Interconnection density and methodology becomes the measure of successfully managing performance. The gap between printed boards and semiconductor technology (wafer level integration) is greater than one order of magnitude in interconnection density capability, although the development of fine-pitch substrates and assembly technology has narrowed the gap somewhat. All viable efforts are being used in filling this void utilizing uncased integrated circuits (flip-chip) and incorporating more than one die or more than one part in the assembly process.

This paper provides a comparison of different commonly used technologies including flip-chip, chip-size and wafer level package methodologies detailed in a new publication, IPC-7094. The IPC document describes the design and assembly challenges for implementing flip-chip technology in a direct chip attach (DCA) assembly. It considers the effect of bare die or die-size components in an uncased or minimally cased format, the impact on current component characteristics and reviews the appropriate assembly methodology. The focus of the IPC document is to provide useful and practical information to those who are mounting bare die or die size components or those who are considering flip-chip process implementation.

Introduction
Although the development of fine-line substrates and advanced assembly technology has narrowed the gap somewhat, the density margin between printed boards and the interconnection density capability of semiconductor technology is greater than one order of magnitude. The bond sites, typically distributed around the periphery of the die element, are somewhat uniform size and spacing, however, the spacing of the bond sites continue to shrink. The bond sites (25 to 50 microns square) are primarily designed to accommodate aluminum or gold wire-bond processes. When bond site spacing cannot accommodate the required wire size, bond sites are often arranged in the staggered pattern. In order to minimize the area required for mounting the uncased die, a growing number of companies are modifying the wire-bond contact site to accommodate direct chip mounting (flip-chip). To ensure that a satisfactory electrical interface is made, the die (typical of that shown in Figure 1) must be furnished with solder reflow compatible contact features (solder alloy bump or ball) and precisely aligned over the corresponding lands provided on the substrate.

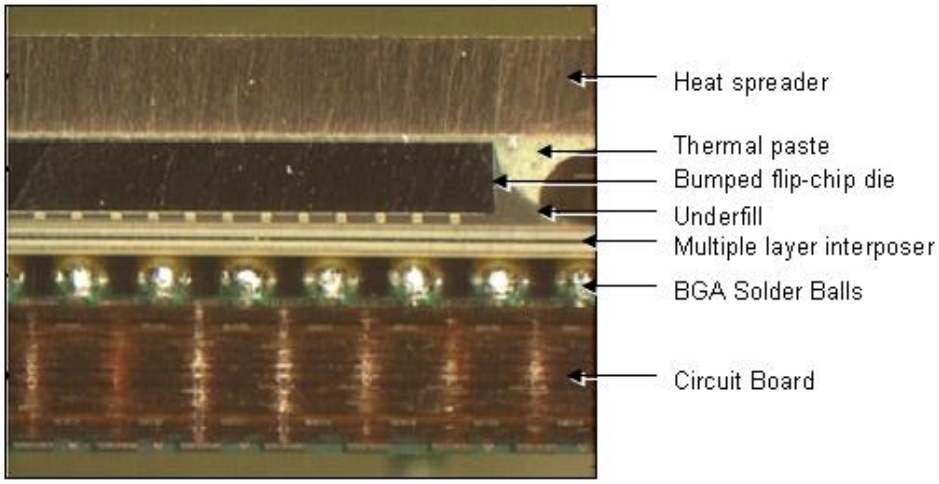


Figure 1. High I/O flip-chip on multilayer BGA configured interposer structure (IBM).

For user defined applications, the co-design of the silicon die to ensure efficient packaging or second level flip-chip attachment is strongly recommended.

Ball and bump contact process methodologies
Several methods have been developed for providing spherical contacts while the die element remains in the wafer format. One method delivers molten solder through a nozzle in a jet-like stream of droplets to build-up a precise volume of alloy at each bond site. Other techniques place or deposit pre-formed spheres onto to the wafer, employing a mass reflow solder process to complete the joining process. Small dimensional differences in bump profile and size, however, can translate into the difference between success and failure in flip chip and chip scale technology implementation.

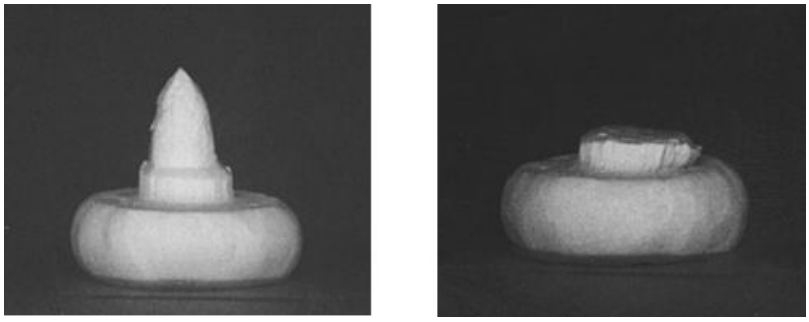
The metallurgical integrity of flip-chip and die size package interconnections will be no lesser important than solder joints on traditional surface mount technology. There are a number of alternative alloys that can be furnished for attaching the uncased die to the substrate or circuit board structure. Until recently, the bump contact most prevalent for mounting flip-chip devices was basically a lead alloy composition with a small percentage of tin alloy. Currently, companies attempting to be compliant with the RoHS directive have adapted alloy compositions that are considered free of lead. This includes combinations of tin and silver alloys, tin, silver and copper, compositions containing indium alloy to reduce the temperature required for attachment. The use of gold for the contacts has proved successful for non-soldered assembly, typically relying on conductive polymers for the electrical interface between the die and the next level assembly.

Plated gold alloy bumping
Preparing the die with a gold alloy bump is a rather complex procedure but performing the process while the die remains in the wafer level format is the most efficient technique.

Plated Gold Bump Process Sequence:

1. Apply metal adhesion layer over the passivation on the active side of wafer
2. Spin-coat photo resist over the wafer surface
3. Image and develop contact pattern to be plated
4. Electroplate Ni on the exposed contact sites
5. Electroplate gold alloy to predetermined thickness
6. Remove photo-resist
7. Chemically etch to remove remaining adhesion layer metallization

Alternative Gold Bumping Process
A less complex process for furnishing a gold contact (bump) on each bond site utilizes the same basic system developed for wire-bond assembly. The process begins with gold wire that is flame-melted onto the typical aluminum plated bond site, creating a solid gold alloy ball contact feature. The wire is immediately broken from the top surface of the gold ball leaving the contact welded in position on the die contact land. For wafer level processing, the wire-bond system requires a wider reach than is typical for package level assembly, however, standard wire-bond systems can easily handle individual die when secured in a smaller format carrier. The shape of the gold contact is seldom really spherical and the break-point of the wire may be irregular as well (see Figure 2).



Example Source: NEC Corporation

Figure 2. Gold stud-bump contact profile comparing a wire break-off to a more uniform cut wire profile.

Systems have been developed to reform the stud-bump contact using a coining process to provide a more uniform shape. Coining will improve coplanarity of the bumps as well, making the uncased die easier to test and ensure a more uniform seating plane during the next level assembly.

Uncased Wafer Level BGA Package Standards
A "wafer level" ball grid array (WLBGA) defined in JEDEC 95/4.18 is a type of BGA where the body size is equal to the bare die outline. This package is sometimes called a "real chip-size" BGA or wafer level CSP. In a wafer level BGA, all

processing required to attach a silicon IC chip onto a circuit board or substrate interposer is performed at the wafer level. The term 'Wafer Level BGA' is used to describe only individual chips after wafer dicing. The dimensions of the body accommodate assembly only of a die with a specific size, and these body dimensions will change as a result of future changes in die size. The format of the uncased device may be square or rectangular, but this aspect ratio may also change as a given device is redesigned to conform to a new die size. As a precautionary note JEDEC warns the user that the outline aspect ratio will likely differ for devices of the same functionality from multiple suppliers. A common application of flip-chip is in combination with common surface mount devices solder attached to a flexible substrate. The flexible materials, typical of that shown in Figure 3, are widely used is in the wireless handset and digital camera industry enabling foldable compact assemblies.

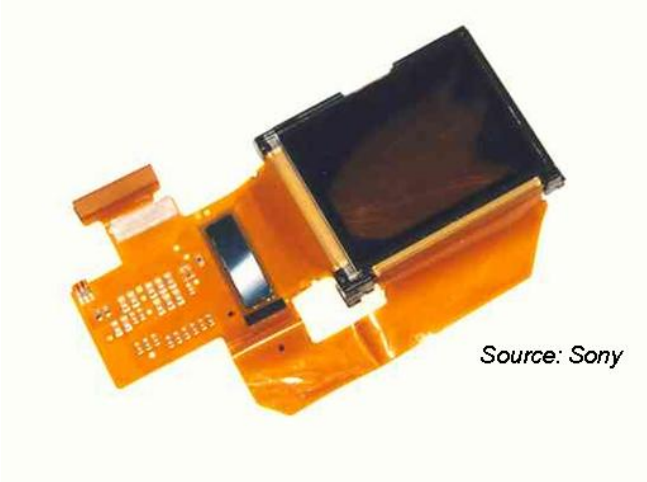


Figure 3. The driver chip for the display module is soldered directly onto plated copper lands on the polyimide substrate.

The bumped flip-chip configured display driver and related SMT devices are first soldered onto the alloy plated land patterns provided on the flexible substrate. Following reflow soldering and cleaning, a liquid polymer material is deposited at the die elements edge. The polymer flows between the active surface of the die and substrate and, following curing, physically reinforces the attachment area and interface.

Contact Redistribution for High Density Applications

The term 'redistribution' is utilized when the existing bond pad locations must be rerouted to better accommodate the flip-chip application. I/O redistribution is a sequential process where additional conductive layers are added to the wafers active surface serially to provide a uniform grid pattern typical of that shown in Figure 4.

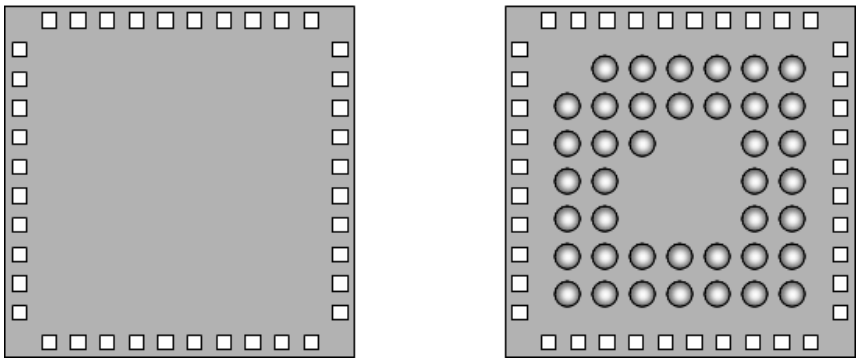
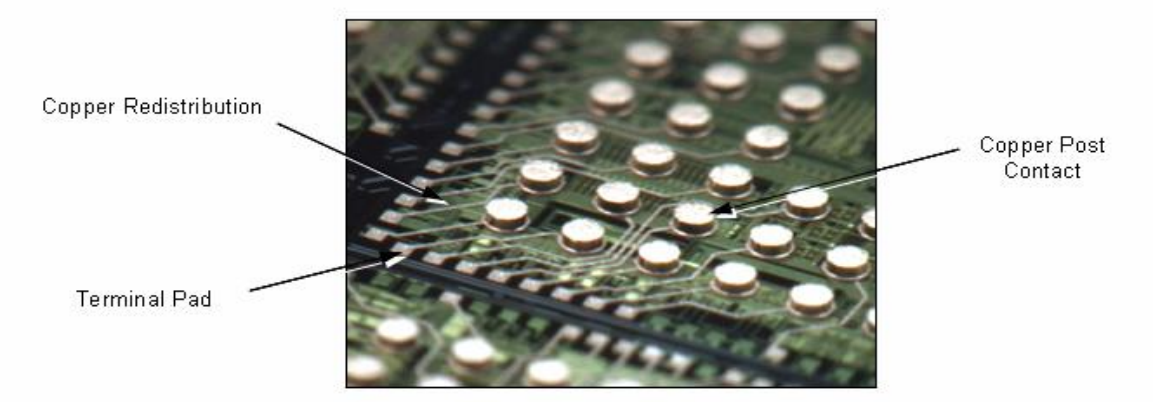


Figure 4. Comparing the 100 micron perimeter wire bond pad configuration to a redistributed 250 micron bumped array contact pattern.

Redistribution provides a uniform array and enables the developer to define a standard contact assignment that can better facilitate component level testing and board or module level assembly. Factors affecting ease of this serial approach are die size, die bond pad size and contact pitch and location selected. Dimensional control is also a vital factor in the implementation of advanced chip level assembly. Small dimensional differences can translate into the difference between success and failure in flip chip and fine-pitch chip scale technology implementation.

There are several areas that must be addressed when developing the array formatted device. These are dimensional control of the array, consistency in the geometry, and dimensions of the attachment bumps. One of the techniques developed to ensure a relatively uniform contact profile adopts a secondary copper electroplating process. Following redistribution plating and before the adhesion layer is removed, a thick polymer mask is applied and photo-imaged to expose the copper array contact features. The wafer is then exposed to additional electroplating to build-up the contact sites with a solid copper post-like feature. When the build-up process is completed the mask material and adhesion layer metallization is removed followed by surface passivation and ENIG plating on the now exposed contact features as illustrated in Figure 5.



Example source: Casio

Figure 5. Redistribution of perimeter bond pads into a raised solid copper post array contact pattern.

When all wafer level processes have been completed, the individual units are singulated using conventional wafer sawing processing. The singulated units are then placed into carrier trays and transferred to electrical test and marking operations.

Established Criteria for WLBGA Contact Features

The ball or bump contact diameter (b) as measured in a plane parallel to the seating plane (mounting surface). The measured value for each ball or bump contact is the largest such diameter for that ball or bump. The JEDEC wafer level BGA design guide states that the measured values shall lie within the ranges specified for each pitch (e) see Table 1.

Table 1
Comparing WLBGA contact pitch (e) to ball or bump contact diameter (b) range

e	b		
	Min	Nom	Max
0.65	0.35	0.40	0.45
0.65	0.30	0.35	0.40
0.50	0.30	0.35	0.40
0.50	0.25	0.30	0.35
0.50	0.20	0.25	0.30
0.50	0.15	0.17	0.19
0.40	0.20	0.25	0.30

Source: JEDEC JC-11

The array contact pitch requirement may be limited by the bumping process or by the substrate layout. The concern with redistribution is its impact on ESD, current carrying capability over device lifetime, functionality and performance. If properly designed, the parasitics of the redistribution layer(s) can be minimized compared to the

resistance and capacitance of the ESD elements. Ideally, the uncased die would be designed from the start for board level attachment.

WLBGA Redistribution process sequence:

1. Apply metal adhesion layer over active side of wafer
2. Spin-coat photo resist over the wafer surface
3. Image and develop contact pattern
4. Electroplate Ni on the exposed contact sites
5. Remove photo-resist
6. Chemically etch remaining adhesion layer metallization
7. Spin-coat photo-imageable polymer over the wafer surface
8. Image and develop polymer to expose Ni plated contact sites
9. Clean Ni plated contacts / apply electroless gold alloy

When selecting the matrix size manufacturers are advised to consider issues relating to handling and shipping systems and test socket availability.

Standards for die-size ball grid array (DSBGA) packaging

A "chip-size" (or die-size) ball grid array is a type of BGA package where the body size is defined to coincide as closely as possible with a specific die outline. The dimensions of the die-size package body will conform to the specific outline of the die, however, these body dimensions will likely change as a result of future changes in die size. The outline of the package may be square or rectangular (as shown in Figure 6), but this aspect ratio is subject to change as a given package is redesigned to conform to a new die size.

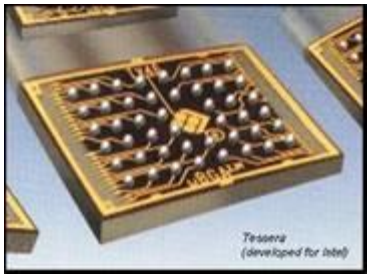


Figure 6. DSBGA packaged ICs are rarely perfectly square but they will likely be designed to furnish a uniform contact matrix for efficient second level assembly.

The JEDEC Standard 95/4.7, Die Size (DSBGA) Design Guide standard defines the physical features of the finished device. Included are the bump and ball contact size and pitch variations, controlling tolerances for position and size, maximum contact capability based on package outline and contact pitch and coplanarity limits as defined in JEDEC Standard 95, Design Guide 4.17 for Array Package Measuring and Methodology. The size of the substrate or carrier is as close to the die size as practically possible (see Table 2).

Table 2 JEDEC Standard contact pitch (e) and contact diameter (b) variations for DSBGA

e = pitch	b min.	b nom.	b max
0.80 mm	0.40 mm	0.45 mm	0.50 mm
0.80 mm	0.35 mm	0.40 mm	0.45 mm
0.80 mm	0.25 mm	0.30 mm	0.35 mm
0.75 mm	0.40 mm	0.45 mm	0.50 mm
0.75 mm	0.25 mm	0.30 mm	0.35 mm
0.65 mm	0.35 mm	0.40 mm	0.45 mm
0.65 mm	0.25 mm	0.30 mm	0.35 mm
0.50 mm	0.25 mm	0.30 mm	0.35 mm

The purpose of these design guide standards are to establish a protocol for developing mechanical outlines, mechanical conformance and to establish land pattern requirements for their attachment. The aspect ratio (outline) will likely differ for devices of the same functionality from multiple suppliers. The DSBGA design standard states that the substrate or carrier of the package may have a square or rectangular shape with a metalized circuit pattern applied to either or both sides of a dielectric structure. The semiconductor die is most likely attached, face-down, to the top surface of this dielectric carrier. On the underside of the dielectric the array pattern of metalized balls provides the mechanical and electrical connection from the package body to the next level component such as a printed circuit board.

Design for Flip-Chip and DSBGA Attachment

Board design for die size component assembly is, in general, typical of that presently used for soldered surface mount assembly. The solder mask's role in controlling the solder defects during the reflow process is significant and designers of the PC board should attempt to minimize clearance or air gap around land pattern features.

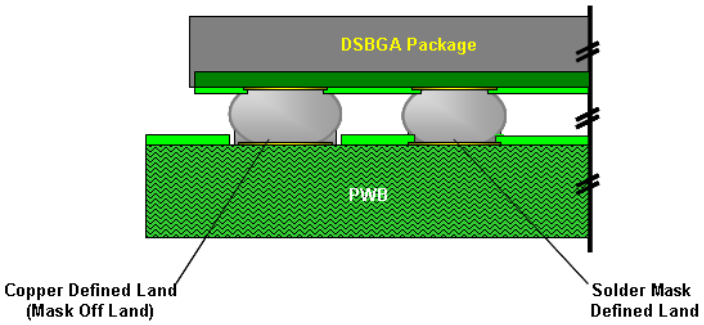


Figure 6. Comparing copper defined and solder mask defined land patterns.

After establishing the contact type (ball or bump) and diameter, determine the contact feature geometry and pitch. Land patterns developed for spherical (ball) contacts can be the same diameter as the sphere or slightly smaller, however, with lower profile bump contacts, the land pattern diameter is more likely to be the same as the bump diameter. In regard to board level solder mask for array devices, most companies are specifying a mask that is clear of the land pattern but mask must cover any conductive features between lands to prevent solder bridging.

Second Level Assembly

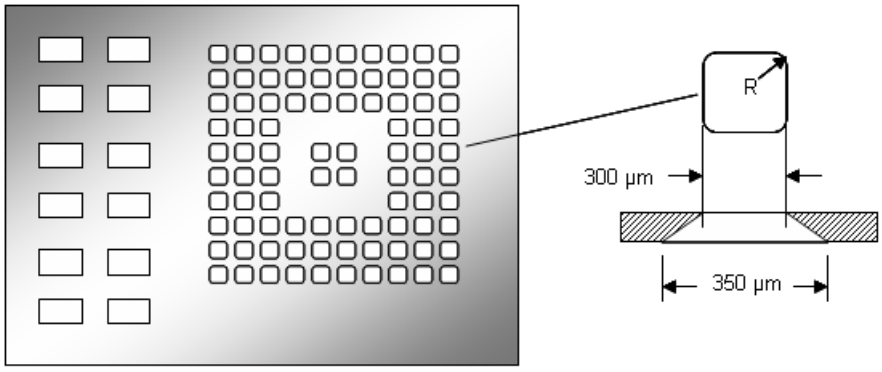
Most manufacturers and service providers in the electronics industry are well aware that to meet the RoHS directive they will need to adapt solder processes that use alloy compositions that are free of lead. And by now they know that the alloy composition finding favor for most commercial applications is basically tin with a relatively small percentage (by weight) of silver and less than one percent of copper. This so called 'SAC' alloy combination is classified as a near eutectic composition and has proved (for a majority of applications) to be a viable substitute for the lead-bearing eutectic solder traditionally used for electronic assembly. A number of concerns for the end products survivability when processed with the lead-free alloy compositions remain however. While many will find that the SAC solder joint reliability meets the stresses typically experienced for a wide number of use conditions, the higher process temperatures required to complete the joining process can adversely impact product reliability resulting from acute material degradation. One exposure to the lead-free solder process may not be of concern but repeated exposures to high process temperature, typical for more complex assemblies, may severely impact the physical integrity of the resin systems used in the circuit board laminates.

Defining stencil aperture geometry

Array packaged devices may adapt conventional SMT assembly processes where solder paste is printed onto the substrate land patterns, devices are placed and mass reflow soldered. A round or square aperture can be specified for fine-pitch array solder printing, however, those specifying the square aperture may prove more beneficial for array package applications. The square stencil pattern can increase the solder volume slightly without bridging. Another factor that has improved paste transfer on the smaller land geometry is the tapered or trapezoidal shaped wall of the opening (typical of laser cut stencils). During stencil fabrication, the opening that will be closest to the board surface should be one or two mils wider than the opening at the top surface.

To achieve a more robust solder connection on wider pitch array contact devices, process engineers may specify a slightly expanded stencil opening. This will also furnish a somewhat higher solder paste volume at each attachment site. The primary concern is that the printing process furnishes solder paste and flux to all contact sites. Many companies have adapted automated inspection as a post-printing requirement to ensure uniform and consistent solder paste print quality. If solder paste is not present on even a single contact site, a 100% solder interface of component-to-board during reflow soldering cannot be achieved.

Although the land pattern on the substrate is generally a circular shape (slightly smaller than the ball contact size), stencil openings that have a square geometry (see Figure 7) generally furnish better solder printing quality.



Source: IPC-7094

Figure 7. Laser cut stencil aperture shape can significantly improve repeatability and uniformity of solder paste transfer.

Refer to IPC-7525 for more detailed guidelines in developing solder stencils.

In regard to assembly processing, placement accuracy and cycle time are factors that contribute most significantly to the overall assembly cost.

Ultra Fine-Pitch BGA Attachment

A wide range of choices exist for both low and high volume assembly of ultra fine-pitch flip-chip and die-size surface mount devices. When the contact pitch is less than 400 microns it is common to attach the device using only flux. The solder attach process begins with pickup and machine vision inspection of the device outline. Flux is applied to either the device contacts using a dip-transfer process or applied directly onto the contact pattern on the substrate. To ensure that a satisfactory electrical interface is made, the die must be precisely aligned over the corresponding lands provided on the substrate. The attachment is completed when the fully populated substrate passes through a reflow furnace.

Underfill Requirements

Although epoxy underfill is not required for all DSBGA package technologies or for WLBGA that are no greater than 5.0 mm square, consideration should be given to the compatibility of the underfill with the solder process and the surface condition of the substrate. In regard to the solder paste and tacky flux, residues that remain on the substrate or components surface after the reflow solder process must be removed. This may also be a factor for the no-clean fluxes where residues may be minimal but, any residue may prove incompatible with the underfill chemistry and restrict the uniform flow needed to promote an underfill that is free of random voiding.

The IPC-J-STD-030, Guidelines for Selection and Application of Underfill for Flip-Chip and Other Micro-packages covers organic underfill materials that match the coefficient of thermal expansion of the underfill material to the flip-chip solder bumps in order to relieve the stress on the solder joints due to thermal cycling. This standard is intended to deal with the materials used for underfill of flip-chips or chip scale packages. The use of underfill will substantially increase the fatigue life of solder bump connections, particularly when the substrate material has a substantially different CTE than the flip-chip or die size package. The flip-chip underfill material composition selected should have a CTE that matches closely the CTE of the solder material used and should not contain any elements that could adversely affect the reliability of the device (ionic impurities or alpha emitters) or adversely affect the electrical performance of the device.

Conclusion

It is important that the user of flip-chip and die-size BGA technologies have a fundamental understanding of the intrinsic material properties and on the design/process driven dimensions for their application. The use environment of the product must be well defined and include factors involved in potential solder joint fatigue. The package design and assembly process can affect the reliability in terms of presence of under-fill, the symmetry of interconnect pattern, misalignments and variations of bump geometries and overall device size. The different surface mount solder attachment compositions can have significantly varying failure modes. Solder joints with essentially uniform load

distributions will typically show similar behavior. Solder joints with non-uniform load distributions, e.g., those on flip-chips and WLBGA components or non compliant DSBGA show localized damage concentrations with the damage in the form of macro-cracking.

The IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments document notes that solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches and are made of a material, solder, that itself has properties significantly different than the bonding structure materials, causing local thermal expansion mismatches. The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment. Underfill can substantially enhance fatigue life. When the underfill is applied correctly, it reduced the solder joint strain level by constraining the expansion of the interconnect materials to be used in a wider range of environments and lager DSBGA device sizes can be accommodated. Underfill material, when needed, must be selected to ensure that it adheres to the assembly surface, but does not adversely stress the interconnect joints. The material must have properties which allow easy application to avoid process defects, and it also must not contain or trap contaminants which could initiate corrosion related problems.

Applicable Documents and Standards

Various standards and design guidelines are applicable in the development of the basic die element, the uncased flip-chip and packaged die. Some documents relate directly to features required for mounting the component, contact size, pitch and array configurations. In any event, the standards and guidelines are furnished for very specific reasons and designers should consider a review of the following resources:

IPC-2221 Generic Standard on Printed Board Design
IPC-2223 Sectional Design Standard for Flexible Printed Boards
IPC-7071 Generic Requirements for Component Mounting
IPC-7075 Sectional Requirements for High Pin Count Area Array Component Mounting
IPC-7076 Sectional Requirements for Chip Scale and Chip Size Component Mounting
IPC-7077 Sectional Requirements for Wire Bonding Bare Chip Component Mounting (Chip on Board)
IPC-7078 Sectional Requirements for Flip Chip Component Mounting (Direct Chip Attach)
IPC-7094 Design and Assembly Process Implementation for Flip Chip and Die Size Components
IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments
IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments
IPC-9702 Monotonic Bend Characterization of Board-Level Interconnects
IPC-9703 Physical Shock Test Methods for Surface Mount Solder Attachments
IPC-J-STD-030 Guidelines for Selection and Application of Underfill for Flip-Chip and Other Micro-packages
JEDEC Publication 95 Mechanical Outlines of Solid State and Related Products

- **Section 4** Design Guides
- **Section 4.5** Fine-pitch, Square Ball Grid Array Package (FBGA)
- **Section 4.7** Die-Size Ball Grid Array Package (DSBGA)
- **Section 4.17** BGA (Ball Grid Array) Package Measuring and Methodology
- **Section 4.18** Wafer Level Ball Grid Arrays (WLBGA)

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Topics of Discussion:

1. Flip-chip and Chip-size package applications
2. Flip-chip and Chip-size IC package standards
3. Land pattern and circuit routing guidelines
4. PCB fabrication and assembly process criteria

Flip-chip and Chip-size Package Applications

Consumer Electronics

- Digital watches
- Cameras
- Calculators
- Toys and games

Business Equipment

- Programmable keys
- Smart cards
- Inventory control
- Electronic security
- Sensors

Communications

- Phone cards
- Cellular phones
- Fiber optic translators
- Displays

Computers and Peripherals

- Hand held computers
- Schedulers
- Print head drivers
- Disc drive controllers

Flip-Chip Advantages And Disadvantages

Advantages

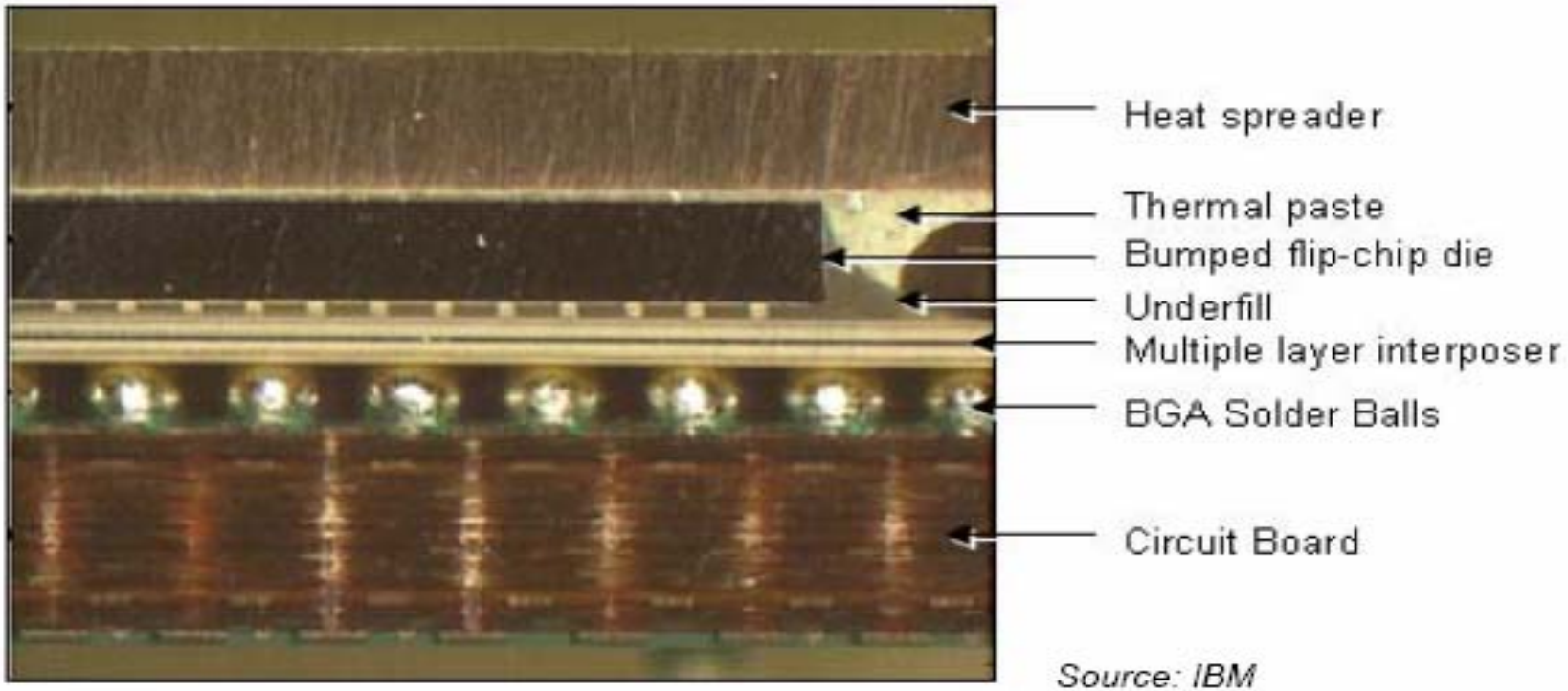
- Low cost (in high volume)
- Light weight
- Thin, low profile assemblies
- Smaller overall assembly
- Faster signal processing
- Simplified structure
- Possibly shorter product development cycles (packaging step is avoided)

Disadvantages

- Requires handling bare die
- Know good die concerns (limited ability to burn in)
- Different assembly tools and skills are required, underfill
- Repair is difficult to impossible
- Test of assembled circuits difficult
- Metallurgy & cleanliness critical
- Responsibility for yield is with the assembler

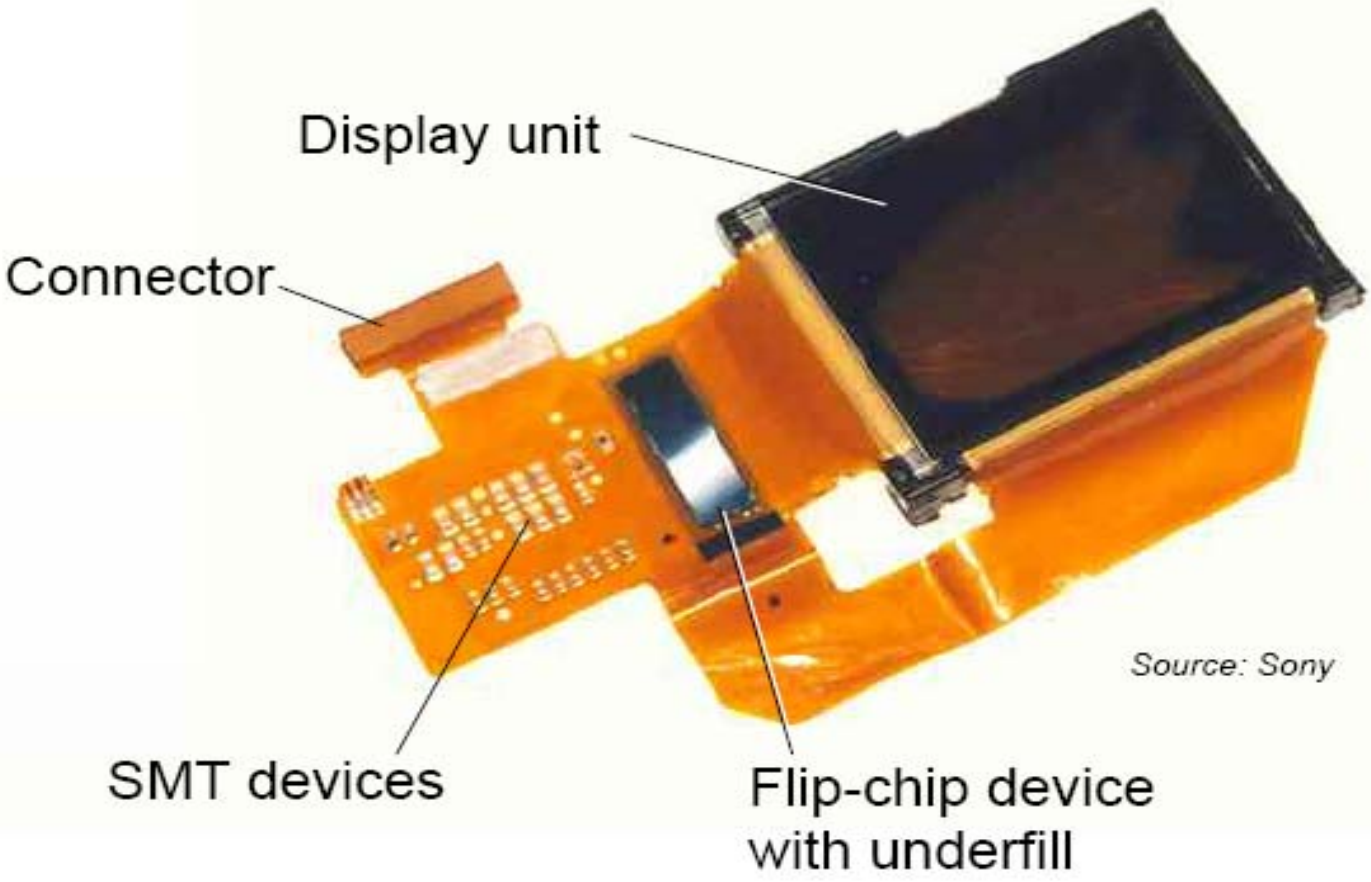
Flip-chip on Package Application

- High I/O flip-chip on multilayer BGA configured interposer structure.



Source: IBM

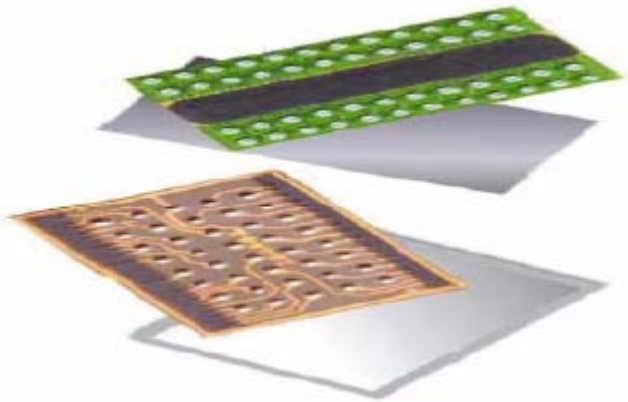
Chip-on-Flex Display Assembly



Color display for i-mode handset

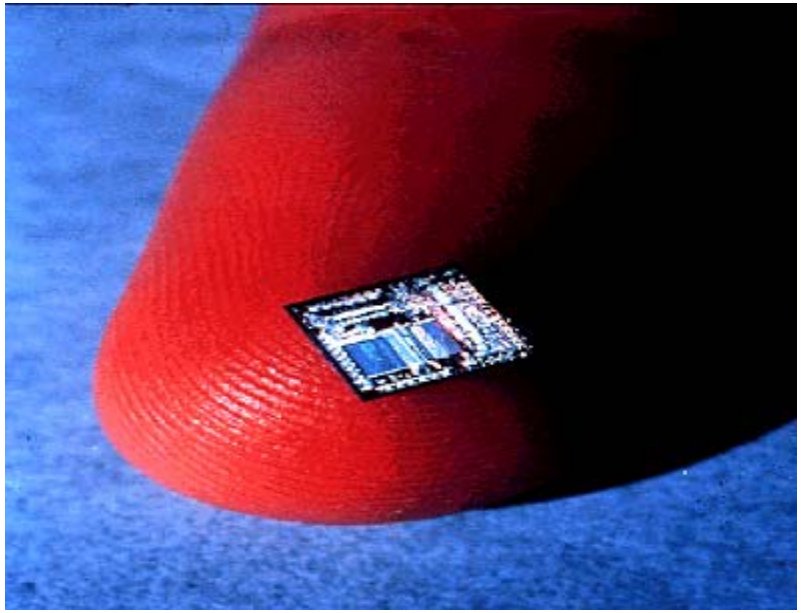
Standardization

Standards have been developed to support incased and uncased chip-size package requirements.



These standards relate to only the physical attributes and tolerance of the packaged die outline not the materials or method of manufacture.

Die Face Down Flip-Chip and Die Size Package Variations:



- Direct (Bumped) Chip Attach
- On Die Redistribution
- Wire Bond and Lead Bond
- Stud Bump Wire Form
- Flex-Lead µBGA

Defining Known Good Die

Bare Die Quality Classification

Level	Visual Mechanical Inspection	Electric Characteristics	Early Failures	Long term Reliability
Level 1 (Known Good Die)	Sampling specified on products spec.	All test items* assured	Assured**	Assured**
Level 2 (Known Tested Die)	Sampling specified on products spec.	All test items* assured	Not assured	Not assured
Level 3 (Probed Die)	Sampling specified on products spec.	Some tests skipped	Not assured	Not assured

* Corresponding to the final inspection items for packaged products

**The same level as packaged products (Including Burn-in)

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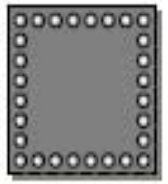
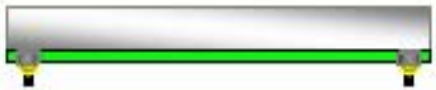
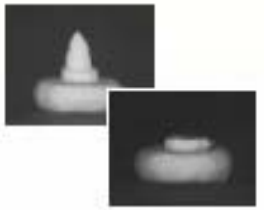
Flip-chip Contact Variations

Bumped Die

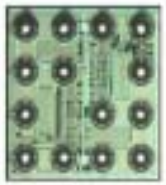




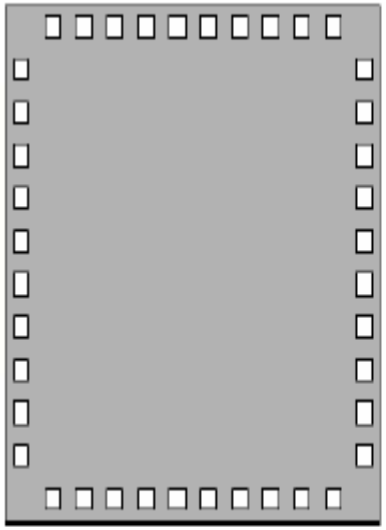
Stud Wire Bump



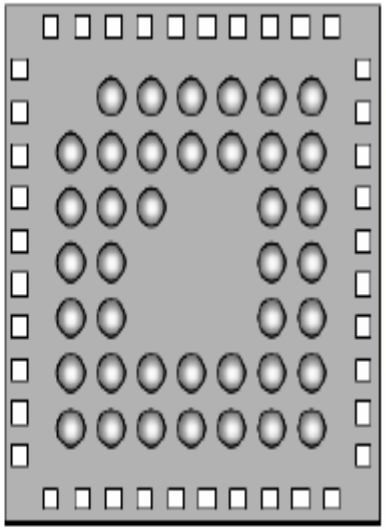
Redistribution



Bond Site Redistribution



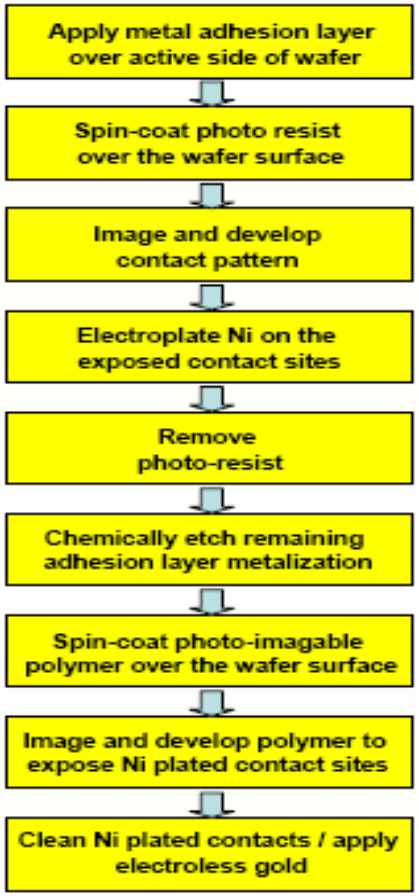
100 micron spacing

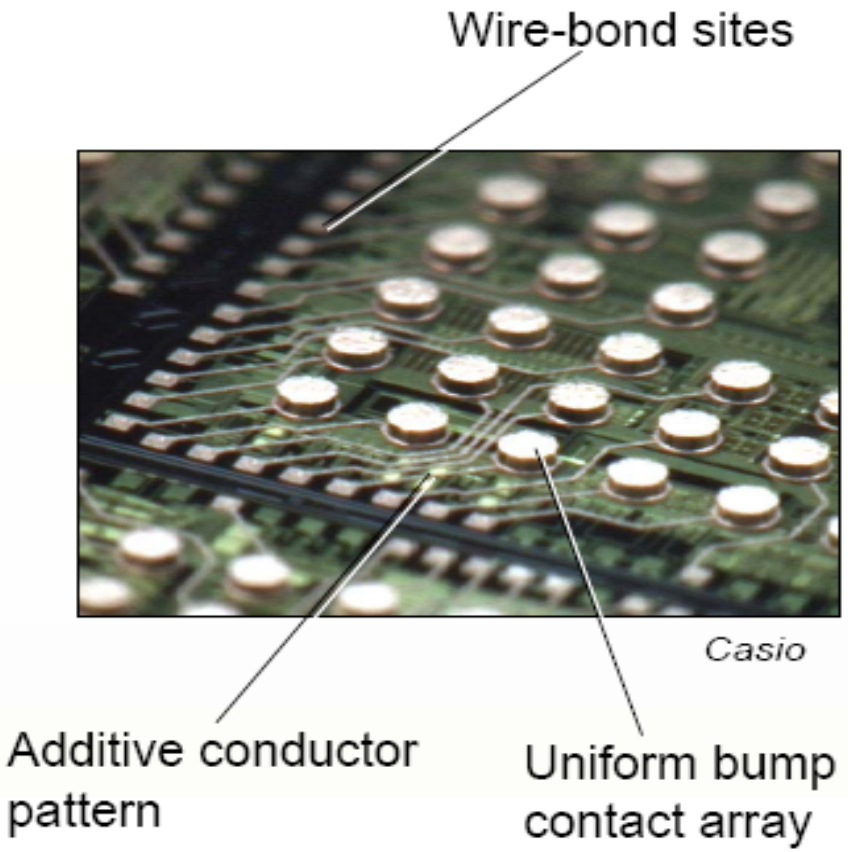


250 micron spacing

Redistribution provides a uniform array and enables the developer to define a standard contact assignment that can better facilitate component level testing and board or module level assembly.

Surface Redistribution Process





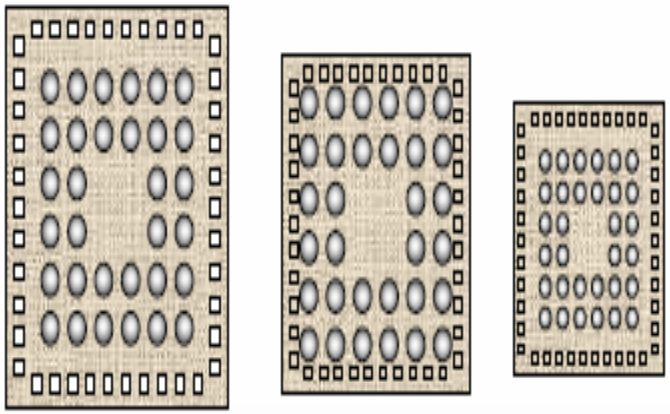
WLBGA Contact Standards

Contact pitch	Ball diameter		
	Min	Nom	Max
0.65	0.35	0.40	0.45
0.65	0.30	0.35	0.40
0.50	0.30	0.35	0.40
0.50	0.25	0.30	0.35
0.50	0.20	0.25	0.30
0.50	0.15	0.17	0.19
0.40	0.20	0.25	0.30

Source: JEDEC JC-11

Die Shrink Concerns

WLP poses the challenge of designing a die sized package with a footprint that remains constant despite die-shrink.



Die may shrink by 5% to 10% from one generation of a die to the next.

Challenges for the User

- Selection of wafer level products having a relatively high fabrication yield.
- Confident that the wafer fabrication process has been stabilized and is not subject to significant change.
- Process utilized for WLP is mature and will deliver a reliable finished product.
- Establish a reliable source of supply for both near term and long term.

Mechanical Outline Standards for Chip-Size (Die-Size) Packaging

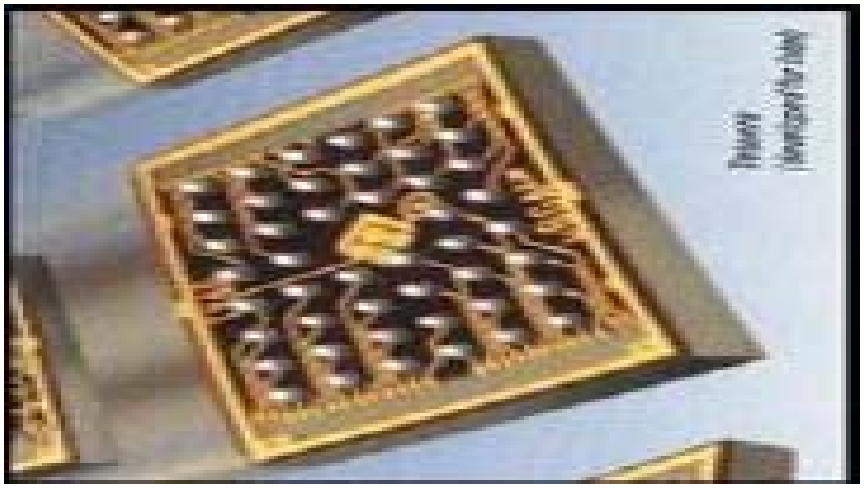
A "chip-size" (or die-size) ball grid array is a type of BGA package where the body size is defined to coincide as closely as possible with a specific die outline.

The DSBGA package is sometimes called a "real chip-size" BGA or CSP.

The dimensions of the die-size package body will conform to the specific outline of the die, however, these body dimensions will likely change as a result of future changes in die size.

Standards for die-size ball grid array (DSBGA) packaging

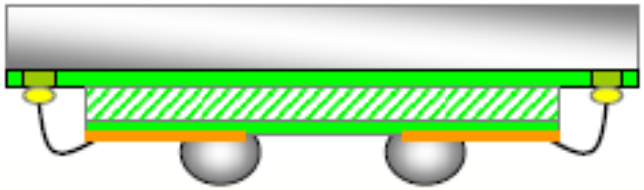
A “chip-size” (or die-size) ball grid array is a type of BGA package where the body size is defined to coincide as closely as possible with a specific die outline.



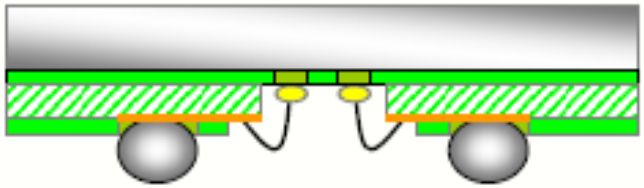
Source: Tessera

DSBGA packaged ICs are rarely perfectly square but they will likely be designed to furnish a uniform contact matrix for efficient second level assembly.

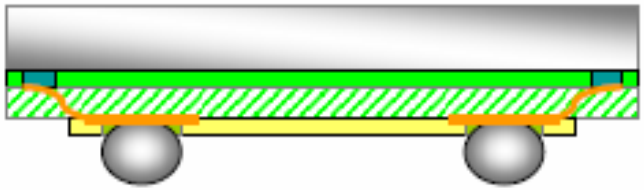
Chip Size Package Technology



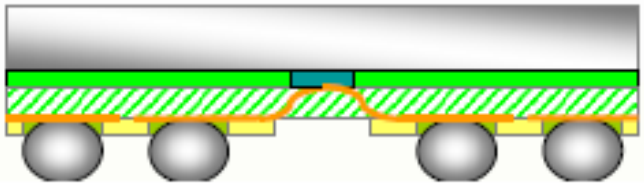
Wire Bond
(perimeter bond pad)



Wire Bond
(center bond pad)



Flex-Lead µBGA
(on polyimide film)



Flex-Lead µBGA
(center bond pad on polyimide film)

DSBGA Standard Contact Size and Pitch Variations (mm)

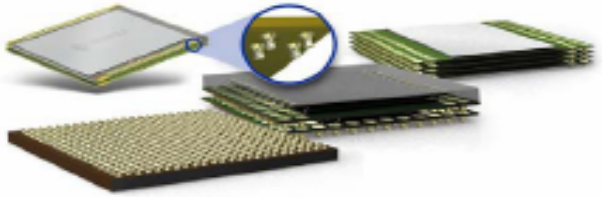
e = pitch	b min.	b nom.	b max
0.80 mm	0.40 mm	0.45 mm	0.50 mm
0.80 mm	0.35 mm	0.40 mm	0.45 mm
0.80 mm	0.25 mm	0.30 mm	0.35 mm
0.75 mm	0.40 mm	0.45 mm	0.50 mm
0.75 mm	0.25 mm	0.30 mm	0.35 mm
0.65 mm	0.35 mm	0.40 mm	0.45 mm
0.65 mm	0.25 mm	0.30 mm	0.35 mm
0.50 mm	0.25 mm	0.30 mm	0.35 mm

Source: JEDEC JC-11

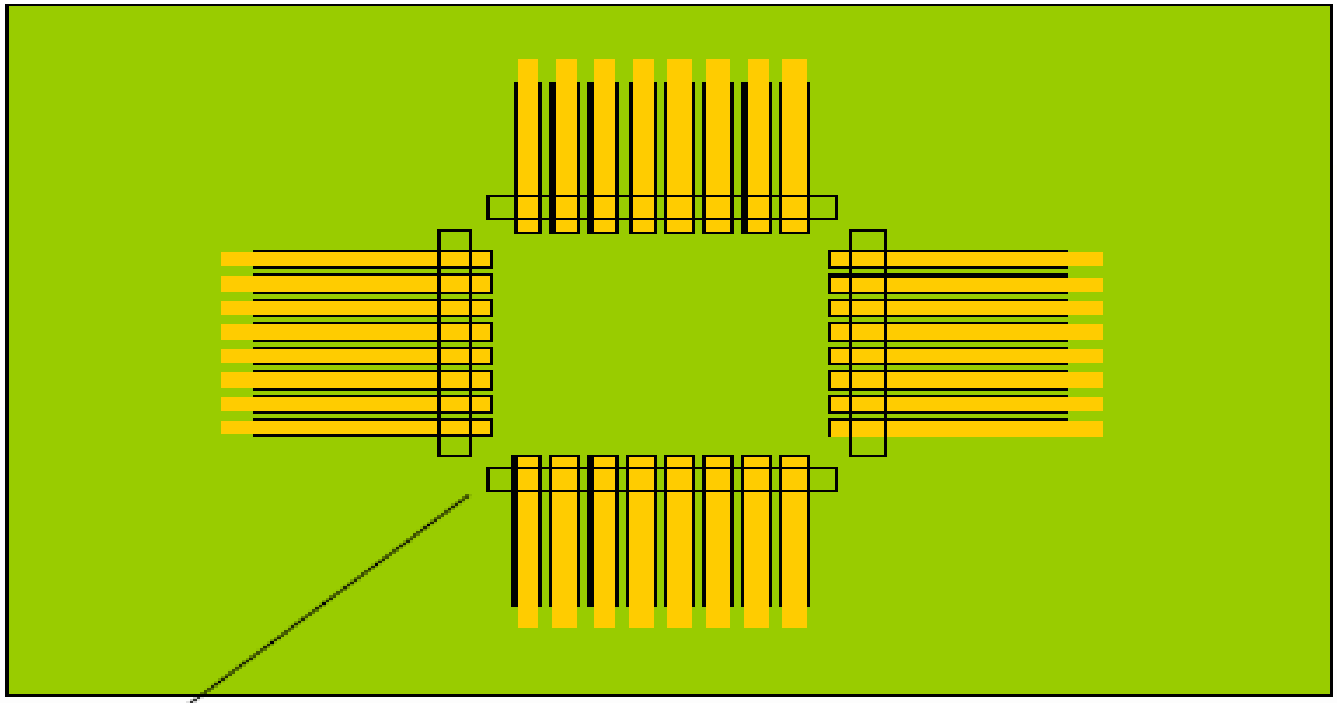
Array Package Design Standards

- JEDEC Publication No. 95, Section 4-
  Design Requirements for Outlines of Solid State and Related Products

- JEP95 Section 4.5 - Fine Pitch (Square) BGA Package (FBGA)
- JEP95 Section 4.6 - Fine Pitch (Rectangular) BGA Package (FRBGA)
- JEP95 Section 4.7 - Die-Size Ball Grid Array Package (DSBGA)
- JEP95 Section 4.10- Generic Matrix Tray for Handling and Shipping
- JEP95 Section 4.14- Ball Grid Array Package (BGA)
- JEP95 Section 4.17- BGA Package Measurement and Methodology
- JEP95 Section 4.22- Fine Pitch Square Ball Grid Array Package (FBGA) Package on Package (PoP)



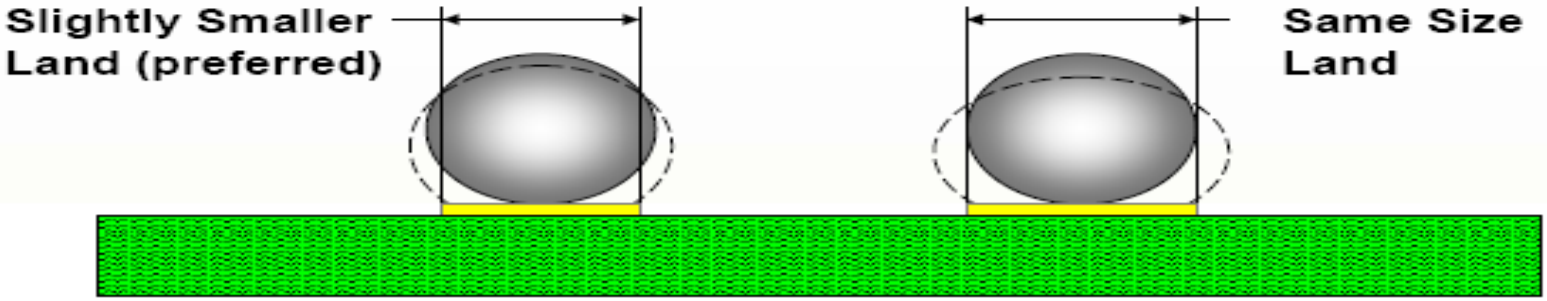
Providing for Flip-Chip Attachment



Slot openings in solder mask provides access for mounting onto the narrow conductor circuit

Array Package Land Pattern Development

Nominal Ball Diameter	Recommended Land Diameter	Approx. Reduction
0.75 mm	0.55 mm	25%
0.60 mm	0.45 mm	25%
0.50 mm	0.40 mm	20%
0.45 mm	0.35 mm	20%
0.40 mm	0.30 mm	20%
0.30 mm	0.25 mm	20%



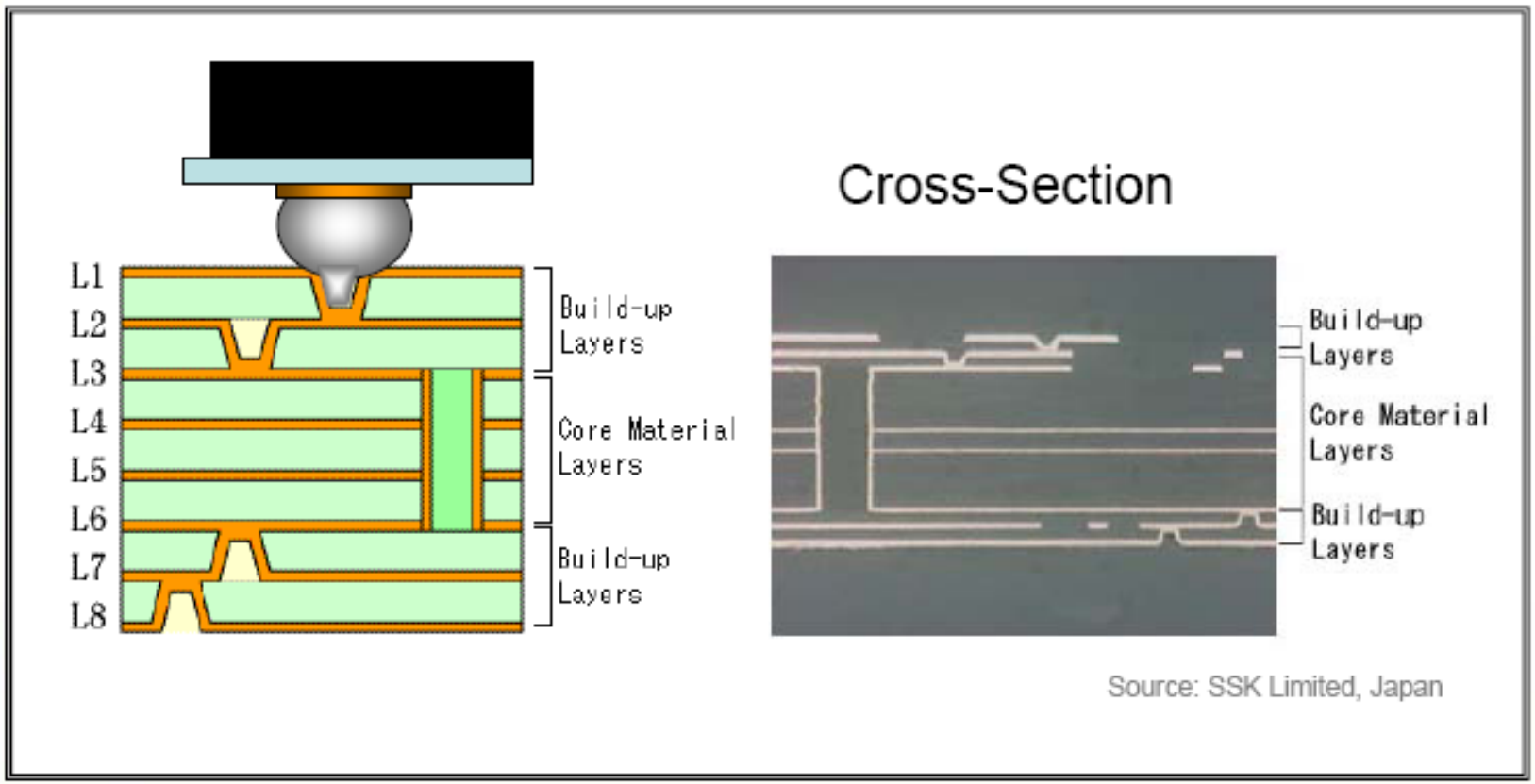
Source: IPC-7095

Consider Benefits of Via-in-Land

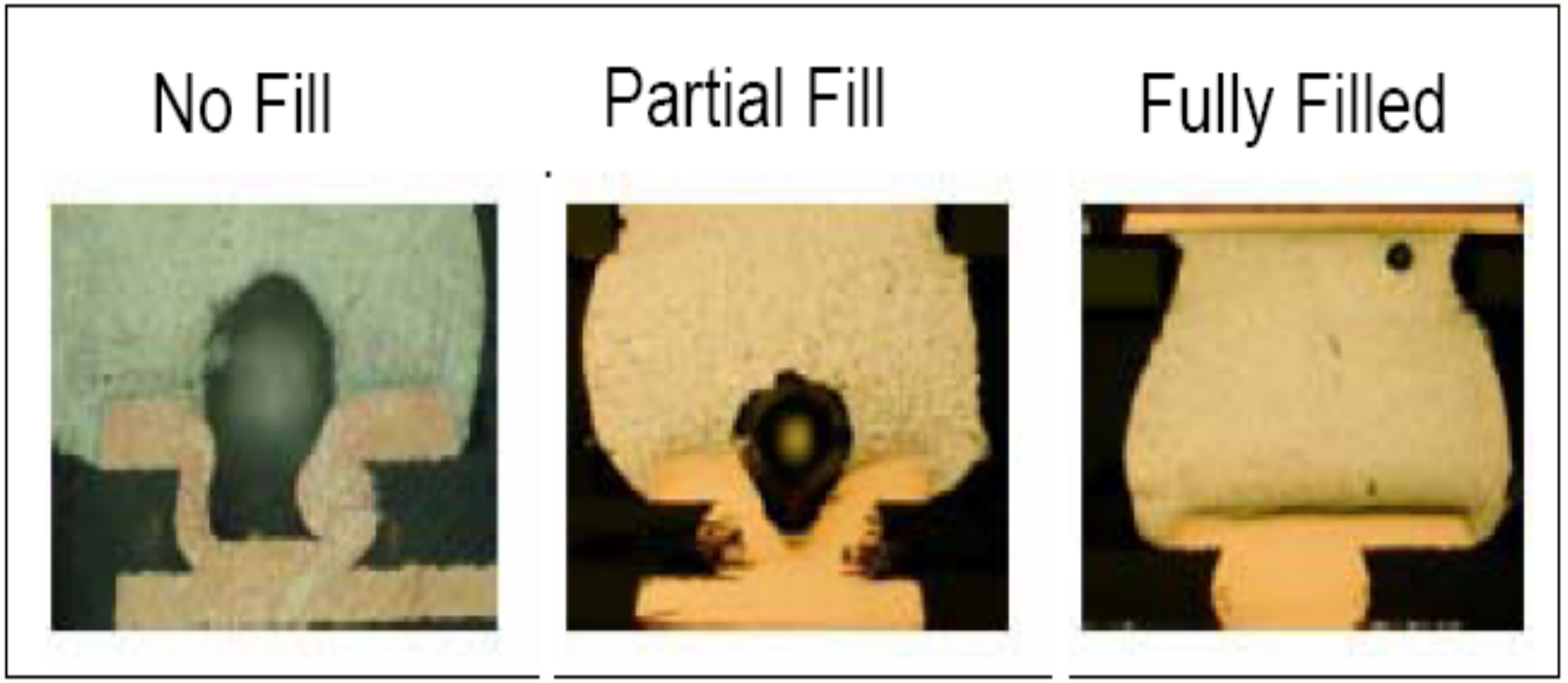
- Higher Component and Circuit Density
- Subsurface Circuit Routing
- Enables Finer Lines and Spaces
- Shorter Circuit Path Enhances Performance

Plated Via-in-Land attachment site is physically stronger than non-supported lands.

8 Layer Via-in-Land Board Example
2 + 4 + 2 Construction



Plating to Fill Via Will Minimize Void Propagation



Examples courtesy of Cookson

Circuit Routing for High Density FC-CS Array Applications

Status of Organic IC Substrate Interposer Fabrication Capability

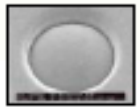
Design features (µm)	Conventional	Leading Edge	State-of-the-Art
Conductor Width & Spaces (minimum)	40 / 40	30 / 30	15 /15
Plated Hole Diameter (minimum)	200	150	100
(Microvia Diameter (minimum)	100	75	50

Source: IPC 2006-2007 Industry Roadmap

1.5 mil

8 mil

4 mil



Assembly Process Options

- Ultrasonic Gold-to-Gold Interconnect
- Conductive polymer dispense, place and cure
- No-flow underfill print, place and reflow
- Flux dip, place and mass reflow
- Solder paste dip, place and mass reflow
- Solder paste print, place and mass reflow

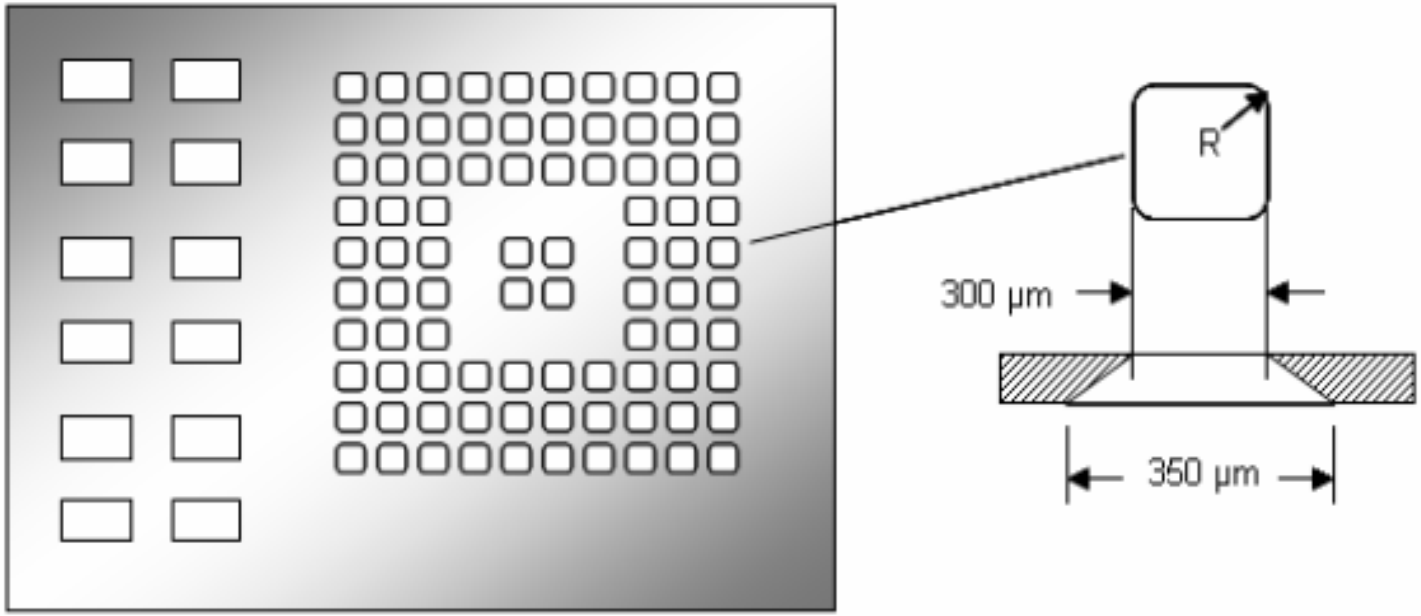
Solder Paste Printing

- To achieve a more robust solder connection on wider pitch array contact devices, process engineers may specify a slightly expanded stencil opening.
- This will also furnish a somewhat higher solder paste volume at each attachment site.
- The primary concern is that the printing process furnishes solder paste and flux to all contact sites.
- Many companies have adapted automated inspection as a post-printing requirement to ensure uniform and consistent solder paste print quality.

If solder paste is not present on even a single contact site, a 100% solder interface of component-to-board during reflow soldering cannot be achieved.

Stencil Design for DSBGA

(0.50 mm pitch example)



Refer to IPC-7525 for more detailed guidelines in developing solder stencils.

Solder Stencil Development for Flip-Chip and DSBGA

Defining Stencil Aperture and Geometry-

- **Changing the shape of the openings from round to square has proved beneficial for array package applications.**

The square stencil pattern serves two purposes:

1. It can increase the solder volume slightly when adapting the smaller pitch devices.

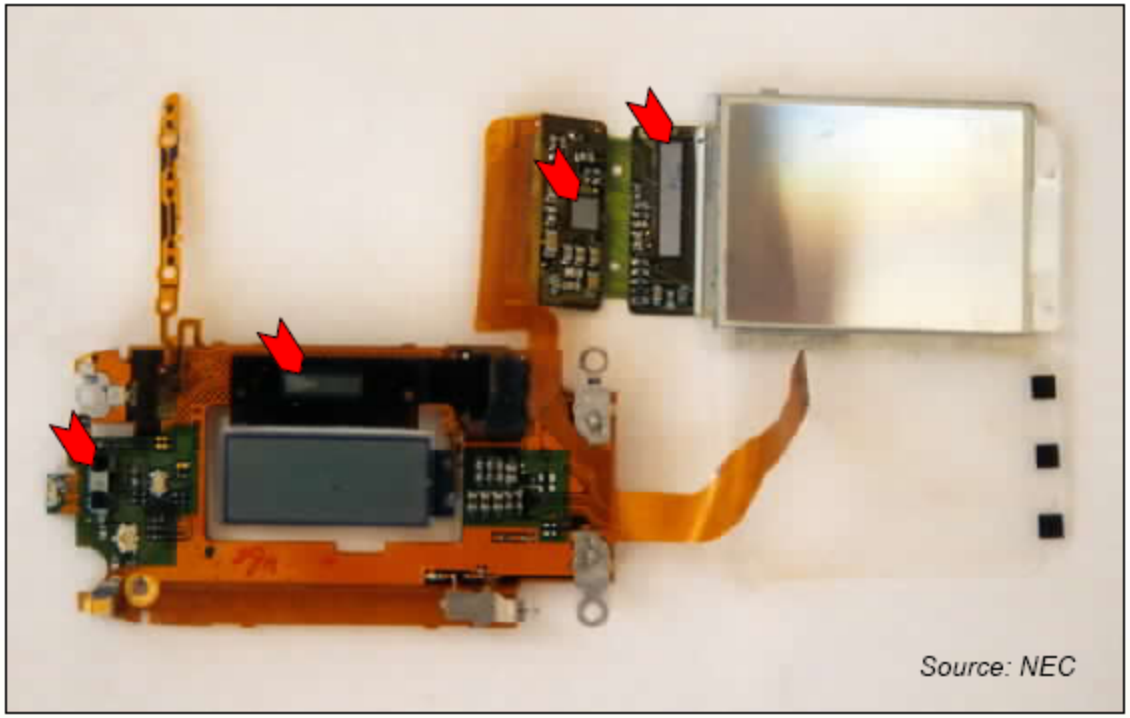
2. The square trapezoidal pattern releases paste from the stencil surface more uniformly.

Specifying Stencil Aperture Size

Contact / Pitch	Land Dia.	A (Aperture Size)*
0.10 / 0.20	0.10	0.10
0.12 / 0.25	0.12	0.12
0.15 / 0.30	0.15	0.15
0.20 / 0.35	0.18	0.20
0,25 / 0.40	0.20	0.25
0.30 / 0.50	0.25	0.30
0.30 / 0.65	0.25	0.30 – 0.40
0.40 / 0.65	0.35	0.40 – 0.45
0.30 / 0.80	0.25	0.30 – 0.40
0.40 / 0.80	0.35	0.40 – 0.45
0.50 / 0.80	0.40	0.50 – 0.55

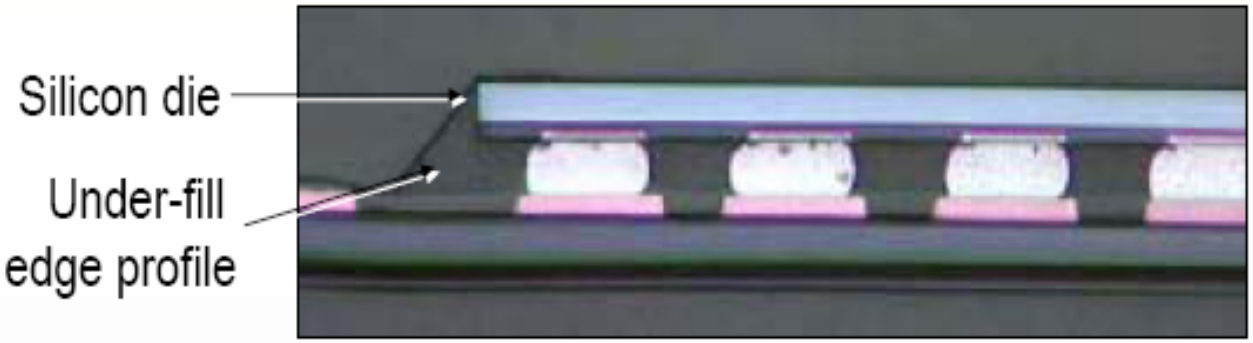
**** Larger aperture recommended for over-print***

Flip-Chip and SMT on Rigid-Flex Circuit for NEC Handset



Under-fill

- Under-fill is used in a wide variety of packages and board level assemblies.
- The "part" to be under-filled can be either an uncased die or a packaged DSBGA substrate.



Source: Auburn University

IPC-J-STD-030 offers guidelines for selection and application of underfill for flip-chip and other micro-packages

Summary and Conclusions

- It is important that the user of flip-chip and diesize BGA technologies have a fundamental understanding of the material properties and assembly process variations.
  - The use environment of the product must be well defined and include factors involved in potential solder joint fatigue.
  - The package design and assembly process can affect the reliability in terms of presence of under-fill, the symmetry of interconnect pattern, misalignments and variations of bump geometries and overall device size.

Relevant IPC Documents…

- IPC-7094, Design and Assembly Process Implementation for Flip Chip and Die Size BGA.
- IPC-7095, Design and Assembly Process Implementation for BGAs.
- IPC-A-610, Acceptability of Electronic Assemblies.
- IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard