The Embedded Passives Journey

Bill Devenish – Harris Corp., Mechanical Advanced Development (MAD)
Andrew Palczewski – Harris Corp., PCB Technologist

Abstract
When planning a trip for the first time there is usually a significant amount of planning and preparation involved. First, the destination is chosen that meets the objective (e.g. Las Vegas for a conference). Next, guidebooks and maps are consulted to chart the route, minimize travel time and cost, and avoid pitfalls along the way such as running out of gas, overheating the engine or not having money for the tolls. The same planning process is generally used in many companies to introduce new technologies. Embedded passives are one of those new technologies in which many companies have an interest in implementing. There is a tremendous amount of hype and excitement in available literature related to the use of embedded passives. Most available information highlights the positive aspects of the technology, with a few negatives sprinkled in occasionally. What is missing happens to be the travel guide that helps a development program avoid the roadblocks, detours, and hazards associated with embedded passives. This paper can be one of those guidebooks. It will highlight the difficulties encountered while implementing embedded passives. It will bring to light some of the design and tool issues, as well as the issues of matching material with board fabricator that appeared along the journey. Those items that were successful will also be shared. So make sure your seat belt is fastened, your tray table is in its upright and locked position, and learn from our journey of implementing embedded passives.

Introduction
RF Communications is a division of Harris Corporation that designs and builds tactical two-way radios for various government and military customers. The main engineering and manufacturing facilities are located in Rochester, New York. Our story begins with the creation of a MAD team within RF Communications. The purpose of MAD, Mechanical Advanced Development, is to reduce the risk of introducing new technology and processes into the latest products. These new technologies and processes are targeted to help meet the goals of reducing product size, cost and time-to-market. A key component of risk reduction for the team is researching, evaluating and testing technologies and processes before they become critical path in a project. This paper summarizes the embedded passives journey that the MAD team undertook at Harris.

Choosing a Destination
The MAD team approached the objective of implementing embedded passives as if taking a trip, with the first activity targeted at setting a travel objective. The team needed to know where they had been, where they currently were, and where they wanted to go. A technology roadmap was the ideal tool for assisting with the choice of destination. The roadmap showed that for decades there has been a trend to reduce the size of electronics while at the same time increasing product functionality and lowering cost. This is especially evident in the consumer electronics world with portable devices like phones and music players continually shrinking in size. The typical consumer has come to expect electronic devices to be small, feature-rich and inexpensive. This same expectation is becoming a part of the mind-set of the typical tactical radio user as well. The customer expects new tactical radios to be small, light-weight and as easy to use as a cell phone. One of the key technologies identified by the MAD team in the roadmapping process was embedded passives. For this report, embedded passives primarily refers to replacing discrete passive components, such as resistors and capacitors that are assembled on the surface of a printed circuit board, with layers of specialized material embedded in the stack-up layers of the actual PC board.

With the travel objective of embedded passives established it was time to identify interesting sights to see along the journey. In other words, what were the benefits of incorporating this technology? The primary benefit highlighted in the roadmapping exercise for considering embedded passives was size reduction by eliminating discrete passive components from the surface of the PC board in order to shrink the overall outline of the board.

As the MAD team continued researching embedded passives through the reading of available literature and attendance at conferences they became aware of other potential benefits. These benefits included increases in board assembly yields, performance improvements, and in some cases, cost reduction due to decreased part count. This was shaping up to be an interesting journey.

Planning the Trip

With the destination chosen it was now time to plan the trip. Typically, trip planning begins with looking at a map. Many people usually look at a map to see where the destination is located and then backtrack to see its relation to the starting point. As routes on the map are scanned the plan begins to take shape. The general direction is determined, waypoints are identified and estimates of how long the journey will take come together in formulating the plan.

The MAD team used the same approach as the plan was created to implement embedded passives in the redesign of an existing board. It was decided to proactively begin working with embedded passives before a project specifically identified the need to allow for the evaluation to be conducted in advance of it becoming a critical path item for a project. It was also decided to redesign an existing board for use as a test board to keep the variables to a minimum.

The team set a goal to reduce the area used by the components on the test board by 25%. This was based on information from the available literature, with a lot of guesswork thrown in. A preliminary evaluation of the Bill of Material identified resistor and capacitor values that could be targeted for embedding. The targeted resistors, consisting mostly of pull-up, pull-down, and termination values, can be seen as the spikes in figure 1, while the targeted capacitors, consisting mostly of by-pass and de-coupling values, are seen in figure 2.

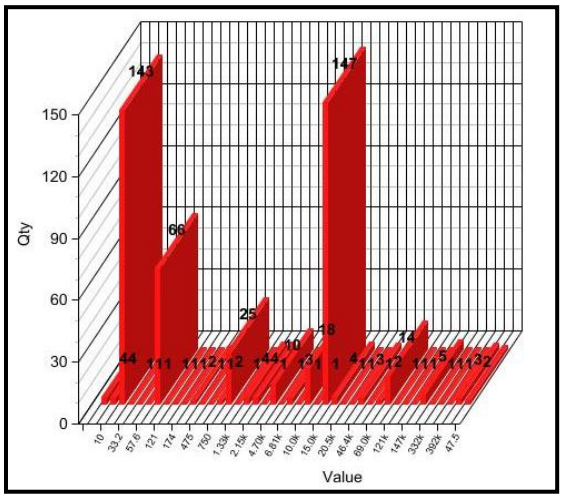


Figure 1: Resistor Quantity

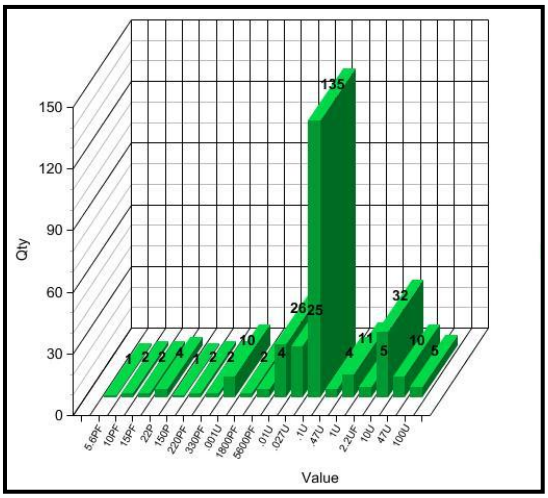


Figure 2: Capacitor Quantity

Since no estimating tools were readily available, the team put together a simple spreadsheet to identify what the potential area savings might be if the targeted resistors and capacitors were replaced with embedded material. The resistors and capacitors accounted for 29.3% of the component area on the board. This indicated that the team was moving in the right direction. Once the open space, connectors and mounting holes were eliminated from the total area on the board it turned out that the estimated component area reduction matched the original goal of 25.0%.

The MAD team was comfortable with the route for the journey but then had the task of guesstimating the travel time, or put another way, throwing darts at the schedule. A number of factors were considered in estimating the ultimate length of time for the project. This project was one of many being conducted at the same time, using the same resources, therefore the engineers were limited in the amount of time allocated to the effort. With no prior experience, the unknowns were unknown. Also, the material suppliers and fabricators were graciously providing their services at little, or no, cost so obviously other concerns could easily become a higher priority for them. After weighing these factors the team felt confident that they could design, fabricate and assemble a test board within 18 months. The route and schedule had been set.

Occasionally, someone who is planning a trip might seek advice from a travel agent. The idea is to gather additional information and insights that would be helpful in planning and taking the trip. Listed below are some of the experts that the MAD team consulted and who were eager to provide assistance.

Dr. Richard Ulrich, University of Arkansas (www.uark.edu)
CALCE, University of Maryland (www.calce.umd.edu)
Mike Fitts, Plexus Technology Group (www.plexus.com)
Happy Holden, Mentor Graphics (www.mentor.com)

Airport Arrival (Design)

There are numerous ways for getting to the airport, such as car, subway, bus or taxi. For those choosing to travel to the airport by car there are also various methods for finding the way there. Maps can be consulted, directions obtained, signs followed, or more recently, a GPS navigation device can be used. The MAD team chose to use GPS to get to the airport.

Since the team only had cursory knowledge of embedded passives, it was determined to enlist the services of an expert who could help guide the way. Mike Fitts, with Plexus, was contacted by the team to be the GPS system. Mike has tremendous experience with embedded passives and arrangements were made to have Mr. Fitts and Plexus assist Harris with converting the existing digital board to one with embedded passives.
The search for a parking space becomes the first task upon arrival at the airport. This is similar to finding and choosing the materials used for embedding passives. Before the materials could be chosen it was important to understand how the materials were going to be used. The team classified embedded passives generally into two categories, digital circuits and RF circuits.

For digital circuits, most resistive elements are pullup, pulldown or terminating resistors, and the majority of the capacitive elements are used for bypass or decoupling. Some of these elements do not require a high level of accuracy and they can accept wide ranges of tolerance in the value and operating features.
For RF circuits, embedded passives need to hold a tighter tolerance in value and operating range that will require the use of discrete or mezzanine features for buried capacitance and the use of a laser to trim the resistive element to a 1% value. For this project it was determined not to use any RF circuits as part of the conversion, with the focus on the digital circuit.
The first focus was on the capacitive materials. It was decided to leave the bulk capacitance on the board in the form of SMD components and attempt to identify and replace all of the decoupling capacitors rated from 0.1uF and below. Anything above 0.1uF would be very difficult to convert with the available materials. These materials have been in use for quite some time now, with many portable electronics products incorporating some sort of buried capacitance within the boards. The material is placed between a power and ground layer, and with high Dk material it is possible to get some sort of capacitance per square inch, whether it's in nano-farads or pico-farads.

Since this design was more about proving the capabilities of embedded capacitance as opposed to looking at it from a manufacturing and cost aspect it was determined to focus on getting the maximum amount of capacitance per square inch out of the material as opposed to what was the easiest material to use in fabrication. The material chosen, Oak-Mitsui FaradFlex BC16T, has a thickness of 16 microns and a Dk of 30 at 1MHz. Based on the area of the board and the capacitance requirements there would need to be two layers of the FaradFlex material. After calculating the total capacitance to be replaced and comparing it to the total embedded capacitance available, the ratio was estimated to be 55:1.

For resistance there are two different types of materials available. One material is a polymer thick film (PTF) which is screened on top of the copper foil layer after etch. It's generally inexpensive and easy to apply. There can be up to three different values on a single layer. This additive process is not readily available in North America and is more common to see in the Pacific Rim countries that are using buried resistors. PTF resistance materials are also known for having issues with stability over time, especially as a result of moisture absorption.

The other method for creating embedded resistance is with the use of resistive foils. This is more common in North America because resistive foil is more conducive to the processes that printed circuit board fabricators are familiar with. Resistive foils use a subtractive process. The process for creating buried resistors is best described through information found on the material vendor’s websites. They provide very good information on how these resistors are etched from the materials, leaving behind only the resistive material for the values desired.

There were almost two dozen resistive and capacitive materials initially identified. The following figures show a summary of the materials reviewed.

BURIED CAPACITANCE									
MATERIAL SUPPLIERS	PRODUCTS	DIELECTRIC MATERIAL	Dk @ 1MHz	Cp @ 1MHz (pF/cm^2)	DIELECTRIC LOSS	THICKNESS (µm)	ELONGATION (%)	DIELECTRIC STRENGTH (kV/mil)	CORE PROCESS
3M	C-Ply	Ceramic Filled Epoxy	16.0	100	0.005	14.0		>.1	Sequential Lamination
ARLON	AD5	Ceramic Filled PTFE	5.1		0.003	71.0		>45.0	Double Sided
	AD10	Ceramic Filled PTFE	10.2		0.008	61.0		>45.0	Double Sided
DUPONT	Interra HK 04	Polyimide	3.5	124	0.003	25.0	>50	6.5	Double Sided
	Interra HK 11	Press release in 2004, but no data sheet from DuPont yet.							
Endicott Interconnect	0S3P	A patent 6,407,341 was received on June 18, 2002 - but no data sheet is available from Endicott yet.							
OAK-MITSUI MITSUI KINZOKU CORPORATE GROUP A Division of Mitsui Kinzoku	FaradFlex BC8	Polymer Film	4.4	480	0.016	8.0	8.5	5.0	Double Sided
	FaradFlex BC12TM	Polymer Film	10.0	700	0.019	12.0	6.0	6.2	Double Sided
	FaradFlex BC16T	Polymer Film	30.0	1700	0.019	16.0	N/A	2.8	Sequential Lamination
ROHM HAAS	InSite	SiO_2			0.020			40.0	
SANMINA-SCI	ZBC 1000	FR-4	5.0	155		25.0			Double Sided
	ZBC 2000	FR-4	4.1	78		50.0			Double Sided

Figure 3: Embedded Capacitance Material Spreadsheet

EMBEDDED RESISTANCE								
MATERIAL SUPPLIERS	PRODUCTS	RESISTOR MATERIAL	OHMS PER SQUARE (OPS)	MATERIAL TOLERANCE (%)	TCR (Temp Coeff of Resist - Max PPM/°C)	ETCHING	PTF vs. FOIL	THICKNESS µm (oz)
Asahi Chemical Research	TU-00-8						PTF	
	TU-00-8M						PTF	
DUPONT	Interra	Not released yet, still in testing					PTF	
MacDermid Printed Circuit Processing Technologies	M-Pass						FOIL	
Ohmega Ohmega Technologies, Inc.	Ohmega-Ply	NiP (Nickel Phosphorous)	10, 25, 50, 100, 250	±3%, ±5%, ±5%, ±5%, ±10%	-20, -50, -80, 100, 100	3 etching cycles	FOIL	0.05 - 1.0?
ROHM HAAS	InSite	Doped Platinum	500, 1000	±10% to ±15%	<150	2 etching cycles	FOIL	18 (0.5) 35 (1.0)
TICER TECHNOLOGIES	TCR	CrSiO (Chromium Silicon Oxide)	1000	±5%	300	1)Ammoniacal 2)Alkaline Permanganate 3)Ammoniacal	FOIL	18 (0.5) 35 (1.0)
	TCR	NiCr (Nickel Chromium)	10, 25, 50, 100	±5%	110	1)Cupric Chloridce 2)Ammoniacal	FOIL	18 (0.5) 35 (1.0)
	TCR	NCAS (Nickel Chromium Aluminum Silicon)	10, 25, 50, 100, 250	±5%	-20	1)Ammoniacal 2)Acidic Permanganate 3)Ammoniacal	FOIL	18 (0.5) 35 (1.0)
SANMINA-SCI	ABR			±5% to ±15%	-300	Annular Ring		

Figure 4: Embedded Resistance Material Spreadsheet

Due to Export Control restrictions, the team focused on what could be fabricated in North America. Utilizing the capabilities of North American fabricators pointed the team to the use of resistive foils. The 2007 IPC/APEX conference approached at the same time as material determinations were being made, therefore, the MAD team setup meetings with various material vendors to assist with the decision process. The Ticer TCR material was chosen as the resistance material. Part of the deciding factor was the lack of grain direction in the material due to the sputter deposition process used to manufacture the material. The TCR foil material offers a resistance range from 10 – 1000 ohms per square. This covered a broad range of values from, 33 ohms to 65k ohms, without consuming large areas of the circuit board.

Now that the vehicle has been parked at the airport, it is time to check-in for the flight and queue up to get through the security checkpoint. Recent advances in computing and networking technology have typically allowed the check-in process to be smooth and quick, however, getting through security can be quite an ordeal.

Figure 5: Getting through security

Once materials were chosen and it was time to proceed with the board layout, the next step was translating the existing layout files from the previous Mentor Graphics PADS file format into the Mentor Graphics Expedition tool. This ended up being as painful and frustrating as getting through airport security. The original schedule estimated no more than a day for the conversion process. It ended up taking at least 6 weeks. The following is a list of file translation issues encountered during the process:

- Via definition - The conversion to Expedition did not allow for multiple vias over the same span. Once in Expedition multiple vias can be assigned manually.
- Not all traces translated correctly – If a DRC error occurred during the conversion, the software removed the associated trace but still kept the net. The solution to this problem was a simple adjustment to the settings of the Design Rules Check, allowing for layouts that might be pushing the technological edge.
- The conversion did not use alternate PCB decals – Harris uses a primary and secondary footprint decal for the components. The conversion software always defaults to the primary decal. The alternate decal must be assigned manually after the conversion.
- A bug was found in the Expedition design software – When a bottom mount resistor is chosen to be converted to embedded in the Mentor EP module, the software mirrors the associated connections. The solution is to delete the trace connecting to the component. Mentor says they have fixed this.

After navigating the security labyrinth it is then time to wade through the pedestrian traffic and find the gate. This is similar to the design layout stage. The boundaries for the layout were fairly simple. The layout was accomplished using Expedition from Mentor Graphics. The team kept the same board outline and component placement so existing test fixtures could be used later for testing the board assemblies. The team also decided to keep the pads for the previous discrete capacitors in place but not populate the parts during assembly, and also to place test points where the discrete resistors were once located. This was done to aid the debug process later.

As the design layout was progressing, the team identified three areas where cost savings from using embedded passives could be quantified. The first was the cost savings associated with the actual elimination of the parts. The second area was the cost savings from the reduced assembly time of the board. The third and most difficult cost saving was related to the cost of quality. This included cost savings based on the reduced amount of rework associated with assembly defects. These three areas were then combined into a total cost savings resulting from part count reduction, shown in the figure below. This does not factor in the additional cost of the board material.

COST SAVINGS		$37.88
-Part Cost		
	CAPACITORS	$1.19
	RESISTORS	$9.77
-Cost of Quality		
	Component	Body
	CAPACITORS	$4.04
		0603
		0402
	RESISTORS	$11.06
		0201
		0402
-Assembly Cost		$11.82
	Total Parts	591

Figure 6: Cost Savings Due To Part Count Reduction

A preliminary quote was received from one of the potential fabricators, for a bare board with embedded resistance and capacitance. This was obtained to see if there could be the potential for cost reduction. The bare board cost estimate was based on the 25% smaller size of the board, which allows for 40 boards per panel instead of the current 16 per panel (see figure below). Even though the embedded material added cost to the panel, getting more boards per panel actually kept the cost of the board from increasing significantly. The cost of the bare board only increased 23%. The cost of the assembled board, therefore, went down by an estimated $24.28 when the cost savings from reducing the part count was factored in.

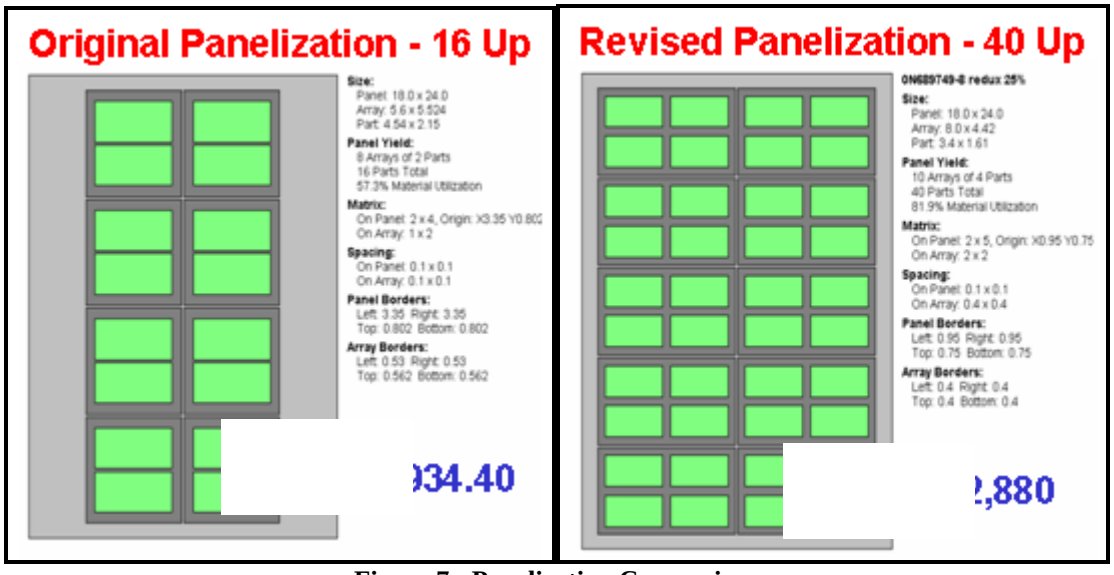


Figure 7: Panelization Comparison

As the quest for EP knowledge continued, the team stumbled across an Embedded Passives Cost Calculator created by Dr. Sandborn of CALCE. The calculator can be downloaded from the following link:
http://www.calce.umd.edu/contracts/AEPT/restricted/EmbeddedPassivesTool.htm
Shown below is the result of a preliminary cost analysis using the CALCE EP Cost Calculator. While it shows the cost of the board increasing, the total cost of the PCB assembly actually goes down because of the reduced number of parts and improved yields. This supported the findings from the earlier manual calculations and validated that the team was on the right track. The traveler is now at the right gate, waiting to board the plane.

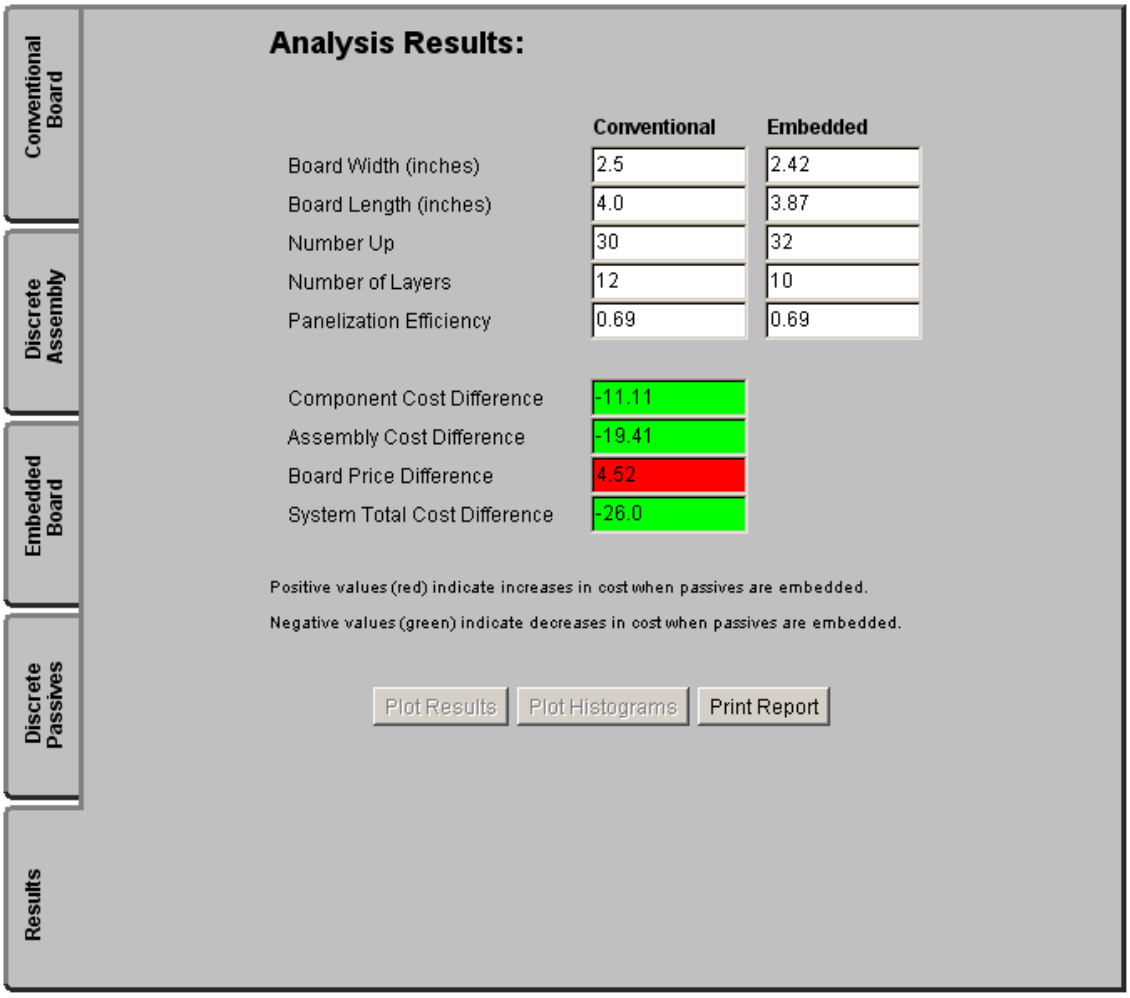


Figure 8: CALCE Embedded Passives Cost Calculator

One of the primary constraints for this conversion was that the embedded design should not deviate very far from the original design. Component placement, trace and via layout changes were kept to a minimum. The buried capacitance was accomplished by adding four layers to the existing stackup that were placed between layers 2-3 and 14-15 of the 16 layer board. The original stackup was placed between these capacitance layers. However, by doing this, a new microvia structure that went from layers 1-4 was unintentionally created. The microvia in the original design was from layers 1-2.

Excitement builds as the ground crew announces that the flight will begin boarding. The excitement quickly turns to frustration as everyone rushes to the door and tries to board first. Similarly, once the PC board layout design had been completed it was hoped that most of the problems had been left behind and the fabrication stage would proceed smoothly. The board design was sent to the selected fabricator for their review, and it turned out that they found a few problems. The first issue appeared when the fabricator found some shorts on the microvias from layer 1 to 4. The next issue was that the 25 OPS resistance material in the material database was set to 10 OPS. The review process took approximately 2 months to make the changes and send new gerber files. Once these issues had been resolved it was time to build the board. In other words, it was time to finally start flying to the destination.

The Flight (Fabrication)

As the plane leaves the jetway there are usually some critical safety measures taken. First, the exits are armed and then the flight attendants describe and demonstrate basic safety instructions for the passengers. While it might seem simple, repetitive and sometimes a distraction, it nonetheless is an important part of ensuring the plane and passengers arrive at their destination safely. This process is similar to choosing a circuit board fabricator. It is critical that there be a good match of fabricator knowledge, experience and capabilities with the materials that are chosen. If the circuit board fabricator is asked to use a new material that requires additional equipment or requires new processes and techniques then it is most likely going to add significant cost and time to the project.

The team started looking at circuit board fabricators that had experience in dealing with the chosen materials. It was key that the fabricator not be learning at the same time the team was learning. The emphasis was placed on minimizing the learning curve for the fabricator. This, however, proved to be much more difficult than anticipated.

It was a surprise to find that quite a few fabricators had some experience with buried capacitance. If fact, all of the advanced level fabricators contacted had used varying levels of buried capacitance in their production boards. All were in the form of planar capacitance and not in discrete or mezzanine outlines. Another aspect encountered was the Sanmina patent for buried capacitance. All of the fabricators looked at had to be licensed to build with buried capacitance. This is an important item to keep in mind if any buried capacitance boards are going into production.

A quick trade study was conducted that optimizes the material selection with the capabilities of the fabricator. This required very explicit questioning of the fabricator to verify that they actually had experience with utilizing the specific materials identified. There are some fabricators that will say they have used the material in question, or were familiar with it, but it usually isn't until a purchase order is placed when it is found that the fabricator needs to establish a new process. A few tips for gaining confidence that the fabricator has experience with the selected material include:

A) See if the specific material is in stock at the fabrication facility
B) Ask for samples of previous boards fabricated with the specific material
C) Review process reports associated with the specific material

Be aware that using a new material that a fabricator is unfamiliar with will have a significantly long lead-time associated with it. It doesn't mean the material cannot be used, but the project needs to know up front that there is a lot of work associated with getting the process up and running, even for small run quantities.

For buried capacitance, the fabricator had to have experience in handling thin-core material. This thin material, 0.6 mils [16 microns], needs special handling to keep it from being damaged during etch. Below three or four mils, it takes a unique handling process to keep the material from getting wrapped up in the rollers and allow people to handle the material without damaging it, which could cause a short between the power planes. This material also has the added restriction of being a sequential lamination to etch. In other words, both sides cannot be etched simultaneously.

The resistor material supplier was asked to give a list of fabricators who had experience using their material. Most of the fabricators were not located in North America, so the list was quickly narrowed down. The fabricators that were contacted all had used the material previously, but they did not have a tremendous amount of experience with it. They had all done limited proof of concept boards. In the end, the team settled on a fabricator that offered to support the project with minimal cost and had an interest in further developing their processes for embedded passives.

After hearing the safety announcements the plane taxis out to the runway for take-off. Some passengers consider this one of the more thrilling parts of the trip, and it is a time when many complex events are happening at once.

The material had to be coordinated from the suppliers to arrive at the fabricator with minimal delay. The capacitive material was a special order with 0.5/0.5 copper over the core and was made in Japan. The resistive copper foil was to be laminated on lead-free FR4 0.004" thick laminate. It took an added effort to verify that the resistive copper foil did not get lost. While it is easy to order the resistive copper foil, having the copper foil applied to the FR4 laminate at the PCB fabricator is not the best option. It is preferred to have the copper foil added to the laminate at a laminate supplier to ensure the best possible level of quality. This is one of those items that were not evident until it came time to act upon it, and then it added 5 additional weeks to the schedule.

Almost every flight encounters turbulence. The embedded passives team had its share as the board moved through the fabrication process. This includes design errors that had not been caught during review as well as process issues that arose due to the complexity of self imposed design constraints.

The beginning of fabrication was delayed as a result of the need to set up a complicated new permanganate heated bath for the 1000 OPS resistive material at the board house. Once the bath was emplaced it took some time to adjust the etching process. There was also some additional time required to establish the laser drilling, since it was the first time it had been used for the BC16T material. This highlights the necessity to match the materials chosen with the capabilities of the fabricator.

There seems to be a law, irrevocably decreed, that when on a flight with in-flight entertainment the airline must show the worst movies ever made. In the main cabin there is also no choice about when to watch the movie. In some ways the embedded passives project was like this. The material suppliers and board fabricator had graciously volunteered their time

and materials to the effort. However, as a result, this effort was understandably not always their top priority. This caused delays in a schedule that had already been established with a very generous timeframe. Even with the occurrence of many unplanned challenges, the team remained on schedule and the boards were delivered in time to be assembled within the 18 month timeline.

Destination Arrival (Assembly & Evaluation)

While the airplane approaches its final destination there is a flurry of activity as the flight attendants prepare for landing. This includes the oft repeated phrase to turn off all electronics, fasten seatbelts and return the tray tables to their upright and locked position. These procedures are similar to what took place in preparing the SMT manufacturing personnel for the upcoming embedded passives board assembly.

The most significant assembly issue encountered was programming the pick-n-place equipment with the output files from Expedition. There were many parts that came through without orientation information. This created a flood of e-mails from the SMT group asking for clarification regarding the direction of the parts on the board. Once programming was completed, the assembly proceeded without any other incidents.

As the plane lands and arrives at the jetway, the passengers quickly escape the environs of the plane and race to claim their baggage. The racing is futile, however, because upon reaching the baggage area everyone stands around for what seems like an eternity to grab their bag and go. The MAD team experienced a similar situation as the assembled boards were to be tested and evaluated. While this paper is being written the boards are being functionally tested and their performance assessed. If problems are found, it is expected that the troubleshooting will take time as the root-cause analysis effort is coordinated. The MAD team is eagerly waiting for the results and the opportunity to share them. So now that the airplane journey has concluded it is time to get in line for hailing a taxi and prepare for another thrilling adventure to find out how well the boards with embedded passives perform.

Figure 9: Waiting for the taxi

Biographies

HARRIS CORPORATION – RF COMMUNICATIONS DIVISION

Located in Rochester, NY, Harris RF Communications is a leading supplier of secure voice and data communications products, systems, and networks to military, government, and commercial organizations worldwide. Harris Corporation (NYSE:HRS) is an international communications and information technology company serving government, defense and commercial markets in more than 150 countries. Headquartered in Melbourne, Florida, the company has annual revenue of over $4 billion and 16,000 employees — including nearly 7,000 engineers and scientists. Harris is dedicated to developing best-in-class assured communications™ products, systems, and services. Additional information about Harris Corporation is available at www.harris.com.

BILL DEVENISH

Bill Devenish has 20 years of engineering and management experience in the telecommunications and wireless world. His work with various international companies has provided exposure to an assortment of global product development cultures. Bill has worked for Motorola, NEC, Nokia and a few, small, start-up companies. He currently leads the MAD (Mechanical Advanced Development) team at Harris RF Communications. Bill received his Bachelors degree in Design Engineering from Brigham Young University and a Masters degree in Engineering Management from Oregon Graduate Institute.

ANDREW PALCZEWSKI

Andrew Palczewski has over 15 years of printed circuit board design experience in telecommunications and industrial products. He has a strong background in advance technology and manufacturability. Andy has worked for Corning, International Game Technology and a multitude of other progressive companies. Andy's current role at Harris RF Communications is that of a PCB Technologist in developing strategic planning for printed circuit boards.

The Embedded Passives Journey

Authors:

Bill Devenish – Harris Corp., Mechanical Advanced Development (MAD)

Andrew Palczewski – Harris Corp., PCB Technologist

HARRIS®

- RF Communications Division located in Rochester, NY
- Develops and manufactures tactical two-way radios

Choosing a Destination

1976-GE 8 Track Player

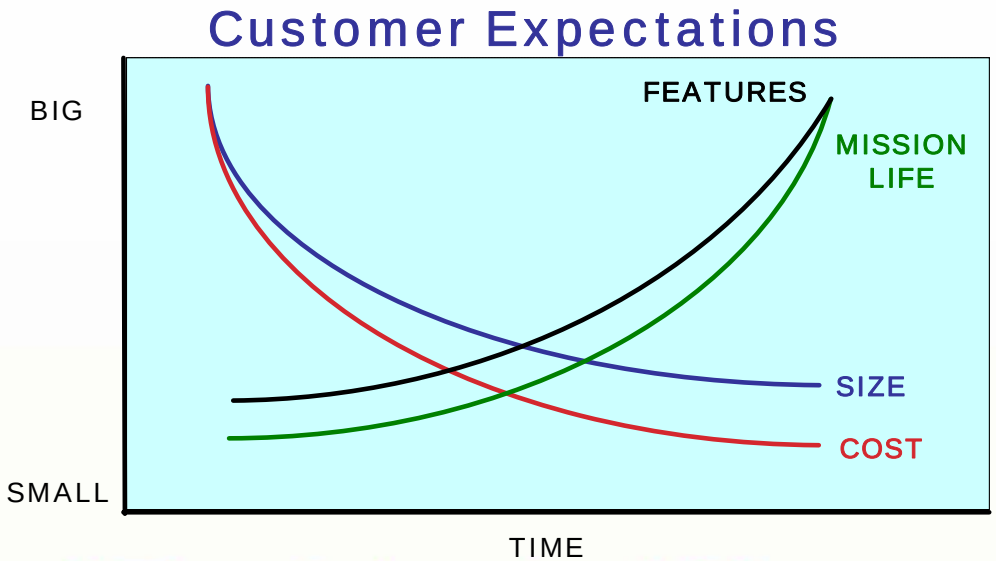
1980-Sony Walkman

2001-Apple iPOD

1984-Sony Discman

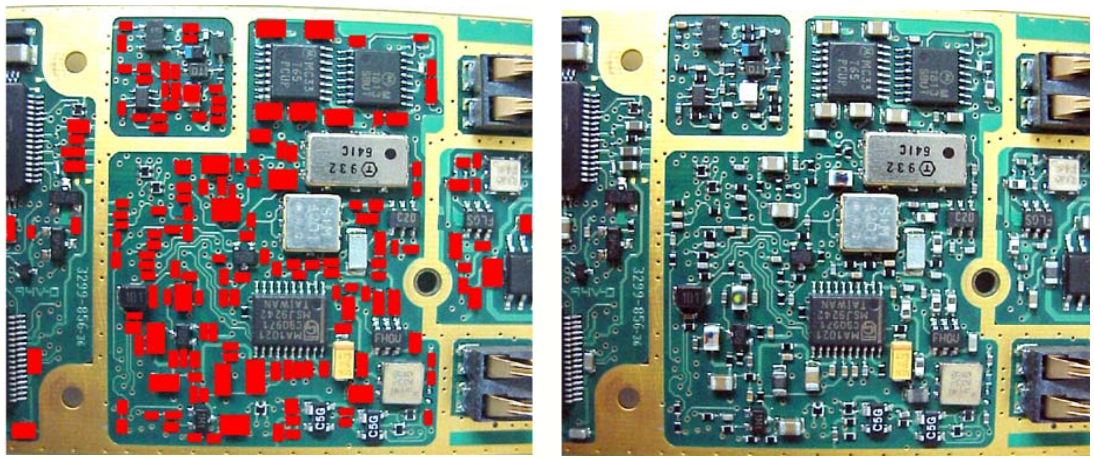
2007-Apple Shuffle

Roadmapping Exercises



Choosing a Destination

Choosing a Destination



Why Embedded Passives?

- Board Area Reduction
- Performance Enhancement
- Quality Improvement & Cost Reduction

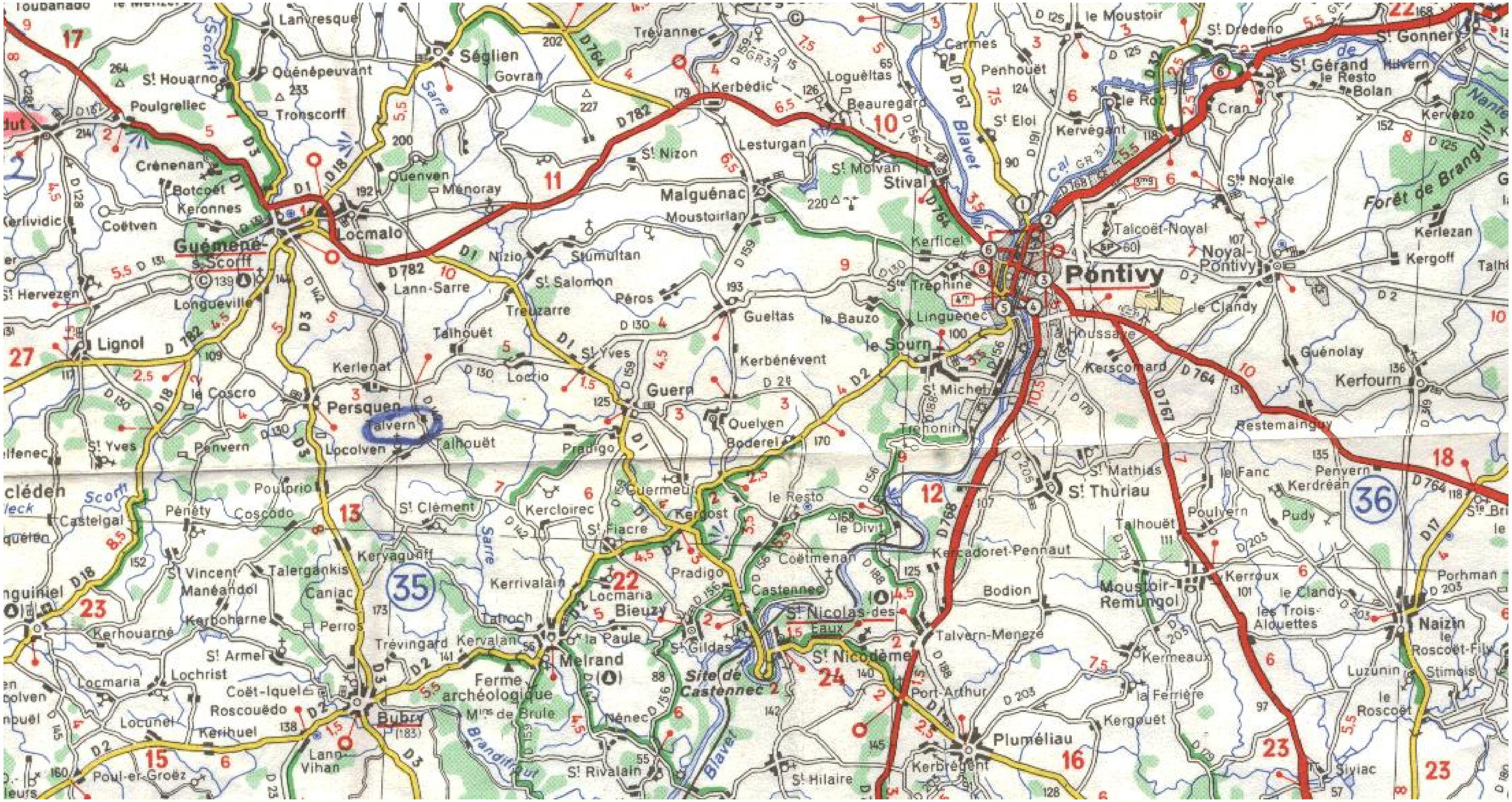
Planning the Trip

Planning the Trip

Embedded Passives Travel Agents:

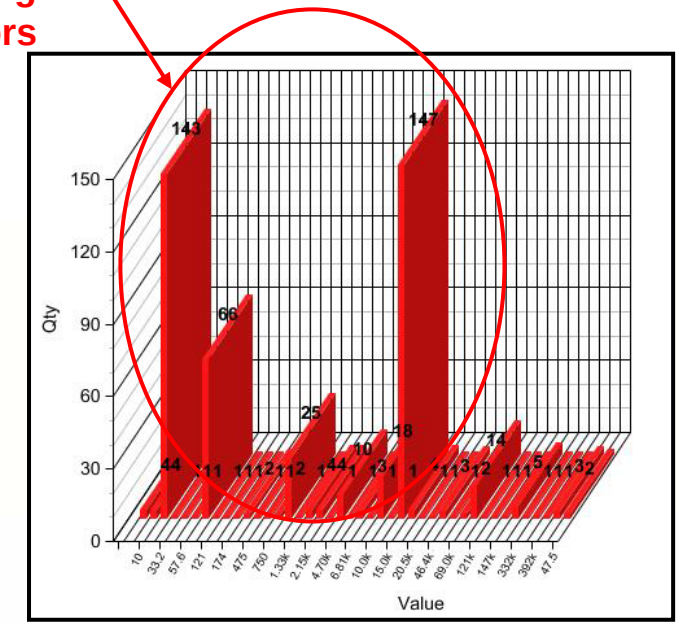
- Dr. Richard Ulrich, University of Arkansas (www.uark.edu)
- CALCE, University of Maryland (www.calce.umd.edu)
- Mike Fitts, Plexus Technology Group (www.plexus.com)
- Happy Holden, Mentor Graphics (www.mentor.com)

Planning the Trip

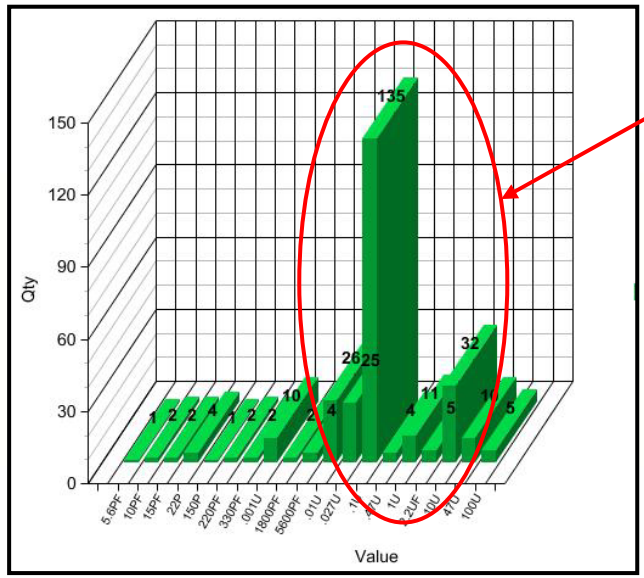


Planning the Trip

Targeted pull-up/down & terminating resistors



Resistors



Capacitors

Targeted by-pass & de-coupling caps

Project Goal:

- Component area reduction of 25%
- Demonstrate area reduction on existing digital board

Airport Arrival (Material)

Airport Arrival (Material)

EMBEDDED RESISTANCE

MATERIAL SUPPLIERS	PRODUCTS	RESISTOR MATERIAL	OHMS PER SQUARE (OPS)	MATERIAL TOLERANCE (%)	TCR (Temp Coeff of Resist - Max PPM/°C)	ETCHING	PTF vs. FOIL	THICKNESS µm (oz)
Asahi Chemical Research	TU-00-8						PTF	
	TU-00-8M						PTF	
DUPONT	Interra	Not released yet, still in testing					PTF	
MacDermid	M-Pass						FOIL	
Ohmega	Ohmega-Ply	NiP (Nickel Phosphorous)	10, 25, 50, 100, 250	±3%, ±5%, ±5%, ±5%, ±10%	-20, -50, -80, 100, 100	3 etching cycles	FOIL	0.05 - 1.0?
ROHM HAAS	InSite	Doped Platinum	500, 1000	±10% to ±15%	<150	2 etching cycles	FOIL	18 (0.5) 35 (1.0)
TICER TECHNOLOGIES	TCR	CrSiO (Chromium Silicon Oxide)	1000	±5%	300	1)Ammoniacal 2)Alkaline Permanganate 3)Ammoniacal	FOIL	18 (0.5) 35 (1.0)
	TCR	NiCr (Nickel Chromium)	10, 25, 50, 100	±5%	110	1)Cupric Chloridce 2)Ammoniacal	FOIL	18 (0.5) 35 (1.0)
	TCR	NCAS (Nickel Chromium Aluminum Silicon)	10, 25, 50, 100, 250	±5%	-20	1)Ammoniacal 2)Acidic Permanganate 3)Ammoniacal	FOIL	18 (0.5) 35 (1.0)
SANMINA-SCI	ABR			±5% to ±15%	-300	Annular Ring		

BURIED CAPACITANCE

MATERIAL SUPPLIERS	PRODUCTS	DIELECTRIC MATERIAL	Dk @ 1MHz	Cp @ 1MHz (pF/cm²)	DIELECTRIC LOSS	THICKNESS (µm)	ELONGATION (%)	DIELECTRIC STRENGTH (kV/mil)	CORE PROCESS
3M	C-Ply	Ceramic Filled Epoxy	16.0	100	0.005	14.0		>1	Sequential Lamination
ARLON	AD5	Ceramic Filled PTFE	5.1		0.003	71.0		>45.0	Double Sided
	AD10	Ceramic Filled PTFE	10.2		0.008	61.0		>45.0	Double Sided
DUPONT	Interra HK 04	Polyimide	3.5	124	0.003	25.0	>50	6.5	Double Sided
	Interra HK 11	Press release in 2004, but no data sheet from DuPont yet.							
Endicott Interconnect	0S3P	A patent 6,407,341 was received on June 18, 2002 - but no data sheet is available from Endicott yet.							
OAK-MITSUI	FaradFlex BC8	Polymer Film	4.4	480	0.016	8.0	8.5	5.0	Double Sided
	FaradFlex BC12TM	Polymer Film	10.0	700	0.019	12.0	6.0	6.2	Double Sided
	FaradFlex BC16T	Polymer Film	30.0	1700	0.019	16.0	N/A	2.8	Sequential Lamination
ROHM HAAS	InSite	SiO_2			0.020			40.0	
SANMINA-SCI	ZBC 1000	FR-4	5.0	155		25.0			Double Sided
	ZBC 2000	FR-4	4.1	78		50.0			Double Sided

Identifying Materials:

- Resistance: Ticer TCR, 25 & 1000 OPS
- Capacitance: Oak-Mitsui FaradFlex BC16T
  - Roughly 55:1 replacement ratio (Risky)

Security (File Conversion)

When airport security agents get bored.

Security (File Conversion)

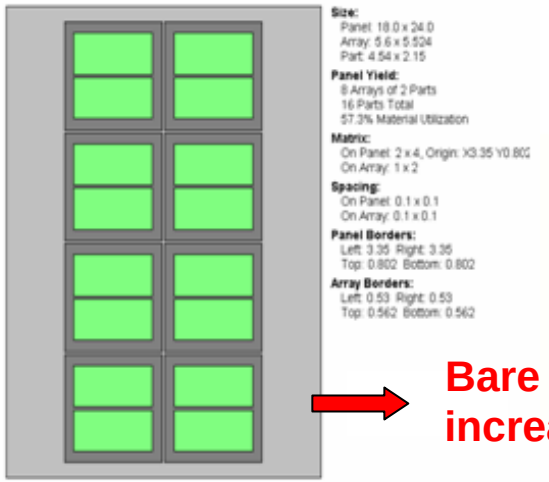
PADS File Conversion to Mentor's Expedition:

- **Via definition** - Expedition did not allow for multiple vias over the same span
- **Not all traces translated correctly** - If a DRC error occurred during the conversion, the software removed the associated trace but still kept the net
- **Conversion did not use alternate PCB decals** - The conversion software defaulted to the primary decal
- **Software bug found** - When a bottom mount resistor is chosen to be converted to embedded in the Mentor EP module, the software mirrors the associated connections

Finding the Gate (Cost)

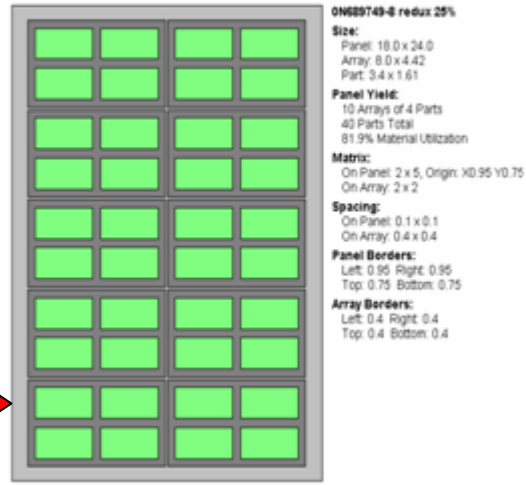
Finding the Gate (Cost)

Original Panelization - 16 Up



Bare board cost only increased by 23%

Revised Panelization - 40 Up



PC Board Cost Impact:

- 25% size reduction allowed for more boards per panel
- Higher cost of materials offset by more boards per panel

Waiting at the Gate (Cost)

Waiting at the Gate (Cost)

PART COST SAVINGS	
PART COST SAVINGS	$10.96
Capacitors	$1.19
Resistors	$9.77
COST OF QUALITY SAVINGS	$15.10
Capacitors	$4.04
Resistors	$11.06
ASSEMBLY COST SAVINGS	$11.82
TOTAL	$37.88

Reduced assembly cost of $24.28

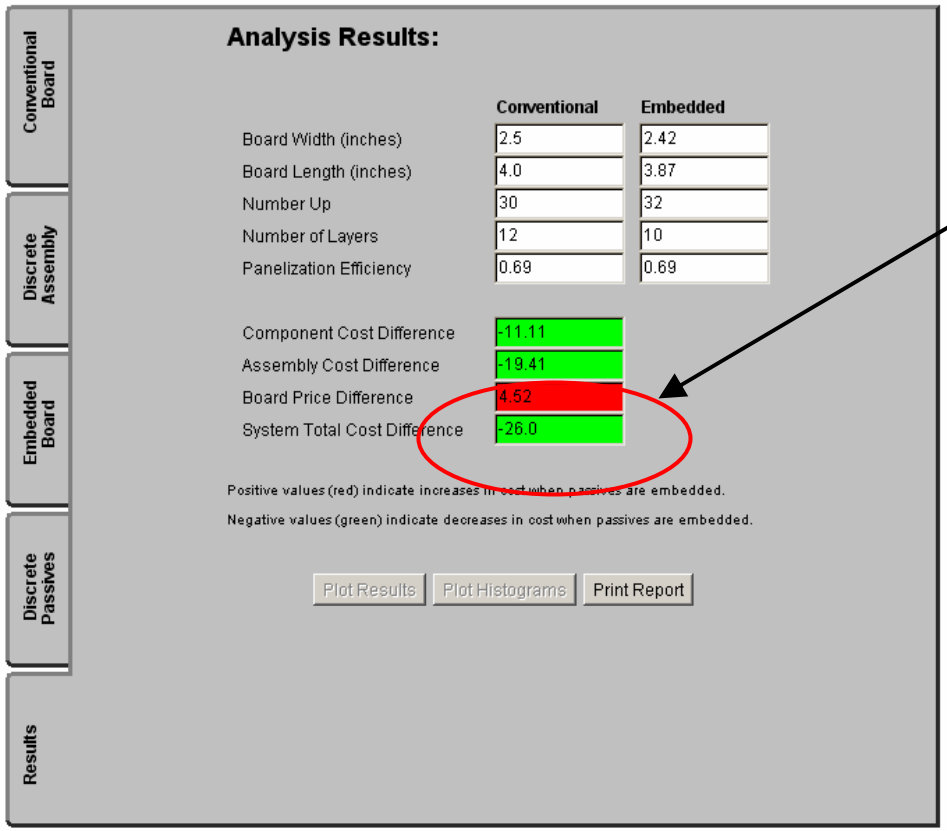
subtracted from increased bare board cost (23%)

Discrete Component Cost Impact:

- Part cost savings are based on elimination of the parts
- Cost of quality savings result from less rework and repair
- Assembly cost savings are due to less pick-n-place and inspection time

Flight Announcement (Cost)

Flight Announcement (Cost)



Compare to manually calculated cost savings of $24.28

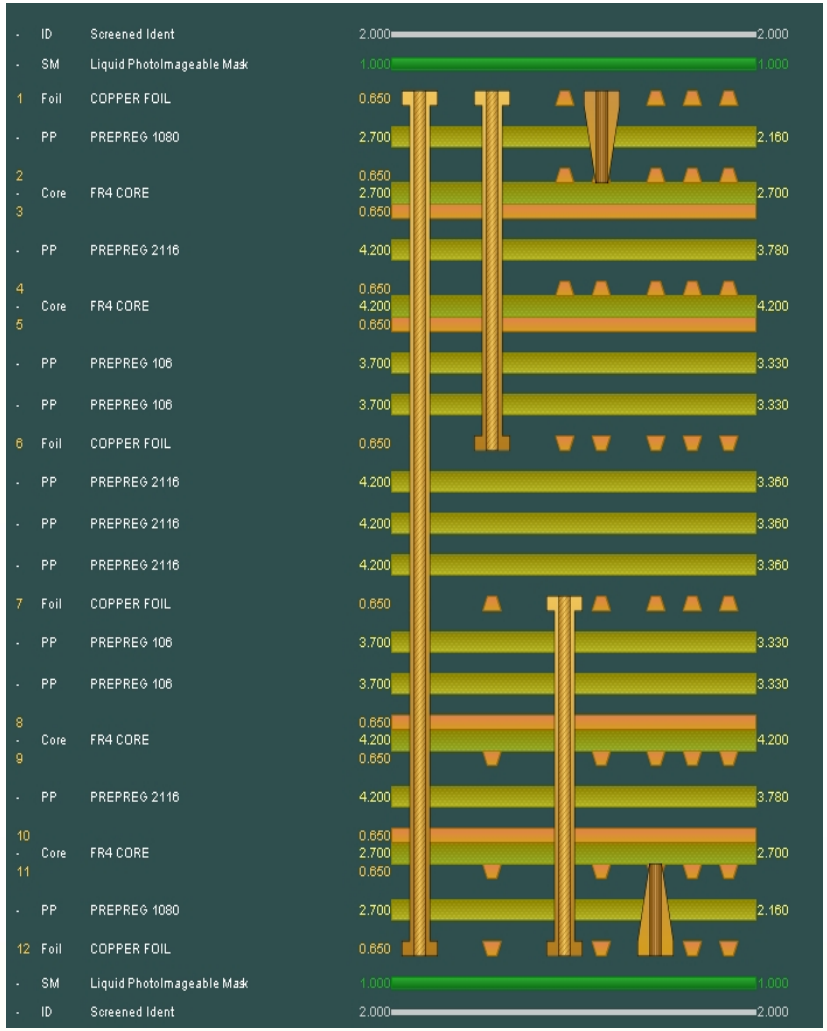
CALCE Cost Calculator:

- Used to validate manual cost calculations

Boarding (Design)

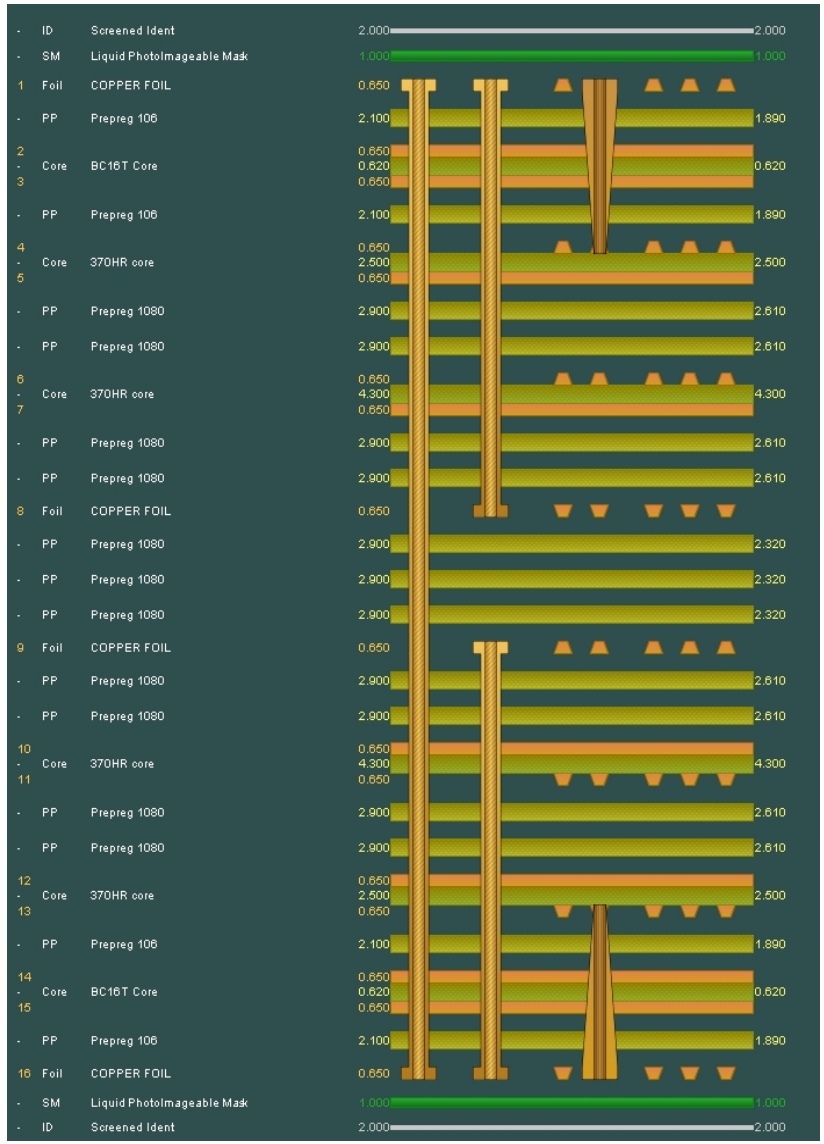
Boarding (Original Stackup)

- 12 Layers
- .064” Thick
- FR4 Material
- No Embedded Layers
- Statistics
  - 986 Parts
    - 538 Top
    - 448 Bottom
  - 5332 SMD Pads
    - 2792 Top
    - 2538 Bottom



Boarding (New Stackup)

- 16 Layers
- .073” Thick
- Isola 370HR
- Embedded Layers:
  - BC16T between:
    - L2, L3 & L14, L15
  - TCR
    - 25 ops – L5, L12
    - 1000 ops – L7, L10
- Statistics
  - 437 Parts
    - 226 Top
    - 211 Bottom
  - 4254 SMD Pads
    - 2180 Top
    - 2074 Bottom



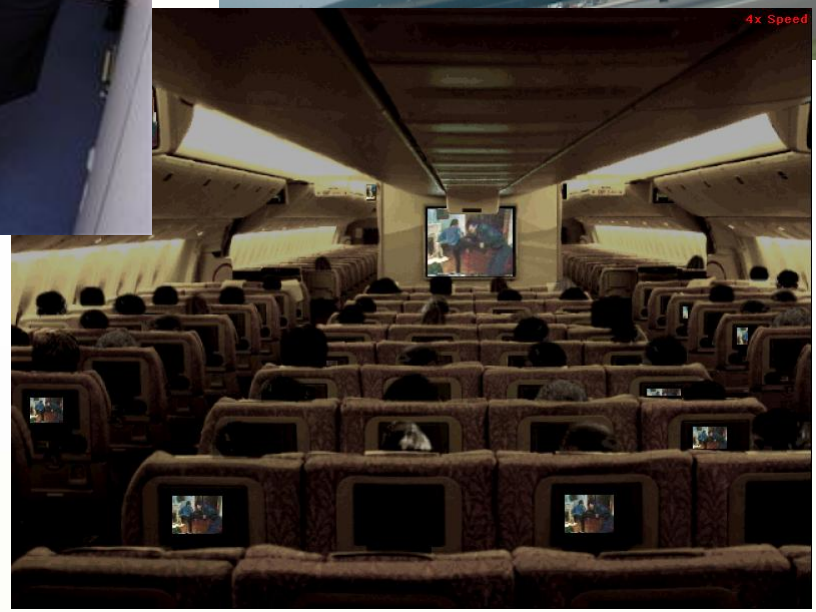
Safety Briefing (Design Review)

Safety Briefing (Design Review)

Design Review Tips:

- Compare BoM
  - Verify that all of the other parts are still accounted for
- Check for microvia shorts
- Add test points, if needed
- Check space between resistors to allow for copper flooding in-between
- Verify materials database
  - Resistor material was set to 10 OPS instead of 25 OPS

The Flight (Fabrication)



The Flight (Fabrication)

Finding the Right Fabricator:

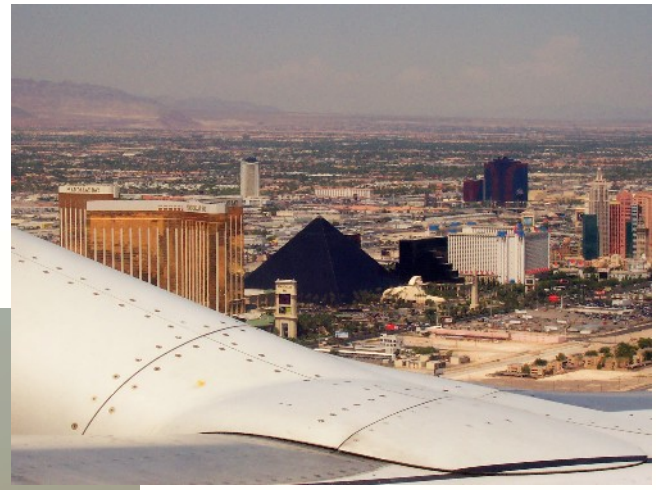
- Match the fabricator with the material to be used
- See if the material is in stock at the fabrication facility
- Ask for samples of boards fabricated with the material
- Review process reports associated with the material

The Flight (Fabrication)

FABRICATION:

- NEW MATERIAL - The fabricator had to setup a heated permanganate bath for the 1000 OPS resistive material
- Specialized handled required for thin capacitance material
- Capacitance material required sequential lamination
- Additional time in the schedule needed for laser drilling of the capacitance material

Destination Arrival (Assy & Eval)



Destination Arrival (Assy & Eval)

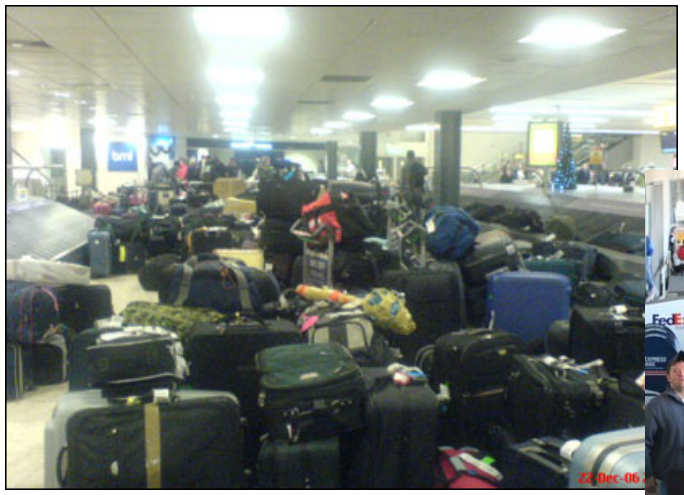
ASSEMBLY:

- Prepare the SMT assembly personnel in advance
  - They kept asking why all of the parts had disappeared
- Programming the pick-n-place machine
  - Many parts in the assembly file had no orientation information

EVALUATION:

- The boards are currently being tested and evaluated
  - No results to share at this time

Waiting for the Taxi (Results?)



Maybe next year we can share the evaluation results